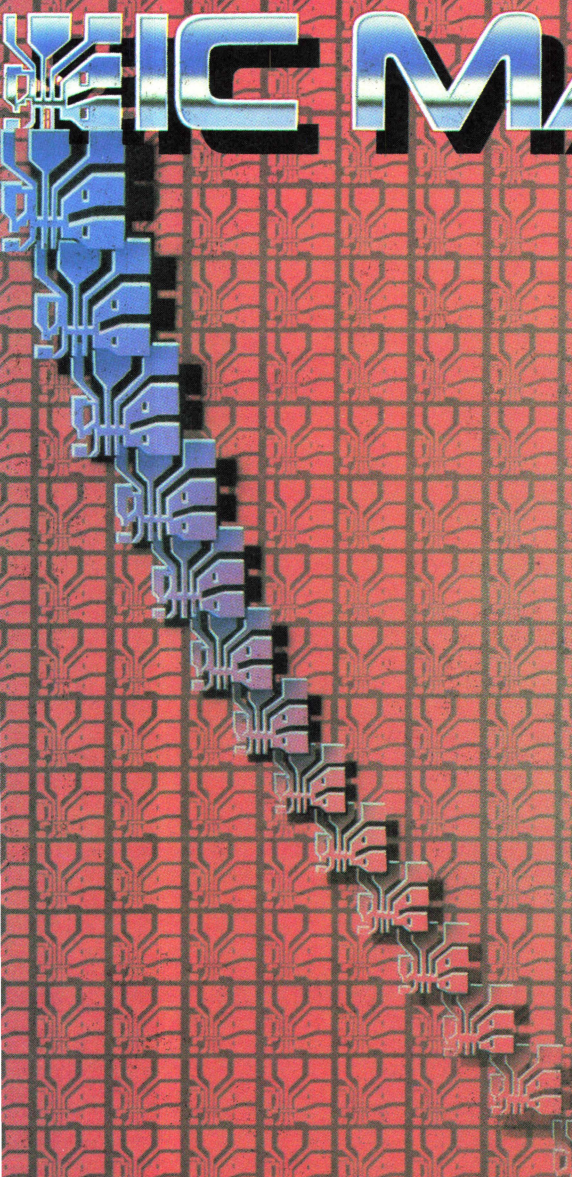


1988

# IC MASTER

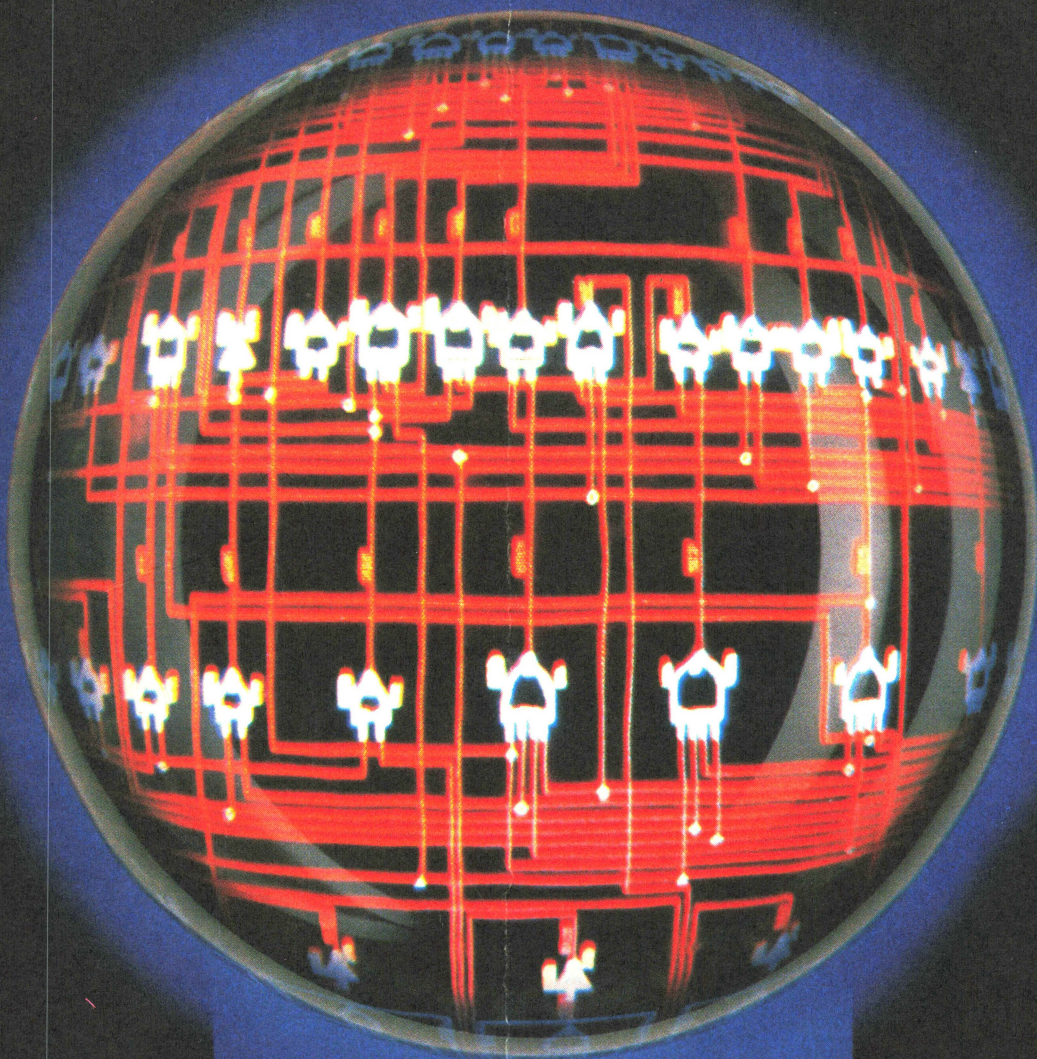


3

ASIC & Design Automation,  
 $\mu$ P Development Systems  
& Microcomputer Boards



AT&T ASICs: We predict  
performance so you can  
protect your investment.





**Advanced CAD tools,  
developed by AT&T  
Bell Laboratories,  
accurately predict  
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Complexity is AT&T's stock in trade. Our capabilities go all the way to 25,000 + gates,

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Start your design at the front end, or just come in for the finishing touches. Either way, we have the people, resources, training assistance, and commitment to help you every step of the way.

Is AT&T ready, right now, to help you build a foolproof standard-cell solution? The answer, predictably, is yes.

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*The Development System that Supports 150 Different Microprocessors.*

## A complete solution

Here, at last, is the working environment of the future for developing error-free and efficient microprocessor code. Save time and money with UniLab II's seamlessly integrated toolset:

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Use UniLab's advanced windows to set up your screen the way you want to... view multiple items of interest. Imagine being able to automatically compare a current trace with previous trace data to instantly determine differences. You can set breakpoints, single-step, then go back to the analyzer without missing a beat. If you make a change in your code, use UniLab's built-in line-by-line assembler to instantly patch the fix and test the results. Think of the time savings.

## Find Bugs Fast

Searching for bugs by single-stepping through suspect code can take forever. Now, with UniLab, just specify the bug symptom you are looking for as a trigger spec and let UniLab catch the bug for you as your program runs in real time.

On-Line Help menus, Command Glossary, and Word List.

Pop-up Mode Selection panel called by soft key.

## Get Running Fast

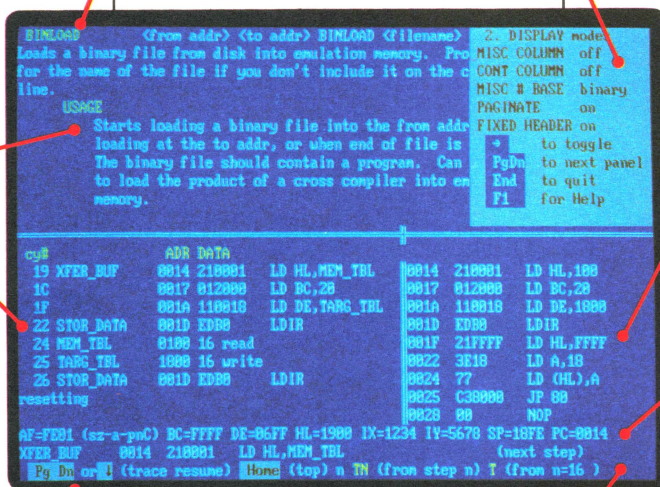
You probably won't use your development system every day. You do need a system that's easy to learn, and easy to come back to. That's UniLab. It lets you use commands or menus—or a mixture of both. The same commands work for all MPUs. Useful help screens, an on-line manual & glossary, instant pop-up mode panels, a quick command and parameter reference, are at the ready.

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At less than \$5,000 UniLab costs less than our less-able competitors. You can add our new Program Performance Analysis option to help you optimize your software. If you don't need UniLab's power, other models are available from \$2,995. Get

the story on UniLab II and how it can revolutionize your software design efficiency, as it has for thousands. Universities, ask about our Education Outreach Discount Program.

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**In California call (415) 361-8883.**



Windows can be used to view source files, previous traces, and more.

Symbol translation or source code line display.

Screen displays scroll off into history buffer—can be viewed later.

UniLab trace filtering eliminates extraneous information and shows you only the program steps of interest.

Context sensitive prompt line.

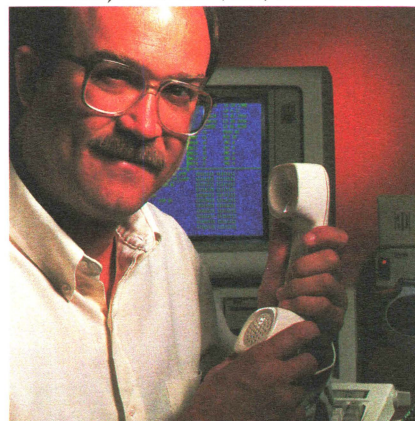
Disassembly of code in memory can be compared with trace in adjacent window.

Symbolic breakpoint register display.

## Set up for any 8- or 16-bit processor in seconds!

Thanks to our innovative emulation approach, moving between processor types requires only a new emulation module and software change. You save both money and time: Our inexpensive

Personality Paks™ (only about \$500) include all the items you need for fast hook-up. Orion MicroTargets™ functioning target circuits for popular MPUs, let you test your software before your own hardware is ready.



**When you own or rent a UniLab II, you get access to Orion's team of Applications Engineers.**

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INSTRUMENTS, INC.

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# IC MASTER

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## HOW TO USE THE IC MASTER

The 1988 edition of the IC MASTER is arranged in three volumes. Each volume serves a specific purpose to help you find the integrated circuit or related product you need. The table of contents on page 1 describes what is in each volume. The table also includes the starting page number for each advertiser.

The IC MASTER is a functional work. You know what you need. The MASTER helps you find it.

Here are typical problems.

### Q. What kinds of functions does the MASTER cover?

A. Turn to page 8 in **Volume One**. Here is a complete list of the devices covered. The page and line numbers refer you to the beginning of the Section in which a particular function appears.

### Q. Who makes a 16384 x 1 static RAM with an access time of 70ns or faster? What are my technology choices?

A. Pick up Volume 1. Turn to the MEMORY section. The first page of the section tells you where the listings of your device begin. See this under:

RAMs  
Bubble  
Dynamic  
**Static**

Turn to the first page of static RAMs. In the first column you see the **Organization**. Browse through the pages until you reach the **16384 x 1** listings. Now look through the listings until you find the access time and characteristics you need. Device numbers are shown by manufacturer. The device numbers of advertisers in the 1988 IC MASTER appear in **bold face**. The page number following the device number is where additional information may be found in **Volume Two**. At the extreme right you will see line numbers. These are the specific lines where a device appears.

### Q. Which microprocessors are listed in the MASTER? How do I find the microprocessor I need?

A. All commercially available microprocessors are listed in the MASTER. Start with the **microprocessor** listing in the **Master Selection Guide Index** (starts on page 8). Here you will find the various kinds of products you will need listed according to function and bit size. Turn to the various pages shown and then to the advertiser's page where more detail may be available.





# IC MASTER

**Q. Who makes a Dual, Low Offset Voltage OpAmp?**

A. This is a **LINEAR** device. Turn to the LINEAR section in Volume One. The first page of the section shows the starting page for each type of device. Turn to the page where **Dual Units** appear. Look down the list for the device you need. Advertisers' devices are listed in **bold face**. Turn to the page in Volume Two where more information may be available.

**Q. I need an IC with Music capability. Which Master Selection Guide should I use?**

A. Turn to the **Master Selection Guide Index** starting on page 8. Look through the list until you find **Music**. The page numbers for each kind of device are shown.

**Q. I plan to use a digital gate array or some other semicustom ASIC in my next project. Where do I find it in the MASTER? Who makes these things?**

A. Turn to Volume Three. Turn to the first page of **ASICs/Custom**. Find Gate Arrays and all of the other devices listed here. Now you can find the device you need. After you find the type of device you need, turn to the proper page and find the manufacturer. Advertisers' pages follow the selection guides in Volume Three.

**Q. I know the digital IC I need is available. Is it available in a surface mount package?**

A. There are two ways to solve this problem. If you know the manufacturer's device number, turn to the Part Number Index in Volume One. Find the basic number and the page number and line where that device is listed in the MASTER. Turn to that page. If the device is available for surface mounting, an open diamond symbol will appear. You can also turn directly to the DIGITAL section and turn to the function of the device you want. The symbol will indicate an SMD is available.

**Q. I am looking for an application note on a specific device. Where can I find out if one is currently available?**

A. Pick up Volume One. Turn to the Application Note Directory. Here you will find app notes arranged by **function**. Find the function involved and turn to the page where the app note is listed.



**Q. We need a device that meets MIL standards. Where do I look in the Master?**

A. Turn to the **MILITARY** Section in Volume One. The Military Device Testing table shows which manufacturers do what kinds of MIL work. Read the instructions on the first page. The cross reference on the following pages tells you which commercial parts have MIL equivalents. This is followed by the MIL to commercial listing. This is followed by a cross reference of DESC drawing numbers to QPL-38510 parts. The next list is a QPL listing based on the latest Defense Electronics Supply Center (DESC) Qualified Product Listing. Additional information is often supplied by the advertisers' pages in Volume Two.

**Q. I know the basic part number is 2502 and that's all I know. Where do I look?**

A. That's easy in the **MASTER**. Turn to the Part Number Index. All prefixes and suffixes have been stripped away. Turn to the page where 2502 appears. All manufacturers with that kind of number appear in order along with the page and line number where the device is described.

**Q. How many manufacturers claim to make a pin-for-pin and function-for-function equivalent to Motorola MC68000?**

A. Turn to the Alternate Source Directory in the back of Volume One. Turn to Motorola. Those manufacturers who claim to be equivalent are listed in order. If you have an MS-DOS computer with a hard drive, you can get the 1988 IC MASTER Alternate Source Directory on a disk. The disk is Clipper compiled from dBaseIII+ and is delivered compressed by PKARC. This is the complete list of alternate sources and allows you to add notes such as your own part numbers, prices, sources and the like. Call Hearst (516) 227-1300 and ask for Book Sales for further information.

**Q. I looked in the Alternate Source Directory. The part I want an alternate source for isn't listed. Why not?**

A. Are you sure you looked through the entire listing for the original manufacturer? Some devices may be listed in odd ways depending on how the MASTER's editors receive the information. Then there is the probability that no other manufacturer makes an exact replacement for your part. It is important for you to understand how the Alternate Source Directory is compiled. Manufacturers supply the information that **their** part is an exact replacement for **another** part. The original manufacturer does **not** tell us his part can be replaced by those listed.

**Q. I need an 8/16-bit microcomputer board with an 8MHz clock frequency and a multibus support system. Can I find this in the MASTER?**

A. Yes! Pick up Volume Three. Turn to the **MICRO-COMPUTER BOARD** Section. Continue to turn pages until the 8/16 appears in the first column. Then look at all of the available boards to find the boards you can use.





# IC MASTER

**Q. I have Valid Logic's "Summary" workstation. Which front end tools are compatible? Can I get one with circuit simulation? What capabilities does it have? Who makes it?**

**A.** Pick up Volume Three. Turn to the Design Automation Section. Check the first page. You will see what is available in the Section. Under Design Tools you will find Front End Tools and Circuit Simulators. Read down for your parameters and across for the vendor.

**Q. What do the manufacturers' part numbers mean? I have a Signetics N8X02N. What do all the letters and numbers mean?**

**A.** Look in Volume One for the Part Number Guide. Turn to the Signetics portion. Now you know the **N** prefix means, zero to plus seventy degrees Centigrade. The **N** suffix indicates the package style. The numbers and letters in the middle are the device type. Each manufacturer has a different code system. Understanding the system is a great help in comparing devices.

**Q. I found the device I want in the MASTER. What are the pinouts? Where can I get more details? Where can I get a price? What is the delivery time?**

**A.** You have just defined exactly what the IC MASTER does. The MASTER is a guide to tell you which devices are available on a commercial basis. After you know this, the next step is to contact the manufacturer, a local sales office or a distributor.

**Q. Where can I find the addresses and telephone numbers of manufacturers, local sales offices and distributors?**

**A.** Pick up Volume Two. Turn to the Manufacturers and Distributors Directory. Read the first page. The information on this page will help you understand why the information in the Directory is so important. It will save time and aggravation.

**Q. I just saw a new device advertised in Electronic Products magazine. It isn't listed in the MASTER. Why not? When will it be listed?**

**A.** Preparing the information for the annual IC MASTER is a tremendous undertaking. It requires the cooperation of every single manufacturer. All of the material must be organized, cross referenced and placed in the data base. This data base must be closed off in November in order to meet the publishing date of late January. That is why some devices are not listed. They came on the market too late for the deadline. There are two updates to the annual MASTER. They are called the **IC MASTER UPDATE**. One is issued in the late Spring and the other in early Fall. Be sure to sign up for copies when you get your new IC MASTER. If you are not sure whether or not you have requested the updates, please write to the Circulation Department at the address shown on page 2 of this MASTER. Be sure to indicate which edition of the MASTER you are using.



## ABBREVIATIONS OF COMPANY NAMES

<b>AB Assoc</b>	AB Associates	<b>Bipolar</b>	Bipolar Integrated Tech	<b>Daisy</b>	Daisy Systems
<b>Abionics</b>	Abionics	<b>Bishop</b>	Bishop Graphics	<b>Dallas</b>	Dallas Semiconductor
<b>ACASI</b>	American Computer Automated Systems	<b>Bit3Comp</b>	Bit 3 Computer Corp	<b>Dasoft</b>	Dasoft Design Systems
<b>ACE</b>	Action Computer Enterprise	<b>Brainpower</b>	Brainpower		
<b>Acotech</b>	Acotech	<b>Brooktree</b>	Brooktree		
<b>AD</b>	Analog Devices	<b>Buckminster</b>	Buckminster Corp	<b>DataGen</b>	Data General
<b>AdvControl</b>	Advanced Control Systems Corp.	<b>Bummer</b>	Bummer Electronics	<b>DataI/O</b>	Data I/O
<b>AdvDigital</b>	Advanced Digital Corp.	<b>Burr-Brown</b>	Burr-Brown Corporation	<b>DASystems</b>	Data Systems
<b>AdvEngSol</b>	Advanced Engineering Solutions			<b>dataCon</b>	dataCon Inc.
<b>AdvLinear</b>	Advanced Linear Devices			<b>Datacube</b>	Datacube Inc.
<b>AdvMicroSys</b>	Advanced Micro Systems	<b>Cadarn</b>	Cadarn	<b>Dataram</b>	Dataram Corporation
<b>AIArchitects</b>	A. I. Architects Inc.	<b>CAD Group</b>	CAD Group	<b>DataTrans</b>	Data Translation
<b>Aida</b>	Aida	<b>Cadic</b>	Cadic, Inc.	<b>Datel</b>	Datel
<b>AjidaTech</b>	Ajida Technologies	<b>Cadnetix</b>	Cadnetix	<b>Datricon</b>	Datricon Corporation
<b>Alcyon</b>	Alcyon Corp.	<b>CAECO</b>	CAECO	<b>Davidge</b>	Davidge Corp.
<b>Aldec</b>	Aldec	<b>Caedent</b>	Caedent	<b>DEC</b>	Digital Equipment Corp.
<b>AllenSys</b>	Allen Systems	<b>Calay</b>	Calay Systems	<b>Den/Pas</b>	Densan/Pascot
<b>Alloy</b>	Alloy Computer Products	<b>CalDevices</b>	California Devices	<b>Dense-Pac</b>	Dense-Pac
<b>Alphatron</b>	Alphatron	<b>Calma</b>	Calma	<b>Devtek</b>	Devtek Systems
<b>Altera</b>	Altera	<b>Calmos</b>	Calmos Systems	<b>Dexter</b>	Dexter Research Center
<b>AMA</b>	American Automation	<b>Calos</b>	Calos	<b>Digital RF</b>	Digital RF Solutions Corp.
<b>AMCC</b>	Applied Micro Circuits	<b>Cambridge</b>	Cambridge Digital Systems	<b>Digitronics</b>	Digitronics Sixnet
<b>AMD</b>	Advanced Micro Devices	<b>CAN-TRON</b>	CAN-TRON	<b>Dionics</b>	Dionics Inc.
<b>Amperex</b>	Amperex Electronic Corp.	<b>CaseTech</b>	Case Technology	<b>DistComp</b>	Distributed Computer Systems
<b>Ampro</b>	Ampro Computers Inc.	<b>Catalyst</b>	Catalyst, Semiconductors	<b>DiversTech</b>	Diversified Technology
<b>Amtelco</b>	Amtelco	<b>CentData</b>	Central Data Corp.	<b>DraftingDyn</b>	Drafting Dynamics
<b>Anadigics</b>	Anadigics	<b>Cermetek</b>	Cermetek	<b>DSB Systems</b>	DSB Systems
<b>AnalDesTools</b>	Analog Design Tools	<b>CharlesRiver</b>	Charles River Data	<b>DSP-Systems</b>	DSP-Systems Corp.
<b>AnalogSys</b>	Analog Systems	<b>Cherry</b>	Cherry Semiconductor	<b>DUAL</b>	Dual Systems Corp.
<b>Analogic</b>	Analogic	<b>Chips&amp;Tech</b>	Chips & Technology		
<b>ANALOGY</b>	Analogy	<b>Chrislin</b>	Chrislin Industries	<b>ECAD</b>	ECAD
<b>Anasco</b>	Anasco Corp.	<b>CIC</b>	Custom Integrated Circuits	<b>ECISemi</b>	ECI Semiconductor
<b>Antona</b>	Antona Corp.	<b>Cirrus</b>	Cirrus	<b>EDI</b>	Electronic Designs Inc.
<b>Apex</b>	Apex Microtechnology	<b>Clarity</b>	Clarity Systems	<b>EdsunLabs</b>	Edsun Laboratories, Inc.
<b>Applicon</b>	Applicon	<b>Clearpoint</b>	Clearpoint Inc.	<b>EES</b>	Electrical Engineering Software
<b>AppBusComp</b>	Applied Business Computer	<b>CMA</b>	Custom MOS Arrays	<b>EESof</b>	EEsof Inc.
<b>AppMicroSys</b>	Applied Microsystems Corp.	<b>CMCInt'l</b>	CMC International	<b>EG&amp;G-Reticon</b>	EG&G-Reticon
<b>AppSys</b>	Applied Systems Corp.	<b>CMD ASIC</b>	CMD ASIC Division	<b>Elantec</b>	Elantec
<b>Aptek</b>	Aptek Microsystems	<b>CMD Micro</b>	CMD Microcircuits Division	<b>Electrologic</b>	Electrologic Inc.
<b>Aptos</b>	Aptos Systems	<b>Codar</b>	Codar Technology Inc.	<b>ElecConServ</b>	Electronics Consulting Service
<b>Argus</b>	Argus Software	<b>Comark</b>	Comark Corp.	<b>Elfab</b>	Elfab Test Systems
<b>ArrayTech</b>	Array Technology	<b>Comlinear</b>	Comlinear Corporation	<b>Elksi</b>	Elksi
<b>ASEA-HAFO</b>	ASEA-HAFO	<b>Commodore</b>	Commodore Semiconductor Group	<b>Emulogic</b>	Emulogic
<b>Astro</b>	AstroSystems Inc.	<b>Compact</b>	Compact Software	<b>ENDOT</b>	ENDOT Inc.
<b>Atec</b>	Atec	<b>CompAuto</b>	Computer Automation	<b>Enterprise</b>	Enterprise Systems
<b>ATITech</b>	ATI Technologies Inc.	<b>CompDyn</b>	Computer Dynamics	<b>ESP</b>	Electronic Software Products
<b>Atlanta</b>	Atlanta Signal Processors	<b>CompModules</b>	Computer Modules Inc.	<b>European</b>	European Silicon Structures
<b>Atmel</b>	Atmel Corp.	<b>Computrol</b>	Computrol Inc.	<b>Exar</b>	Exar Corporation
<b>AT&amp;T</b>	AT&T	<b>CompVision</b>	Computervision	<b>EXEL</b>	EXEL Microelectronics
<b>Augat</b>	Augat, Inc. Systems Div.	<b>ConnMicro</b>	Connecticut MicroComputer	<b>Excelan</b>	Excelan Inc.
<b>AutoDesk</b>	AutoDesk	<b>Contemporary</b>	Contemporary Control Systems		
<b>AutoSys</b>	Automated Systems Inc.	<b>Context</b>	Context Corp.		
		<b>ControlData</b>	Control Data		
		<b>Contrex</b>	Contrex Corp.		
		<b>Conway</b>	Conway	<b>Factron</b>	Factron-EDA
<b>Babcock</b>	Babcock Material Handling Group	<b>CreMicro</b>	Creative Micro Systems	<b>Fairchild</b>	Fairchild
<b>Barvon</b>	Barvon BiCMOS Technolgy Inc.	<b>Crystal</b>	Crystal Semiconductor	<b>Faraday</b>	Faraday
<b>Basicon</b>	Basicon Inc.	<b>CTI</b>	Circuit Technology Inc.	<b>Ferranti</b>	Ferranti Electric
<b>B&amp;C Micro</b>	B&C Microsystems	<b>Cubit</b>	Cubit Inc.	<b>Force</b>	Force Computers
<b>Bedford</b>	Bedford Control Systems Inc.	<b>CustomArrays</b>	Custom Arrays Corp.	<b>Ford</b>	Ford Microelectronics
<b>Berne</b>	Berne Electronics	<b>Cyberchron</b>	Cyberchron Corp.	<b>FujitsuA</b>	Fujitsu America
<b>Bicc-Vero</b>	Bicc-Vero Electronics	<b>Cybernetic</b>	Cybernetic Micro Systems	<b>Fujitsu</b>	Fujitsu Microelectronics, Inc.
<b>BinaryTech</b>	Binary Technology	<b>Cypress</b>	Cypress Semiconductor	<b>FutureNet</b>	FutureNet



<b>GainElec</b>	Gain Electronics	<b>IntCirSys</b>	Integrated Circuit Systems	<b>Micrel</b>	Micrel
<b>Gaill</b>	Gaill Motion Control	<b>IntMeasSys</b>	Integrated Measurement Systems	<b>MicroAide</b>	Micro Aide Corp.
<b>Gateway</b>	Gateway Design Automation	<b>IntSolutions</b>	Integrated Solutions	<b>Microbar</b>	Microbar Systems, Inc.
<b>GE/Intersil</b>	GE/Intersil	<b>IntTech</b>	Integrated Technology	<b>MicroCompSys</b>	Microcomputer Systems
<b>GE/RCA</b>	GE/RCA Solid State	<b>Intech</b>	Intech Advanced Analog	<b>Microcosm</b>	Microcosm
<b>GE Semi</b>	GE Semiconductor	<b>Intel</b>	Intel	<b>MicroDesigns</b>	Microdesigns
<b>GenMicro</b>	General Microsystems	<b>Intelcom</b>	Intelcom Systems Ltd.	<b>MicroIndns</b>	Micro Industries Corp.
<b>Gennum</b>	Gennum Corporation	<b>IntelComp</b>	Intelligent Computer Integration	<b>MicroLinear</b>	Micro Linear
<b>GenRad</b>	GenRad	<b>Interactive</b>	Interactive Circuits and Systems, Ltd.	<b>MicroNet</b>	Micro Networks
<b>GENROCO</b>	GENROCO	<b>Interconics</b>	Interconics	<b>MicroNetech</b>	Micro Net Technology
<b>Gerber</b>	Gerber Scientific Instrument	<b>InterconMicro</b>	Intercontinental Micro Systems	<b>Micropac</b>	Micropac Industries
<b>GigaBit</b>	GigaBit Logic	<b>Interdesign</b>	Interdesign/Ferranti	<b>MicroPwr</b>	Micro Power Systems
<b>GIM</b>	General Instrument Microelectronics	<b>Intergraph</b>	Intergraph	<b>Micro-Link</b>	Micro-Link Corporation
<b>GoldStar</b>	GoldStar Semiconductor	<b>Interphase</b>	Interphase Corp.	<b>Micro-Rel</b>	Micro-Rel
<b>Golden</b>	Golden Electronics	<b>Intronics</b>	Intronics	<b>Microsim</b>	Microsim
<b>Gordos</b>	Gordos Arkansas	<b>Intusoft</b>	Intusoft	<b>MicroSys</b>	Micro/sys
<b>Gould</b>	Gould Inc.	<b>Inventive</b>	Inventive Systems Inc.	<b>Microvoice</b>	Microvoice
<b>GTSys</b>	GT Systems	<b>IoInc</b>	Io Incorporated	<b>Mikros</b>	Mikros Systems Corp.
<b>GW-Three</b>	GW Three Inc.	<b>IPS</b>	Integrated Power Semiconductors	<b>MillerTron</b>	MillerTronics
		<b>Itronics</b>	Itronics Inc.	<b>Miller</b>	Miller Technology
		<b>Isocom</b>	Isocom, Inc.	<b>Mimic</b>	Mimic, Inc.
		<b>ITT</b>	ITT Semiconductors	<b>MiniCompTech</b>	Mini Computer Technology
		<b>IXYS</b>	IXYS Corp.	<b>Minntronics</b>	Minntronics Corp.
				<b>Mitchell</b>	Mitchell Electronics
<b>Harris</b>	Harris Semiconductor	<b>KSystems</b>	K-Systems Inc.	<b>Mitel</b>	Mitel Semiconductor
<b>HEI</b>	HEI Corporation	<b>Kern</b>	Kern Systems	<b>Mitsubishi</b>	Mitsubishi Electronics America, Inc.
<b>Hercules</b>	Hercules Computer Technology	<b>Kontron</b>	Kontron Electronics		
<b>Heurikon</b>	Heurikon Corp.			<b>MMI</b>	Monolithic Memories, Inc.
<b>HHB-Sys</b>	HHB Systems	<b>Lambda</b>	Lambda Semiconductors	<b>Modula</b>	Modula
<b>HiLevel</b>	Hi-Level Technology	<b>Laserpath</b>	Laserpath	<b>MonSys</b>	Monolithic Systems Corp.
<b>Hitachi</b>	Hitachi America, Ltd.	<b>Lattice</b>	Lattice Semiconductor	<b>Morrow</b>	Morrow Technologies
<b>HiTech</b>	HiTech Equipment Corporation	<b>LiitMach</b>	Little Machines, Inc.	<b>Mosaid</b>	Mosaid
<b>Holt</b>	Holt Inc.	<b>LinearTech</b>	Linear Technology Corp.	<b>Motorola</b>	Motorola Semiconductor Products
<b>Honeywell</b>	Honeywell	<b>LMS</b>	LMS Electronics	<b>Multiwire</b>	Multiwire, Div. Kollmorgen
<b>HoneywellISPT</b>	Honeywell Signal Processing Technologies	<b>LogicAuto</b>	Logic Automation	<b>Mylex</b>	Mylex Corp.
		<b>LogicDev</b>	Logic Devices Inc.		
<b>HP</b>	Hewlett-Packard	<b>LogicalDes</b>	Logical Design Group		
<b>Hughes</b>	Hughes Aircraft, Solid State Products	<b>Logiccraft</b>	Logiccraft Inc.	<b>NationalInst</b>	National Instruments
		<b>Lomas</b>	Lomas Data Products, Inc.	<b>National</b>	National Semiconductor
<b>HybridSys</b>	Hybrid Systems	<b>LPKF-Pacific</b>	LPKF-Pacific	<b>NCAI</b>	North Coast Automation, Inc.
<b>HyComp</b>	HyComp	<b>LSIComp</b>	LSI Computer Systems	<b>NCR</b>	NCM Corporation
<b>HYTEK</b>	Hytek Microsystems	<b>LSI Logic</b>	LSI Logic	<b>NEC</b>	NCR Microelectronics
<b>Hyundai</b>	Hyundai Electronics America	<b>LupiData</b>	Lupi Data, Inc.	<b>NMB</b>	NEC Electronics
				<b>NMB</b>	NMB Semiconductor Corporation
<b>IBM</b>	IBM	<b>M2M</b>	M2M Robotics	<b>Northern</b>	Northern Precision Labs
<b>ICC</b>	International Cybernetics	<b>Magnum</b>	Magnum Opus	<b>Novix</b>	Novix
<b>ICDC</b>	Integrated Circuit Design Centre	<b>Marconi</b>	Marconi Electronic Devices Inc.	<b>NthGraphics</b>	Nth Graphics
<b>ICI</b>	Integrated Circuits Inc.	<b>Marinco</b>	Marinco Computer Products	<b>NTI Group</b>	NTI Group
<b>IC Options</b>	IC Options, Inc.	<b>MasterLogic</b>	Master Logic Corporation		
<b>ICSensors</b>	IC Sensors, Inc.	<b>Matra</b>	Matra Design Systems	<b>Octagon</b>	Octagon Systems Corp.
<b>ICT</b>	International CMOS Technology	<b>Matra-Harris</b>	Matra-Harris Semiconductors	<b>Octal</b>	Octal
<b>ICT Comp</b>	ICT Computer Drafting	<b>Matrix</b>	Matrix Corp.	<b>OEI</b>	Optical Electronics Inc.
<b>IDT</b>	Integrated Device Technology	<b>Matrox</b>	Matrox Electronics Systems	<b>OKI</b>	OKI Semiconductor
<b>IKON</b>	Ikon Corp.	<b>Maxim</b>	Maxim Integrated Products	<b>Omaton</b>	Omaton
<b>IKOS</b>	IKOS Systems	<b>MCE</b>	MCE Semiconductor	<b>Omnibyte</b>	Omnibyte Corp.
<b>ILC-DDC</b>	ILC Data Device Corporation	<b>Mentor</b>	Mentor Graphics	<b>Omnicad</b>	OmnCAD
<b>iLSi</b>	Integrated Logic Systems	<b>MTC</b>	Mesa Technology Corp.	<b>Onset</b>	Onset Computer Corp.
<b>IMI</b>	International Microcircuits, Inc.	<b>MetaSoft</b>	Meta Software	<b>Optima</b>	Optima Technology
<b>IMP</b>	International Microelectronic Products	<b>Metatek</b>	Metatek Inc.	<b>Origin</b>	Origin, Inc.
		<b>Micom Int</b>	Micom-Interlan	<b>Orion</b>	Orion Instruments
		<b>Micra</b>	Micra Corp.	<b>OwlComp</b>	Owl Computers
<b>Imaging</b>	Imaging Technology Inc.				
<b>IndComp</b>	Industrial Computer Designs				
<b>IndTech</b>	IndTech Inc.				
<b>Inmos</b>	Inmos Corporation				
<b>InnovRes</b>	Innovative Research				
<b>Inova</b>	Inova Microelectronics				
<b>InrVision</b>	Inner Vision				



## CONT.

PacificM Pacific Panasonic Panatech PC-Office PCAD PEP-Modular Performance PlesseyMicro Plessey	Pacific Microcomputers, Inc. Pacific Microcircuits Panasonic Panatech Semiconductor PC-Office PCAD PEP Modular Computers Performance Semiconductor Corp. Plessey Microsystems Plessey Semiconductors	Siliconix Siltronics Silvaco SilvarLisco Simucad Simulog SingleBoard Slicer SMC	Siliconix Siltronics Silvaco Data Systems Silvar Lisco Simucad Simulog Single Board Solutions Slicer Computers Inc. Standard Microsystems Corporation Scientific Microsystems Softwestern Company, Great Solarcom Technology Inc. Solarise Enterprises Inc. Solitron Devices Sony Corporation of America Sophia Computer Systems Space Research Technology, Inc. Spectrum Software Sprague Electric Company Solid State Micro Technology for Music	Trimarchi Trimeter	Trimarchi and Associates Trimeter Technologies
PLXTechnology PMI Polycore Praxis Pro-Log Proximity	PLX Technology Precision Monolithics Inc. Polycore Electronics Praxis Systems Pro-Log Corp. Proximity	SMS Softwestern Solarcom Solarise Solitron Sony Sophia SpaceResearch Spectrum Sprague SSM	Scientific Microsystems Softwestern Company, Great Solarcom Technology Inc. Solarise Enterprises Inc. Solitron Devices Sony Corporation of America Sophia Computer Systems Space Research Technology, Inc. Spectrum Software Sprague Electric Company Solid State Micro Technology for Music Stantel-STC STD Microsystems Stanford Telecommunications Stynetic Systems Sunshine Semiconductor Supertex Inc. Synergy Microsystems Syscon Corp. Systech Systek Systems Calculations Systems Datar	UMC Unicorn Unitrode Universal United USDesign UTMC	United Microelectronics (UMC) Unicorn Microelectronics Unitrode Universal Semiconductor, Inc. United Silicon Structures US Design Corp. United Technologies Microelectronics Center
Quadtree Qualogy Quantic	Quadtree Qualogy Corporation Quantic Laboratories, Inc.	Stantel-STC STD STI Stynetic Sunshine Supertex Synergy Syscon Systech Systek SysCalc SysDatar	STantel-STC STD Microsystems Stanford Telecommunications Stynetic Systems Sunshine Semiconductor Supertex Inc. Synergy Microsystems Syscon Corp. Systech Systek Systems Calculations Systems Datar TL Industries Inc. TL SI, Inc. TRW LSI Products Tangent Systems Corp. Tatum Labs Technitrol Techno Inc. Technology 80 Technology Modeling Tektronix Tektronix/CAE Systems Tektronix/Integrated Circuit Operations Teledyne Crystallonics Teledyne Philbrick Teledyne Semiconductor Telefunken Teletek Enterprises Teltone Corporation Teradyne Texas Instruments The Destek Group Third Domain Thomson Components-Mostek Titan/SESCO Toko America Topaz Semiconductor Toshiba America Transmag TriQuint	Valid Validyne VAMP VDA Vectron VersaLogic Vesta VIA-Systems ViewLogic Visionics VisionsUnlim Vitelc Vitesse VLSI Tech VME-Microsys VMI Votrax VTC Vutek	Valid Systems Validyne Engineering VAMP VLSI Design Associates Vectron Graphics Systems Versalagic Corp. Vesta Technology VIA Systems View Logic Systems Visionics Visions Un-limited Vitelc Corp. Vitesse Electronics VLSI Technology (San Jose) VME Microsystems Int'l Corp. VLSI Microsystems, Inc. Votrax VTC Vutek Systems, Inc.
RACAL RanchoTech RapidSys Raytheon RCIData Recognition RELMS Renaissance Ricoh RIFA RLCEnterprise Robotrol Rockwell RTC	RACAL-REDAC Rancho Technology Rapid Systems, Inc. Raytheon Semiconductor RCI Data Recognition Technology Relational Memory Systems Renaissance GRX Ricoh Company Ltd. RIFA R.L.C. Enterprises Robotrol Corp. Rockwell Semiconductor Products Riehl Time Corporation	TL Industries TL SI TRW-LSI Tangent Tatum Technitrol Techno Tech80 TechModl Tektronix Tek/CAE Tek/ICO	TL Industries Inc. TL SI, Inc. TRW LSI Products Tangent Systems Corp. Tatum Labs Technitrol Techno Inc. Technology 80 Technology Modeling Tektronix Tektronix/CAE Systems Tektronix/Integrated Circuit Operations Teledyne Crystallonics Teledyne Philbrick Teledyne Semiconductor Telefunken Teletek Enterprises Teltone Corporation Teradyne Texas Instruments The Destek Group Third Domain Thomson Components-Mostek Titan/SESCO Toko America Topaz Semiconductor Toshiba America Transmag TriQuint	Waferscale WDC Webster Weitek Western WinSystems Wintek	Waferscale Integration Inc. Western Design Center Webster Computer Co. Weitek Corporation Western Digital WinSystems Inc. Wintek Corp.
S-MOS Samsung Sanyo SBE SDA-Systems SciCalc SDA-Systems SeattleSi SEEQ Semicon Sensoray SerialLab Sertek SGS SharedRes Sharp Siemens Sierra Sigma Info Signetics SiCompilers SiControls SiliconG SiliconSys	S MOS Systems Samsung Semiconductor Sanyo Semiconductor SBE, Inc. SDA Systems Scientific Calculations SDA Systems Seattle Silicon Tech. SEEQ Technology, Inc. Semicon, Inc. Sensoray Co. Serial Lab Products Inc. Sertek Inc. SGS Semiconductor Shared Resources Sharp Siemens Sierra Semiconductor Sigma Information Systems Signetics Silicon Compilers Silicon Controls Silicon General Silicon Systems Inc.	TeledyneC TeledyneP TeledyneS Telefunken Teletek Teltone Teradyne TI Destek ThirdDomain Thomson Titan/SESCO Toko TopazSemi Toshiba Transmag TriQuint	Teledyne Crystallonics Teledyne Philbrick Teledyne Semiconductor Telefunken Teletek Enterprises Teltone Corporation Teradyne Texas Instruments The Destek Group Third Domain Thomson Components-Mostek Titan/SESCO Toko America Topaz Semiconductor Toshiba America Transmag TriQuint	XCAT Xerox Xicor Xilinx Xycom Xylogics	XCAT Xerox Xicor Xilinx Xycom Xylogics, Inc.
				ZAX Zapco Zecom Zendex Ziatech Zilog Zitek Zitel Microcosm Zuken ZyMOS	ZAX Corp. Zeff Advanced Product Co. Zecom Inc. Zendex Corp. Ziatech Corporation Zilog Zitek Corp. Zitel Zuckerboard Zuken America ZyMOS



# INTRODUCTION TO ASIC/CUSTOM CIRCUITS

This section describes ASIC/Custom products and services. It shows interrelationships, covering the devices and manufacturers' capabilities as well as the design tools for use by OEM engineers and system designers. The first guide lists custom capabilities. The subsequent guides cover devices and the specific tools that can be applied.

For more detailed information on devices and tools you can review the manufacturer-supplied technical data. In the case of tools you can also refer to the Design Automation Master Selection Guide.

Category	
Capabilities Charts	4010
Gate Arrays	4041
Linear and Linear/Digital	
Arrays	4065
Programmable Logic	4070
Standard Cells	4082
Gate Array Design	
Automation Tools	4088
Linear and Linear/Digital	
Design Automation Tools	4092
Programmable Logic Design	
Automation Tools	4093
Standard Cell Design	
Automation Tools	4094
VLSI/LSI Macrocell Libraries	4097



## CUSTOM/SEMICUSTOM

Manufacturer	Advanced Linear Devices	Advanced Micro Devices	Alphatron
FOR DETAILED DATA SEE:		(Page 4201)	
Customized Standard Circuits	Linear, combined linear/digital		
Gate Array		Programmable Array Logic	
Chip Density Range (equiv. gates)		200 to 800	Up to 4400 2-input gates
Cell Library	CMOS	CMOS	
Design Kit Available		Yes	Yes
Full Custom Circuits Digital			Silicon- or metal-gate PMOS, NMOS, CMOS
Linear	Silicon-gate CMOS		Silicon- or metal-gate PMOS, NMOS, CMOS
Combined Digital Linear	Silicon-gate CMOS		Silicon- or metal-gate PMOS, NMOS, CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Circuit diagram, block diagram, circuit inputs and outputs		Alphamap layout logic diagram, functional description block diagram
Design Aids		AMPALASM-20 software for Boolean equation generation. AMPLPL software provides similar capability for advanced products.	Logic simulation, breadboard assistance, design rule checks, decals
Production	Procured and in-house	In-house	Wafer production procured from outside foundries. Testing done in-house
Preferred Delivered Product		Ceramic and plastic DIPs, leadless chip carriers, dice; all available in commercial and military	Any upon request
Test Program Generation	Yes		Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental	100% dc, ac and functional testing; burn-in, thermal shock, environmental, MIL	Functional, parametric, burn-in, thermal shock, environmental, MIL
Electrical Test Systems Available	Industry standard and custom test systems	Xincom, Accutest	In-house designed, customer supplied, or outside service
Comments	Supply voltage range: 1V to 12V	Commercial programmers available. Software output JEDEC PLDTF. Most complex programmable logic parts available.	Multiple sourcing; cell library and design rule handbook



**CUSTOM/SEMICUSTOM (cont.)**

Manufacturer	Applied Micro Circuits	Aptek Microsystems	Array Technology
<b>FOR DETAILED DATA SEE:</b>			
Customized Standard Circuits		Digital/analog	Digital
Gate Array	ECL, TTL, mixed, and silicon-gate CMOS		Silicon-gate CMOS
Chip Density Range (equiv. gates)	250 to 9,300 gates		150 to 3,300
Cell Library	ECL, TTL, mixed, and silicon-gate CMOS	Si-gate CMOS	CMOS
Design Kit Available	Yes		No
<b>Full Custom Circuits</b> Digital	ECL, TTL, mixed silicon-gate CMOS	Silicon-gate CMOS, metal-gate CMOS, NMOS, bipolar TTL, I <sup>2</sup> L	Silicon-gate CMOS
Linear		CMOS, switched capacitor filters	Limited
Combined Digital Linear		CMOS, switched capacitor filters	Limited
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Netlist and simulation vectors, functional specification and test vectors	Functional specification, logic diagram, circuit diagram, breadboard	Logic diagram, circuit diagram, test vectors, functional specification
<b>Design Aids</b>	MacroMatrix software design kits for Daisy, Mentor, Tegas, Tektronix/CAE Systems and Valid. Includes symbol and logic libraries, engineering rule checks, delay annotation software, pattern test formatter.	Logic and device simulation, CAD, CAE, design rule checks	Design rule checks, logic simulation, circuit simulation
<b>Production</b>	In-house	Procured	Procured
<b>Preferred Delivered Product</b>	Packaged devices, dice	Packaged devices	Packaged units
<b>Test Program Generation</b>	Yes	Yes	Yes
<b>Production Test</b>	Functional, parametric, ac, burn-in, thermal shock, environmental, MIL-STD-883	Functional, parametric	Functional, parametric, burn-in
<b>Electrical Test Systems Available</b>	Sentry X, Sentry XXI, and Trillium Array Matrix		Sentry
<b>Comments</b>	Mixed I/O (ECL/TTL) capability; plus Si-gate CMOS; ECL 10K and 100K or both capability; MSI and custom macros available; second sourced; military screening available on all arrays	Independent design center, multiple source compatibility, specialize in CMOS Analog	Linear includes data separator



# IC MASTER

## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	ASEA-HAFO	AT&T	Barvon Research
FOR DETAILED DATA SEE:		(Page 4207)	
Customized Standard Circuits	Digital, combined digital/linear		Digital, combined digital/linear
Gate Array			2.5 $\mu$ silicon-gate CMOS, Bi-CMOS (bipolar and CMOS)
Chip Density Range (equiv. gates)	Up to 10,000 gates		100 to 10,000 2-input gates
Cell Library	Metal- or silicon-gate CMOS, silicon-gate CMOS/SOS		CMOS, BiCMOS
Design Kit Available			Yes
Full Custom Circuits Digital	Silicon-gate CMOS, metal-gate CMOS, silicon-gate CMOS/SOS (radiation hardened)		Silicon-gate CMOS, HCMOS, HMOS, BiCMOS
Linear	Silicon-gate CMOS, metal-gate CMOS, silicon-gate CMOS/SOS (radiation hardened)	Complementary bipolar, CMOS, bipolar (dielectric isolation)	Silicon-gate CMOS, HCMOS, BiCMOS
Combined Digital Linear	Silicon-gate CMOS, metal-gate CMOS, silicon-gate CMOS/SOS (radiation hardened)	I <sup>2</sup> L, bipolar/MOS (dielectric isolation), CMOS	Silicon-gate CMOS, HCMOS, BiCMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Verified netlist, test vectors, logic diagram, circuit diagram, PG tape, black box.	Functional diagram, schematic, specification, breadboard.	Logic diagram, circuit diagram, breadboard, functional specification, test vectors, COT, known good device
Design Aids	Schematic entry, circuit simulation, design rule checks, test program generation.	CAD assistance, linear simulation, engineering and breadboard assistance	Circuit simulation, logic simulation, schematic entry, test program generation, design rule checks, breadboard assistance
Production	In-house	In-house	In-house, procured
Preferred Delivered Product	Wafers, dice packaged test units	Probed wafers or packaged dice	Packaged devices, others available
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, MIL: burn-in, environmental	Functional, parametric, burn-in, environmental	Functional, parametric, burn-in, thermal shock, environmental, MIL
Electrical Test Systems Available	LTX, Sentry VII, Teradyne VLSI Tester.	LTX, AT&T Stetzler (bipolar)	Sentry, Teradyne
Comments	Standard cell libraries for various workstations, quality level to MIL 883C Level S	Wafer fabrication services, products include 30 and 90 volt linear arrays, microwave arrays.	Complete custom capability including design, instruction, CAD and technology licensing. Standard cell library available.



**CUSTOM/SEMICUSTOM (cont.)**

Manufacturer	California Devices	Cherry Semiconductor	Circuit Technology Inc.
<b>FOR DETAILED DATA SEE:</b>			
Customized Standard Circuits	Digital	Digital, linear, combined digital/linear	Digital
Gate Array	Silicon- or metal-gate CMOS	P <sup>2</sup> L, LSI <sup>2</sup> L, ECL and other bipolar	Silicon gate CMOS, CMOS on sapphire
Chip Density Range (equiv. gates)	200 to 20,000 2-input gates	64 to 150 gates/mm <sup>2</sup>	560 to 1440 for 5 micron single-metal; 1120 to 3876 for 4 micron double metal
Cell Library	CMOS	P <sup>2</sup> L, LSI <sup>2</sup> L, ECL and other bipolar	CMOS and LSTTL
Design Kit Available	Yes	Yes	Yes plus CAD
Full Custom Circuits Digital		P <sup>2</sup> L, LSI <sup>2</sup> L, ECL and other bipolar	Silicon gate CMOS, CMOS on Sapphire
Linear		P <sup>2</sup> L, LSI <sup>2</sup> L, ECL and other bipolar	
Combined Digital Linear		P <sup>2</sup> L, LSI <sup>2</sup> L, ECL and other bipolar	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Simulated netlist from CAE workstation, logic diagram, customer-owned tooling	Customer-owned tooling, circuit diagram, logic diagram, breadboard	Logic diagram and test vectors, customer-owned tooling, functional specification
Design Aids	Wise I, Wise II complete software for electrical and physical design	Logic simulation, breadboard assistance, design rule checks	Logic simulation, auto layout, rules checks, network comparison checks
Production	In-house	In-house	In-house plus second sourcing availability
Preferred Delivered Product	Scribed dice, packaged dice, substrate-mounted device	Packaged dice, flip chips	All options available
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL	All except military	Full capability including full MIL, class S and geothermal (200°C)
Electrical Test Systems Available	Sentry VII, Sentry Series 20	Teradyne 1259, A310, A311	Fairchild Series 10
Comments	Channelless architecture. Si-gate isolated oxide CMOS has TTL/LSTTL interfacing capability, high-speed performance. Output drivers 32mA.	Dice can be solder-bump flip chips with nitride passivation; packaged dice can be delivered from COT for full custom.	No limit on package variety, in-house multichip hybrid capability



## IC MASTER

## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Cirrus	Comlinear Corporation	Custom Integrated Circuits
FOR DETAILED DATA SEE:			
Customized Standard Circuits	VLSI custom microprocessor peripherals	Yes	Digital, linear, combined digital/linear
Gate Array			I <sup>2</sup> L, Linear Master Slice, design on other companies' gate arrays
Chip Density Range (equiv. gates)	5,000 to 40,000		50 to 8,000 (5-input gates)
Cell Library			CMOS, I <sup>2</sup> L
Design Kit Available			
Full Custom Circuits Digital	Compiled custom NMOS, CMOS		CMOS, TTL, I <sup>2</sup> L, and other bipolar devices
Linear			Bipolar, CMOS
Combined Digital Linear			CMOS/linear; bipolar/linear
Provide Design Assistance	Yes, full turnkey	Yes	Yes
Acceptable Customer Input (in order of preference)	System description, state diagram, functional specification	Functional specification	No preference
Design Aids	Proprietary silicon compiler; terminal input of register transfer logic description (RTL); functional simulation S/LA with detailed logic and timing simulation; automatic layout from S/LA	Computer simulation	Logic simulation, circuit simulation, design rule checks, breadboarding, complete Calma layout system, in-house CAD software, engineering assistance
Production	Manufacturing alliances	In-house or procured	Procured
Preferred Delivered Product	Packaged, tested parts	Packaged circuit, printed card mounted units, hybrid circuits	No Preference
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, environmental, MIL-STD 883	Functional, burn-in, thermal shock, linear, MIL	All
Electrical Test Systems Available	Sentry	Complete time domain and frequency domain testing from dc to 18 GHz	HP, MCC
Comments	Applications and product engineering support; full turnkey design and manufacture; alternate source for wafer fabrication; Over 100,000 transistor complexity	Specialties include amplifiers with extremely wide bandwidth and fast settling time, fast sample-hold and A/D conversion products.	Total IC development from concept through product delivery; any subset of the development cycle (design, layout, etc.)



**CUSTOM/SEMICUSTOM (cont.)**

Manufacturer	Custom MOS Arrays	ECI Semiconductor	Exar Corporation
FOR DETAILED DATA SEE:			(Page 4222)
Customized Standard Circuits	Digital	Digital, digital/linear	Digital, linear, combined digital/linear
Gate Array		3 $\mu$ silicon-gate CMOS, ECI bipolar, BiCMOS	Metal-gate CMOS, I <sup>2</sup> L, Si-gate CMOS
Chip Density Range (equiv. gates)	448 to 1,568	100 to 2,500	100 to 1,250
Cell Library	Yes	BiCMOS, ECI bipolar	I <sup>2</sup> L, Si-gate CMOS, linear bipolar
Design Kit Available			Yes
Full Custom Circuits Digital		BiCMOS, bipolar, CMOS	Metal-gate CMOS, I <sup>2</sup> L, Si-gate CMOS
Linear		BiCMOS, bipolar, CMOS	Bipolar, CMOS
Combined Digital Linear		Bipolar, BiCMOS	I <sup>2</sup> L, other bipolar
Provide Design Assistance			Yes
Acceptable Customer Input (in order of preference)		Logic diagram, circuit schematic, functional specification, database tapes, PG tapes, tooling	Database tapes, complete layout, breadboard, circuit diagram, logic diagram, functional diagram
Design Aids		Logic simulation, design rule checks, netlist verification, test verification	Logic simulation, breadboard assistance, design rule checks, cell libraries, design manual; schematic capture, simulation, layout on IBM PC/AT
Production		In-house	In-house
Preferred Delivered Product		1. Packaged parts, 2. tested dice, 3. wafers	Packaged devices, dice, dice in wafer form, wafers
Test Program Generation		Yes	Yes
Production Test		Functional, parametric, environmental, burn-in	Functional, parametric, environmental, burn-in
Electrical Test Systems Available		Sentry VII, Fairchild 5000	Fairchild 5000, Teradyne J273, A311, A312, A360, A360D, A370, Sentry 10, 20, EPRO 140, EPRO 210 and 8832 Loadstar
Comments		BiCMOS "Smart Power" and ECI type 3GHz+ bipolar standard cells are major strengths.	



**CUSTOM/SEMICUSTOM (cont.)**

Manufacturer	Fairchild	Fujitsu Microelectronics, Inc.	Gain Electronics
FOR DETAILED DATA SEE:		(Page 4229)	
Customized Standard Circuits	Digital	Digital	Digital
Gate Array	ECL, 2 $\mu$ silicon-gate CMOS	Silicon-gate CMOS, LSTTL, ECL, BiCMOS	Gallium Arsenide
Chip Density Range (equiv. gates)	ECL: 500 to 2,000 3-input NAND; CMOS: 500 to 6,000 2-input NAND	200 to 20,000	1,700; 3,500; & 6,000
Cell Library	Yes	Silicon-gate CMOS, LSTTL, ECL, 7400/4000 + memory.	GFL- Gain FET Logic (see comments)
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits			
Digital	Implemented in gate array format; ECL or 2 $\mu$ CMOS	Silicon-gate CMOS, LSTTL, ECL	ECL, TTL, and CMOS compatible
Linear		Silicon-gate CMOS, LSTTL	
Combined Digital Linear		Silicon-gate CMOS	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram to PG tape - depending on customer interface required	Logic data and test timing data (Fujitsu format); Tegas netlist, schematic and test vectors	Logic diagram, circuit diagram, test vectors, functional specifications
Design Aids	Logic simulation, breadboard assistance, design rule checks. FairCAD design system provides full design capability.	Logic simulation, design rule checks, complete CAD system; software and libraries for Daisy, Mentor, Valid, and FurureNet workstations	Schematic capture, design rule checks, logic and timing simulations, automatic placement and routing, circuit simulation, post layout annotation, physical rule checking, and test vector generation
Production	In-house	In-house	In-house
Preferred Delivered Product	Packaged die preferred	Packaged dice	Scribed dice, packaged dice, substrate-mounted device
Test Program Generation	Yes	Automatic	Yes
Production Test	Functional parametric to MIL 883B	Functional, ac and dc parametric	Parametric, wafer sorting based on low speed functional test, high speed test at temperature extremes
Electrical Test Systems Available	In-house	In-house	Kiethley 450, Advantest 3320
Comments	High performance ECL and 2 $\mu$ silicon-gate CMOS gate arrays in volume production	Dual- and Triple-layer metal; CAD system verifies designs; auto placement and routing from customer's inputs; guaranteed 90% gate utilization	GFL is a digital logic structure with the following features: high noise margin, high speed, flexibility in implementation of complex logic functions, and low power dissipation.



**CUSTOM/SEMICUSTOM (cont.)**

Manufacturer	GE Solid State (GE/RCA)	GigaBit Logic	Gennum Corporation
FOR DETAILED DATA SEE:	(Page 4235)	(Page 4240)	(Page 4239)
Customized Standard Circuits	Digital, linear/digital	Digital GaAs	Linear and combined digital/linear
Gate Array	Silicon-gate CMOS		Bipolar
Chip Density Range (equiv. gates)	640 to 50,000	50 to 5,000	Linear bipolar 100-479
Cell Library	CMOS	SC1 (D-Mode), SC2 (HME/D)	Common circuit block and micro cells
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	Silicon-gate CMOS	Depletion Mode (D-mode) GaAs MESFET; High Margin Enhancement/Depletion Mode (HME/D)	I <sup>2</sup> L, RTL
Linear	CMOS		Bipolar
Combined Digital Linear	CMOS	Yes	TL, I <sup>2</sup> L, some linear functions
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, circuit diagram, breadboard test vectors, customer-owned-tooling (pattern generator tape, composite drawing), known good device	Calma GDSII tape, cell library schematic, block diagram	Pencil connected layout, logic diagram spec, PG tape, circuit diagram and breadboard, reticles
Design Aids	Logic simulation, breadboard assistance, design rule checks	Comprehensive design rules and manuals; ERC, DRC, LVS, SPICE simulation, logic simulation, cell libraries, prototype tools	Design rule checks, CAD, circuit simulation, design manual, breadboard parts, layout sheets, seminar
Production	In-house	In-house	In-house
Preferred Delivered Product	Probed wafers, scribed dice, packaged dice	Wafers, die, or packaged units	Packaged dice, bare dice, probed wafers
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in	Functional ( 10 MHz ), high speed ( 3GHz )	Functional, parametric, environmental
Electrical Test Systems Available	Teradyne, Sentry 7, Sentry 21, J273, J193, J283, J325, LTX, MTS 77	MegaTest, IMS, custom high speed	Industry standard tester, custom tester
Comments	SOS radiation hardened	All customer-interface levels supported. Guaranteed high speed performance to customer specifications.	Complete in-house services; design layout, PG, masking, wafer fabrication, assembly, test, Q.A.



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Gould Inc.	GTE/CMD ASIC	Harris Semiconductor
FOR DETAILED DATA SEE:	(Page 4244)	(Page 4214)	(Page 4246)
<b>Customized Standard Circuits</b>	Digital, linear, combined digital/linear		Digital, linear, combined digital/linear
Gate Array	2 $\mu$ and 3 $\mu$ silicon-gate CMOS	ADV-CMOS	3 $\mu$ silicon-gate CMOS
Chip Density Range (equiv. gates)	1000 to 10K 2-input gates (gate array), to 15,000 (standard cell)	504 to 3,000	Up to 10,000 (CMOS) (Rad Hard); Up to 2,500 (TTL-AS); 120, 312 and 918, (TTL-ALS) (Rad Hard)
Cell Library	Yes	ADV-CMOS	2.5 $\mu$ silicon-gate CMOS; DLM silicon-gate CMOS
Design Kit Available	Daisy, Mentor, Gould AMI, P-CAD, FutureNet	Yes	Daisy, Mentor, Harris SDA
<b>Full Custom Circuits</b>			
Digital	Silicon-gate CMOS with high-voltage output capability, up to 60V	ADV-CMOS	Metal-gate and silicon-gate CMOS; silicon-gate PMOS, LSTTL, ALSTTL, STTL, N <sup>2</sup> L
Linear	Silicon-gate CMOS, filter, amplifier to rf	ADV-CMOS	Bipolar (dielectric isolation); metal-gate CMOS/bipolar; silicon-gate CMOS
Combined Digital Linear	Silicon-gate NMOS, CMOS, 14-bit resolution, VHF-rf	ADV-CMOS	Silicon-gate CMOS; bipolar
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Layout database, PG tape, validated netlist, semi-validated netlist, functionally validated netlist, unvalidated netlist, logic diagram, functional specifications, masks	Netlist, Calma tapes, PG tapes, masks, logic diagrams	Logic diagram, logic database, Calma masks; database
<b>Design Aids</b>	CAD assistance, training manuals	Design rule checks, logic simulation	Proven cell library macros, logic simulation, layout programs and test grading, parasitic extraction, logic to layout verification
<b>Production</b>	In-house	In-house	In-house
<b>Preferred Delivered Product</b>	DIP, plastic chip carriers, SOIC packages, wafers, die to commercial or military specifications	Packaged die, probed wafers, mapped wafers	Wafer, packaged dice, scribed dice, and packaged devices
<b>Test Program Generation</b>	Yes, CAD-supported	Yes	Yes
<b>Production Test</b>	Functional, parametric, burn-in, thermal shock, environmental, MIL	Functional, parametric, burn-in	Up to and including equivalent class "S" military flow; also in-house total dose testing
<b>Electrical Test Systems Available</b>	Sentry, Teradyne, Xicom, LTX, General Radio	Sentry, LTX	Sentry
<b>Comments</b>	Complete custom capability including design, instruction, cell library licensing; CAD also available at Design Centers		Also offer low voltage CMOS; radiation hardening for most process technologies; also provides silicon foundry



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Holt Integrated Circuits, Inc.	Honeywell	IC Options, Inc.
FOR DETAILED DATA SEE:	(Page 4253)		
Customized Standard Circuits	Linear, digital, combined linear/digital		Digital/analog
Gate Array	Metal-gate CMOS, silicon-gate CMOS	HGT5000, ALS; HGE200, ECL; HGM1000, ALS/ECL	Not available
Chip Density Range (equiv. gates)		5000- ALS; 2000- ECL; 1000- ALS/ECL	100 to 10,000
Cell Library	Metal gate CMOS, silicon-gate CMOS, EPIC	75 functions	CMOS, 1.5 micron
Design Kit Available	Yes, PDS, Silvar-Lisco	Yes	No
Full Custom Circuits Digital	Silicon-gate, metal-gate CMOS	NMOS, CMOS, ECL	No
Linear	Silicon-gate, metal-gate CMOS		No
Combined Digital Linear	Metal-gate CMOS, silicon-gate CMOS	Yes	No
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Netlist, Calma tapes, logic diagram, chip, schematic, logic data base	Engineering workstation database; logic specification and simulation; circuit documentation	Logic diagram, functional specification, netlist
Design Aids	Logic simulation, breadboard assistance, DRC, ERC, sample cells in packages, silicon breadboard chip.	Computer-aided design package	CAD/CAE: schematic entry, simulation, place and route, verifications, verified cell and macroblock library, module generation
Production	In-house with second source	In-house	Multisourced procurement
Preferred Delivered Product	Packaged devices, probed die	Choice of package	Fully tested packaged parts, or scribed die
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL, SEM, Class "S"	Functional, 100% dc, and 100% ac	Functional, parametric, burn-in, MIL STD-883C
Electrical Test Systems Available	Eagle LSI-4, plus IEEE-488, Analog Instrumentation, IT-200, Custom Testers/IBM based	Fairchild Sentry VIII and Series 20	Sentry
Comments	Specialize in high voltage/low power CMOS and integrated analog/digital custom circuits		Design assistance offered through affiliated design companies and consultants in customers local area



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	ILC Data Device Corporation	iLSi (Integrated Logic Systems, Inc.)	Integrated Circuit Design Centre
FOR DETAILED DATA SEE:			
Customized Standard Circuits	Digital, linear, power		Digital
Gate Array		2 micron CMOS double metal, 1.5 micron ECL double metal.	Silicon gate CMOS
Chip Density Range (equiv. gates)		CMOS 800-15,000, ECL 500-5,000	560 to 1,440- 5 $\mu$ single metal; 1,120 to 3,800- 3 $\mu$ double metal
Cell Library		Full 7400 series, user definable ROM, RAM, PLA in standard cell density; 2900 family; all of above in CMOS or ECL .	150 cell generic library and 150 macrocells
Design Kit Available		Daisy, Mentor, PC, MicroVAX II	PCAD library disks available
Full Custom Circuits Digital	Bipolar, CMOS		Silicon-gate CMOS
Linear	Bipolar		Silicon-gate CMOS, 10 functions
Combined Digital Linear	Bipolar, CMOS		Silicon-gate CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, circuit diagram, test vectors, functional specifications	Simulated schematic or functional description	HILO/PCAD/Silvar-Lisco netlist plus verified test vectors
Design Aids		Schematic capture, logic simulation, automated R-C extraction, timing verification, design rule checking, electrical rule checking, auto place and route, customer training, design center	Schematic creation, logic simulation, fault coverage, auto layout, re-simulation from layout
Production	In-house	In-house and procured wafer production	AMES plus second sourcing
Preferred Delivered Product	Packaged units	Packaged dice available in commercial and military	Tested chips and packaged parts
Test Program Generation	Yes	100% automated test program generation	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL	98% fault coverage typical, 100% dc/ac and functional testing; burn-in military reliability	All
Electrical Test Systems Available	Custom equipment	Sentry VIII, Sentry XX, Sentry XXI, Genrad 16, 18	Fairchild Sentinel, Sentry, and LTX
Comments	New packaging technology and materials enable DDC to develop power hybrids with typical power dissipation of 100 watts, and are capable of handling typical currents of 50 amperes with low junction-to-case thermal resistance.	Gate array architecture offering complex functions with standard cell density; full scan path test program generation and fault grading; available in commercial and military	All parts including first samples tested fully to customer's test pattern.



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Integrated Circuit Systems	Integrated Power Semiconductors	Integrated Technology Inc.
FOR DETAILED DATA SEE:	(Page 4256)		
Customized Standard Circuits	Digital, linear, combined digital/linear		
Gate Array	CMOS		
Chip Density Range (equiv. gates)	20,000		
Cell Library	Metal-gate CMOS, Silicon-gate CMOS		
Design Kit Available	No		
Full Custom Circuits Digital	CMOS/SOS, CMOS, GaAs, NMOS, Si- or metal-gate, double level metal, double level poly	Yes	Silicon- or metal-gate CMOS, NMOS, STTL, LSTTL, I <sup>2</sup> L, ECL, other bipolar
Linear	CMOS	Yes	Silicon- or metal-gate CMOS, bipolar
Combined Digital Linear	CMOS	Yes	Silicon- or metal-gate CMOS, bipolar
Provide Design Assistance	Yes	Yes	
Acceptable Customer Input (in order of preference)	No minimum required	Working plates, pattern generation tapes, breadboard, schematic diagram, functional specification	
Design Aids	DRC and ERC on VAX 11/780, Calma GDS II sticks software, production test systems, Mentor and Daisy workstations	Daisy Chipmaster	Logic simulation, breadboard assistance, design rule checks, transient analysis
Production	Yes	In-house	Procured
Preferred Delivered Product	Packaged parts	Probed wafers, dice, packaged units	Mapped wafers, probed wafers, packaged dice, PC mounted packaged units, design tooling, complete systems
Test Program Generation	Yes	Yes	Yes
Production Test	Yes	Parametric die sort with trim capability, hot, cold, room temp.	Functional, parametric
Electrical Test Systems Available	Megatest, Sentry	LTX	Siemens
Comments	Services: design, layout, chip/PCB artwork, test generation, product engineering, test and production	100% burn-in, Mil spec manufacturing line	Services: design, tooling for custom ICs; service industry used for photomasks, wafer fab, assembly, some testing; system design and production with custom ICs



## IC MASTER

## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Interdesign/Ferranti	International Microcircuits, Inc.	International Microelectronic Products
FOR DETAILED DATA SEE:			
Customized Standard Circuits	Digital, linear, combined digital/linear	Digital	Digital, combined linear/digital
Gate Array	Metal-gate and silicon-gate CMOS, bipolar digital and linear	Silicon- or metal-gate CMOS	No
Chip Density Range (equiv. gates)	See comments	75 to 7,500	200 to 10,000
Cell Library	Yes	Yes	Silicon-gate CMOS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	Silicon-gate CMOS, metal-gate CMOS, CDI bipolar, linear bipolar, linear CMOS.		Silicon-gate NMOS and CMOS
Linear	Bipolar, CMOS		
Combined Digital Linear	Bipolar, CMOS		Silicon-gate NMOS and CMOS
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Pencil-connected layout, logic diagram, specification, PG tapes, circuit diagram and breadboard (for linear bipolar)		Functional specification, logic diagram, circuit diagram, breadboard, test vectors, customer-owned tooling (pattern-generator tape, composite drawing), known good device
Design Aids	Logic/circuit computer simulation, breadboard parts, layout sheets, functional overlays, evaluation parts		Logic simulation, breadboard assistance, design rule checks, engineering assistance
Production	Part processed wafers procured, other functions in-house	In-house and procured	In-house
Preferred Delivered Product	Packaged dice, bare dice, probed wafers	Scribed dice, packaged dice	Mapped wafers, probed wafers, scribed dice, packaged dice, or special packages.
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, MIL 883B, environmental	Functional, parametric, burn-in, thermal shock, environmental, MIL	Functional, parametric, burn-in
Electrical Test Systems Available	Teradyne J325, LTX CP/TS70, LOMAC LM325, Fairchild 5000, LTX DX90, Pragmatic Inspector 100	Genrad, Sentry	Sentry 20, Kiethley
Comments	Linear bipolar 100-276 components; analog CMOS 100 gates & 732 components; digital CMOS 70-1,500 gates; digital bipolar 100-4,000 gates; analog/digital bipolar to 575 gates & 1,305 components		



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Lattice Semiconductor	LSI Computer Systems	LSI Logic
FOR DETAILED DATA SEE:		(Page 4267)	(Page 4268)
Customized Standard Circuits			Digital
Gate Array	E <sup>2</sup> programmable logic GAL and RAL versions		Silicon-gate HCMOS
Chip Density Range (equiv. gates)	300 to 500 gates		300 to 50,000
Cell Library			7400/4000 CMOS and HCMOS, 500 cells includes 2900 series, 8200, 6800, multipliers, adders, DSP cells, etc.
Design Kit Available	Yes		3-day class
Full Custom Circuits Digital		Metal-gate PMOS, CMOS, silicon-gate NMOS, silicon gate CMOS	
Linear		Metal-gate PMOS, CMOS, silicon-gate CMOS	
Combined Digital Linear		Metal-gate PMOS, CMOS, Silicon-gate CMOS	
Provide Design Assistance	Yes	Yes	Over 20 LSI design centers
Acceptable Customer Input (in order of preference)	Masters, JEDEC Fuse Map, logic equation and test vectors	Logic diagram, customer-owned tooling (pattern-generation tape, composite drawing), circuit diagram, breadboard, functional specification	
Design Aids	CUPL, ABEL	Design rule checks, computer aided transient analysis, Applicon 760	Modular Design Environment (MDE) software modules include: The Logic Integrator - entry-level design & simulation tools; The Silicon Integrator - for design & simulation of complex ASICs; and The System Integrator - for designing an entire system, including multiple ASICs & standard components.
Production	Procured	Procured	In-house, on shore
Preferred Delivered Product	Packaged units	Packaged dice, dice	Packaged dice
Test Program Generation	Yes	Yes	Yes, automatic
Production Test	Programmability, functional, parametric, and ac	Functional, parametric, burn-in, thermal shock, environmental, MIL	Functional, parametric to Mil 883B
Electrical Test Systems Available	Sentry	Macrodata 107 and customized equipment	Industry standard testers, Sentry Series 10,20, Ando 256 pin 40 MHz.
Comments	Programmer available	Multiple-sourced production	Multiple sourced; over 20 LSI design centers



## IC MASTER

## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Master Logic Corporation	Matra Design Systems	MCE Semiconductor
FOR DETAILED DATA SEE:			
Customized Standard Circuits	Digital	Digital	Linear, digital, combined linear/digital, bipolar, CMOS
Gate Array	Silicon- or metal-gate CMOS	Silicon-gate CMOS	CMOS, ECL, dielectric isolation, I <sup>2</sup> L, Linear
Chip Density Range (equiv. gates)	50 to 1500, silicon-gate; 50 to 600, metal-gate	250 to 1,200	50 to 10,000
Cell Library	Yes	LS or HCMOS SSI/MSI function libraries	Yes
Design Kit Available	Yes		Yes
Full Custom Circuits			
Digital	Silicon- or metal-gate CMOS		CMOS, TTL, LSTTL, I <sup>2</sup> L, ECL, linear
Linear	No		Up to 75 volts
Combined Digital Linear	No		Up to 20 volts
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Any		MCE will interface with customer anywhere in design sequence; UniDES software
Design Aids	Design manual, CAD with VIA Systems' GATES design package	IBM PC XT based total integrated system for gate array designs	Logic simulation, breadboard assistance, design rule checks, UniDES
Production	Procured		In-house manufacturing; 4-inch wafer fabrication
Preferred Delivered Product	Any		Mapped wafers; probed wafers; scribed dice; substrate-mounted dice; packaged dice; custom packaging
Test Program Generation	Yes	Yes	Yes
Production Test	In-house		Functional; parametric
Electrical Test Systems Available	Pragmatic Designs		Teradyne J273 and A300 with laser trim; Pragmatic Inspector 200 (72 pin digital IC); Kiethley 300
Comments	Multiple sourced		Functional arrays available CMOS MGA and SGA series; also linear function cells



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Micrel	Micro Linear	Micro Power Systems
FOR DETAILED DATA SEE:	(Page 4276)		
Customized Standard Circuits	Combined CMOS/DMOS linear/digital	Analog semicustom ASIC with some digital	2,000 digital, linear and digital/linear cells
Gate Array		Bipolar tile array	
Chip Density Range (equiv. gates)		500 to 3,000 analog components	Up to 10,000 gates
Cell Library	Yes	Macrocells available	CMOS, bipolar, with BiMOS with thin film resistors
Design Kit Available		Yes	Yes
Full Custom Circuits Digital	PMOS, CMOS, DMOS, NMOS silicon or metal-gate, isopolar type processing		Moly gate CMOS, bipolar, BiMOS, all compatible with thin film resistors
Linear	Bipolar, CMOS, DMOS	Yes	High gain/low current analog bipolar, CMOS, BiMOS with thin film resistor; (10 ohms to megohms)
Combined Digital Linear	Up to 200 volts	Yes	CMOS digital/linear bipolar digital/linear BiMOS digital/linear all compatible with thin film resistors
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Customer owned tooling, PG tape, database tape; circuit logic, functional specifications	Analog schematic diagram, CAD schematic with simulations, GDSII tape	Circuit logic diagrams, functional specifications, customer owned tooling, PG tapes, database tapes, breadboards
Design Aids	Design rule checks, Calma CAD, breadboard, logic simulation, circuit simulation	Engineering support, Analog Design Tools and Daisy CAD libraries, kit parts	Cooperative design, logic/circuit diagrams, Calma CAD, workstation based, and design tools
Production	In-house wafer fabrication; 4-inch lines. Procured assembly	In-house and procured	In-house wafer fabrication, two second sources
Preferred Delivered Product	Packaged tested die, probed wafers, mapped wafers	Dice or packaged units	Customer specified: wafers, die, final test, custom and standard packages available
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, MIL STD 883. Rad hard Class B,S	Functional, parametric, burn-in, full MIL-STD-883C	Functional, parametric, burn-in, environmental, linear, full MIL STD 883, rad hard
Electrical Test Systems Available	Sentry VII, Series 20	Sentry	Custom testers, BTS, Datatron, Fairchild, LTS, Macrodata
Comments	Bipolar-linear, CMOS, DMOS power devices combined; 60V, 100V, 200V; 3 $\mu$ CMOS Si-gate dual poly; 1 GHz DMOS power FET	Mostly linear arrays with some digital capacity (120 gates)	Combination CMOS and bipolar, 1 to 5V CMOS, 1 to 200 $^{\circ}$ V bipolar, 2-micron 250 MHz CMOS (Flash-MOS); bipolar linear combined with digital CMOS and thin film resistors (HallMOS)



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Micro-Rel	Mitel Semiconductor	Mitsubishi Electronics America, Inc.
FOR DETAILED DATA SEE:	(Page 4280)		
Customized Standard Circuits		Digital	Digital
Gate Array		Silicon-gate CMOS	3 $\mu$ , 2 $\mu$ , 1.3 $\mu$ silicon-gate CMOS
Chip Density Range (equiv. gates)		500- 6,000 gates	200 to 50,000 2-input NAND
Cell Library	Silicon-gate CMOS	Silicon-gate CMOS	CMOS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	Silicon-gate CMOS	Silicon-gate CMOS	
Linear	Silicon-gate CMOS, bipolar	Silicon-gate CMOS, double poly	
Combined Digital Linear	Silicon-gate CMOS	Silicon-gate CMOS, double poly	
Provide Design Assistance	Yes	Yes	
Acceptable Customer Input (in order of preference)	Logic or circuit diagram, functional specification, breadboard, database tape	Functional specification, logic diagram, circuit diagram, customer-owned tooling	Netlist and test vectors, schematic using macrocell and test vectors, TTL- schematic and test vector or timing diagram
Design Aids	Logic and circuit simulation, kit parts available for linear bipolar design, schematic entry, DRC, ERC, LVS, LPE	Logic simulation, design rule checks	Circuit simulation, logic simulation, schematic entry, test program generation, design rule checks, fault simulation
Production	In-house	In-house	In-house
Preferred Delivered Product	Die, packaged devices, wafers, hybrids	Mapped wafers, probed wafers, scribed dice, packaged dice	Packaged
Test Program Generation	Yes	Yes	Automatic
Production Test	MIL STD, DESC 1772 certified	Functional, parametric, burn-in, thermal shock, environmental, MIL linear	Functional, parametric, burn-in standard
Electrical Test Systems Available	Sentry 7, Series 80	Sentry VII, LTX-DS80	Sentry, Ando
Comments	Radiation-hardened bipolar circuits available	Custom/semicustom products supplied through affiliate organization- VLSI Design Associates	Gate isolation; compatible with standard cell macrolibrary



**CUSTOM/SEMICUSTOM (cont.)**

Manufacturer	Monolithic Memories, Inc.	Motorola Semiconductor Products	National Semiconductor
FOR DETAILED DATA SEE:		(Page 4282)	(Page 4294)
Customized Standard Circuits		Digital	Digital
Gate Array	Field Programmable Logic- PAL and mask-programmed version- HAL	HCMOS, ECL, TTL-LS	Silicon-gate CMOS
Chip Density Range (equiv. gates)	100 to 5,000 gates	Up to 6,000 gates (gate arrays); up to 10,000 gates (standard cells)	To 12,000
Cell Library		Extensive digital, analog, functional block, $\mu P$ core	Yes
Design Kit Available	Yes	Training course, manuals	Yes
Full Custom Circuits			
Digital		NMOS, CMOS, ECL, TTL-LS, FAST	Metal-gate PMOS, metal- or silicon-gate NMOS, high voltage metal-gate CMOS, low voltage metal- and silicon-gate CMOS, metal double poly silicon-gate CMOS, dual layer XMOS, oxide isolated and Schottky devices, PL
Linear		Standard cells- HCMOS functional blocks	Same as above
Combined Digital Linear		Standard cells- HCMOS functional blocks	Same as above
Provide Design Assistance		21 Design Support Centers	Yes
Acceptable Customer Input (in order of preference)	PALS- not required; HALS- logic equations, 25-50 "seed" vectors for test generation software	CAD interface, verified netlist, circuit documentation.	Any
Design Aids	PALASM software for simulation, fault grading, fuse pattern generation, (mask design input for HALs)	Training course and manuals, software for simulation, timing analysis and test programs; popular engineering workstations	Computer aided circuit analysis, logic and system simulation, digitizing cell plotting and editing, design rule check, pattern generation, photolithography
Production	In-house	High volume production; in-house fab, assembly and test	In-house
Preferred Delivered Product	DIPs, LCCs, flat paks, PCCs, PGAs	Choice of packages- DIPs, PLCC, PGA, LCC for surface mount or thru board mount	Packaged dice
Test Program Generation	Yes	Yes, evaluation and production	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL	100% ac and dc parametric and functional	All except linear
Electrical Test Systems Available	In-house designed	Sentry Series, Sentinel, Trillium up to 256 I/O	Sentry VI and VII, Sentinel, Teradyne, Megatest
Comments	Several commercial programmers available	Complete standard cell and macrocell array families with mapability of designs; second source: NCR	Complete standard cell families available in 1.4 $\mu m$ CMOS

## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	NCM Corporation	NCR Microelectronics	NEC Electronics
FOR DETAILED DATA SEE:			
Customized Standard Circuits	Linear, digital, combination	Digital, linear, $\mu$ C, memory, combinations	Digital, linear, combined digital/linear
Gate Array	CMOS (si-gate, metal-gate), bipolar	Si-gate CMOS DLM $2\mu$ gate arrays	CMOS with analog macros, BiCMOS, ECL, TTL
Chip Density Range (equiv. gates)	1,000 (max.)	Up to 5,000 gates (gate array); up to 15,000 gates (standard cells)	CMOS up to 45,000 gates, BiCMOS up to 10,000 gates, ECL up to 8,000 gates, TTL up to 2,000 gates
Cell Library	Yes	$2\mu$ Si-gate CMOS DLM; $3\mu$ Si-gate CMOS 1 level metal, Supercells, Analog, $\mu$ P	SSI, MSI, Megamacros, analog macros
Design Kit Available	No	Training course, manuals, license	Yes; training course
Full Custom Circuits Digital	CMOS (Si-gate, metal-gate), bipolar, PMOS (si-gate, metal-gate)		Yes (and standard cell)
Linear	CMOS (si-gate, metal-gate), bipolar	Standard cells, Si-gate CMOS, $2\mu$ and $3\mu$ Supercells	Limited functions
Combined Digital Linear	CMOS (si-gate, metal-gate), bipolar	Standard cells, Si-gate CMOS, $2\mu$ and $3\mu$ Supercells	Yes, with limited analog macros
Provide Design Assistance	Yes	12 Design Centers	Yes
Acceptable Customer Input (in order of preference)	Functional specs, logic diagram, circuit diagram, breadboard, test vectors, customer-owned-tooling, known good devices	Verified netlist, circuit diagram and specs, database tape	Verified netlist, circuit diagram and specs, PG tape
Design Aids	Logic simulation, breadboarding, design rule check, cell library	Training course and manuals, software for simulation, timing analysis and test programs, popular engineering workstations	Training course and manuals, software for simulation, ERC, timing analysis, fault simulation, automatic test pattern generation if using NEC scan-path design, ATPG, support popular engineering workstations
Production	Procured	In-house fab and test, in-house and procured masks and packaging	In-house including Roseville, CA.
Preferred Delivered Product	Packaged units, dice, probed wafers, pc assemblies	Packaged units in DIPs, plastic leaded chip carrier, pin-grid arrays, chip-on-board, probed wafers or dice; SMT	Packaged parts
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal cycle	AC and DC functional and parametric, voltage/frequency corners	Functional, parametric
Electrical Test Systems Available	In-house built, microcomputer-controlled test systems	Sentry Series, Sentinel	Sentry, Ando
Comments		Complete standard cell and gate array compatibility; applications support; Design Centers; in-house mask shop; manufacturing and assembly; Second source: Motorola for $3\mu/2\mu$ std cells and $2\mu$ Macrocell arrays, Standard Microsystems for $3\mu$ std cells	Six design centers in the U.S. Complete gate array and standard cell capability. State-of-the-art processing and CAD tools.



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Pico Design	Plessey Solid State	Polycore Electronics
FOR DETAILED DATA SEE:			
Customized Standard Circuits	No	Digital, linear, combined digital/linear	
Gate Array	No	Bipolar, ECL and CMOS	Bipolar
Chip Density Range (equiv. gates)	10,000	ECL to 1,200; CMOS to 10,440	TTL to 500
Cell Library	Yes	Yes	
Design Kit Available	No	Yes	
Full Custom Circuits Digital	Silicon- or metal-gate PMOS, NMOS, CMOS, or other MOS	PMOS, NMOS, CMOS, I <sup>2</sup> L, ECL	MOS metal-gate, LSTTL, TTL, ECL
Linear	No	Bipolar, CMOS	Bipolar
Combined Digital Linear	No	I <sup>2</sup> L, ECL, bipolar, CMOS	Power interface/driver circuits
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, circuit schematic, breadboard, functional specification	Logic diagram, breadboard, customer-owned-tooling, database tape	Schematics, performance specs, customer-owned-tooling, database tape
Design Aids	Logic and circuit simulation, design rule checks, Calma GDSII	Design rule check, testability analyzer, autoplacement, autorouter, logic simulator	Breadboard simulation, SPICE
Production	Procured		In-house wafer fabrication, procured assembly
Preferred Delivered Product	All except PC-mounted packaged units	Packaged tested dice, scribed dice, probed wafers, mapped wafers	Packaged units, dice
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric	Functional, parametric, burn-in, MIL-STD-883	Functional, parametric, burn-in, thermal shock, environmental, MIL-STD-883
Electrical Test Systems Available	Fairchild, Sentry VII and Series 20	Teradyne J274, Fairchild Sentry, special in-house	Special in-house
Comments			Also provide silicon foundry service in linear, I <sup>2</sup> L, MOS metal gate, gold doped bipolar and dual layer metal ECL

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## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Precision Monolithics Inc.	Raytheon Semiconductor	S MOS Systems
FOR DETAILED DATA SEE:		(Page 4296)	(Page 4305)
Customized Standard Circuits	Linear	Linear, digital	Digital
Gate Array	From customer-owned-tooling	Bipolar digital ISL, bipolar digital ECL, bipolar digital/linear, CMOS digital	Silicon-gate CMOS
Chip Density Range (equiv. gates)		Up to 20,000 gates	400 to 38,550
Cell Library	Standard parts available in chip form	TTL, CMOS	Basic cells and MSI Macros
Design Kit Available	Kit parts	Yes	Yes
Full Custom Circuits Digital	TTL, LSTTL, ISL, I <sup>2</sup> L; ECL, ISO/CMOS Si-gate	Consult factory (bipolar)	Si-gate CMOS
Linear	20, 40, 60V supply voltage	Bipolar	
Combined Digital Linear	I <sup>2</sup> L, ECL, TTL, LSTTL	Consult factory (bipolar)	
Provide Design Assistance	Yes	Yes	
Acceptable Customer Input (in order of preference)	Customer-owned-tooling (pattern generator tape, composite drawing), known good device	TEGAS netlist, circuit schematics, physical database program	Netlist, P.G. tape, schematic
Design Aids	Kit parts	Evaluation devices, design source manual, factory tutorial	Schematic entry, circuit simulation, logic simulation, design and electrical rule checks
Production	In-house; 3" and 4" lines	Yes	In-house
Preferred Delivered Product	Mapped wafers, probed wafers, packaged units	Packaged units, dice	Any
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL, linear	Functional, parametric, burn-in, thermal shock, environmental, MIL	Functional, parametric
Electrical Test Systems Available	LTX, F-5000	Sentry 7, Sentry Series 21	Takeda-Riken
Comments	Ion implantation, dual layer metalization, nitride passivation, thin film resistors, MIL 38510 qualified	Radiation tolerance test data available	



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	SGS Semiconductor	Sierra Semiconductor	Signetics
FOR DETAILED DATA SEE:			(Page 4300)
Customized Standard Circuits	Digital and analog standard cell; digital channelled gate array	Analog telecomms/datacomms and EEPROM	Digital
Gate Array	Silicon-gate 1.5 $\mu$ ; silicon-gate 2 $\mu$ , 3 $\mu$ , 3.5 $\mu$		Silicon-gate CMOS, ECL 100K and 10K compatibility (0.5ns), ISL-48mA drive TTL compatible
Chip Density Range (equiv. gates)	100 to 12,000 gates; 200 to 10,000 gates; 200 to 20,000 gates	To 100,000 gates	330 to 1,100 Si-gate-CMOS; 600 to 2,200-ECL; Up to 2500 used gates -Flexx Array
Cell Library	CMOS	CMOS with analog and EEPROM	Silicon-gate CMOS, TTL and LSTTL-Si-gate CMOS; Macrocell library-ECL; Full library of soft & hard macros-Flexx Array
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital		CMOS 2 micron	No* Yes, using the Flexx Array as foundation
Linear	Very limited op amp, comparators & bandgap reference cells in standard cell library.	CMOS 2 and 3 micron, SCF	
Combined Digital Linear		CMOS 2 micron cell library, 3 micron custom	
Provide Design Assistance	Yes	Design centers worldwide	Yes
Acceptable Customer Input (in order of preference)	1. Netlist with test vectors; 2. Schematics with electrical or timing specs; 3. Functional description	IF or GDS II database, simulated netlist, schematic and specification, block diagram and specification	Schematic input
Design Aids	1. Circuit simulation; 2. Logic simulation; 3. Design Rule Checks; 4. Test program generation (gate array and sea-of-gates); 5. Schematic entry	Complete VLSI tools: schematic capture, simulation (including analog/digital simulation), layout, custom design	Schematic capture, complete simulation, auto place, auto route, auto test generation
Production	In-house	In-house, 5-inch with second source	In-house
Preferred Delivered Product	Package unit, others available	Wafers, die or packaged units	Packaged units
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric	Functional, parametric, burn-in	Functional, parametric and ac
Electrical Test Systems Available	Sentry 20/21	Sentry Series 80, Megatest Q2/62	Sentry VII, VIII, and 21, Takeda Riken system
Comments	CB200 digital & CB300 digital/analog standard cell families as well as sea-of-gatesxfamilies supported on Daisy, Mentor, Sun and VAX. Channelled arrays second sourced by LSI Logic and supported on Daisy, Mentor, Valid And PC workstations.	2 micron process shrinkable to 1.6 microns; second source VLSI Technology Inc.	*Standard cells from 200 to 2,000 gates

## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Silicon Systems Inc.	Siltronics	Sprague Electric Company
FOR DETAILED DATA SEE:			
Customized Standard Circuits	Analog/digital		
Gate Array			
Chip Density Range (equiv. gates)			
Cell Library	Analog/digital standard cells and compiled macros		
Design Kit Available	No		
Full Custom Circuits Digital	Silicon- or metal-gate PMOS, NMOS, CMOS, bipolar, TTL, STL, SRTL, LSTTL, ECL, I <sup>2</sup> L	TTL, STTL, LSTTL, I <sup>2</sup> L, ECL, other bipolar	Silicon-gate CMOS, NMOS, metal-gate CMOS
Linear	Silicon- or metal-gate PMOS, NMOS, CMOS, bipolar		Silicon-gate CMOS, NMOS
Combined Digital Linear	Silicon- or metal-gate CMOS, bipolar, TTL, SRTL, I <sup>2</sup> L, STL	I <sup>2</sup> L	Silicon-gate NMOS, CMOS
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Functional specification, logic diagram, circuit diagram, breadboard, test vectors		Minimum of functional diagram, breadboard, pattern generator tape or database tape
Design Aids	Breadboards, logic and circuit simulation, design rule checks, test-program development	Breadboard assistance, design rule checks	Logic simulator assistance, breadboard assistance, design rule checks
Production	In-house	In-house wafer fabrication; in-house assembly	In-house
Preferred Delivered Product	Packaged units and tested dice	Fully tested assembled package	No preference
Test Program Generation	Yes	Yes	Yes
Production Test	Automatic testers for analog and digital devices, functional and parametric	Customized to suit	Full screening available including burn-in and full environmental screening
Electrical Test Systems Available	LTX	LTX77, J259-style equipment, custom testers	Sentry VII, Sentinel, Teradyne
Comments		Specialize in mixed analog/digital bipolar; die sizes to 40,000 mil <sup>2</sup>	Capabilities include: design layout, CAP, mask shop, wafer fabrication assembly, and test



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Standard Microsystems Corporation	Stantel-STC	Sunshine Semiconductor
FOR DETAILED DATA SEE:	(Page 4310)		
<b>Customized Standard Circuits</b>	Digital, combined digital/linear, memory, $\mu$ C	Digital/analog, memory	Digital, combined linear/digital
Gate Array			
Chip Density Range (equiv. gates)	50 to 10,000	500 to 9,000	
Cell Library	Silicon-gate NMOS, CMOS	Silicon-gate NMOS/CMOS	Si-gate CMOS
Design Kit Available	Yes	Yes	
<b>Full Custom Circuits</b>			
Digital	Silicon-gate NMOS, CMOS	Silicon-gate CMOS/NMOS	Silicon-gate CMOS, metal-gate CMOS, nonvolatile CMOS
Linear	Silicon-gate NMOS, CMOS	Silicon-gate, CMOS/NMOS, UHF bipolar	
Combined Digital Linear	Silicon-gate CMOS	Silicon-gate CMOS/NMOS, merged bipolar/CMOS	Metal Gate CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specification, logic diagram, Calma database tape, netlist	Functional spec and block diagram, customer-owned-tooling, Calma database tape	Product description, block diagram with specifications, logic diagram
<b>Design Aids</b>	Logic simulation, design rule checks, electrical rule checks, transient analysis, automatic breadboard wiring, logic simulation with extracted delays, training course, software	Alphanumeric netlist or schematic entry, circuit simulation, logic simulation, design and electrical rule checking	Breadboard, circuit and logic simulation, DRC, graphics, NCC
<b>Production</b>	In-house	In-house	Procured
<b>Preferred Delivered Product</b>	Packaged devices preferred; all others available	Fully tested assembled packages, wafers and all others available	Packaged dice, bare dice, design and layout
<b>Test Program Generation</b>	Yes	Yes	Yes
<b>Production Test</b>	Full testing and screening including burn-in	Full testing and screening; burn-in if required	Procured
<b>Electrical Test Systems Available</b>	Fairchild Sentry 20, 21, Sentinel, Genrad GR-16	Fairchild Sentry	
<b>Comments</b>	Specialize in digital MOS/LSI and VLSI; will also customize by modifying MOS/LSI standard parts; second sources available; macrocells	Total capability offered	Services include product and specification finalization, logic and circuit design, layout, test definition

## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Supertex Inc.	Tektronix/Integrated Circuit Operations	Texas Instruments
FOR DETAILED DATA SEE:			(Page 4314)
Customized Standard Circuits	Linear, digital		Digital
Gate Array	Silicon- or metal-gate CMOS		Standard cells, silicon-gate CMOS, 2μ DLM SystemCell Series, 3μ
Chip Density Range (equiv. gates)	50 to 2,000		Up to 10,000
Cell Library			CMOS digital, analog, & CompilerCell functions (SRAM, ROM, PLA).
Design Kit Available	No		Yes
Full Custom Circuits Digital	Silicon- or metal-gate CMOS, HVC MOS for high voltage ICs	Full custom, bipolar	Silicon-gate CMOS
Linear	Silicon- or metal-gate CMOS	Full custom, bipolar, Quick Custom (analog arrays)	Yes
Combined Digital Linear	Silicon- or metal-gate CMOS, HVC MOS for high voltage ICs	Full custom, bipolar, Quick Custom (analog arrays)	Yes
Provide Design Assistance	Yes	Yes, also class instruction	Yes
Acceptable Customer Input (in order of preference)	Breadboard with functional specification and logic diagram, customer-owned tooling	Output from proprietary layout software, GDS, EDIF, Stream, Netlist, CIF, schematic and logic diagram	Workstation netlist (captured schematic/simulated database), functional specification, logic diagram
Design Aids	Logic simulation, breadboard assistance	Quickie (layout tools), T-Spice (SPICE simulator), T-Logs (logic simulator)	Simulation, testability analysis, test grading, design rule checking software, workstation-compatible cell libraries, design workshops, and manuals
Production	In-house	In-house	In-house
Preferred Delivered Product	Probed wafers, inspected dice, packaged dice	Ceramic and plastic leaded and leadless chip carrier hybrids, wafers and DIPs	Choice of packages: DIPs, SOIC, PLCC, LCC, PGA, and Quad Flat Pack
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, environmental	Parametric, functional	Functional and parametric
Electrical Test Systems Available	Teradyne J193, Genrad 2225, XINCOM	Sentry, Tektronix, laser wafer trimming to .01%	Sentry 21, ACTV, Trillium
Comments	Primary custom services include standard metal gate CMOS wafer foundry and full custom HVC MOS development and manufacturing.	Quick Custom, Quick Chips, analog and analog/digital arrays	Standard Cells characterized over full military temperature range; second source available, supported through Distributor Design Centers (Arrow/Wyle) and TI Regional Design Centers (Atlanta, Dallas, Boston, Chicago, Santa Clara)



**CUSTOM/SEMICUSTOM (cont.)**

Manufacturer	Thomson Components-Mostek	TLSI, Inc.	Toshiba America
FOR DETAILED DATA SEE:	(Page 4321)		(Page 4327)
Customized Standard Circuits	Digital, linear, combined digital/linear		Digital
Gate Array	Silicon-gate CMOS, double-level metal	Silicon-gate CMOS	Silicon-gate CMOS: 2 $\mu$ and 1.5 $\mu$
Chip Density Range (equiv. gates)	1,000 to 10,000	300 to 4,000	550 to 50,000 2-input NAND gates; also offers complementary standard cell line
Cell Library	Hard macros, soft TTL look-alike macros	Si-gate CMOS, NMOS digital/analog	CMOS
Design Kit Available		No	Yes
Full Custom Circuits Digital	Silicon-gate CMOS, double level metal, standard cell library	CMOS, NMOS, PMOS	1.5 $\mu$ CMOS, Mega-cell library, Z80 family, 82CXX peripherals, others, 1.2 $\mu$ 2H87
Linear	Yes	CMOS, NMOS, PMOS	1.5 $\mu$ CMOS, A/D, D/A, etc.
Combined Digital Linear	Yes	CMOS, NMOS, PMOS	Yes
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Simulated net list, logic diagram, functional test patterns	Specification, logic diagram, schematic, breadboard, customer-owned-tooling	1) Workstation interface (tape or floppy); 2) Logic diagram with netlist and test vectors; 3) circuit diagram/schematic
Design Aids	Highland 2 Design System- logic simulation, timing analysis, test pattern evaluation, automatic layout, back annotation of wiring capacitance, test program generation and design archiving	Custom cell library, logic simulation, CAD, CAE, design rule checks	Circuit simulation, logic simulation, test program generation; turn-key implementation for Mega-cell based custom circuits
Production	In-house	Procured	In-house
Preferred Delivered Product	Packaged device, dice	Packaged die, dice	Packaged units (DIP, PLCC, PFP, CFP, PGA)
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, ac, burn-in, MIL screened	Functional, parametric, burn-in, linear, MIL	Functional, parametric
Electrical Test Systems Available	Sentry 20	LTX, Genrad	Sentry VII, Sentry 10/20, TACT-820
Comments	No minimum production requirements	No minimum production requirements; second sources available	Toshiba offers gate array, standard cell and custom (super-integration); design centers in Boston, Dallas, and Sunnyvale CA.

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## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	TriQuint	Unicorn Microelectronics	United Microelectronics (UMC)
FOR DETAILED DATA SEE:	(Page 4328)		(Page 4329)
Customized Standard Circuits	GaAs Q-LOGIC standard cells, 100 ps depletion mode logic	Digital, microcomputer, PC peripheral combinations	Digital, combined digital/analog
Gate Array	TQ3000- GaAs enhancement/depletion gate array		3 $\mu$ and 2 $\mu$ silicon-gate HCMOS
Chip Density Range (equiv. gates)	Q-LOGIC up to 1,500 gates, TQ3000 up to 3,000 equivalent gates		200 to 4,080 2-input NAND gates
Cell Library	Yes for both	3 $\mu$ , 2 $\mu$ , 1.5 $\mu$ Si-gate CMOS, 2 level metal	HCMOS
Design Kit Available	Yes for both	No	Yes
Full Custom Circuits			
Digital	GaAs IC designs by customer or TriQuint	3 $\mu$ , 2 $\mu$ , 1.5 $\mu$ Si-gate CMOS, 2 level metal	5 $\mu$ metal-gate ALCMOS, 3 $\mu$ and 1.5 $\mu$ silicon-gate HCMOS
Linear	Including MMICs to 18 GHz		3 $\mu$ silicon-gate HCMOS
Combined Digital Linear	Yes		3 $\mu$ silicon-gate HCMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	CALMA GDSII for customer designs, Schematics for TriQuint designs	Function specification, logic diagram, breadboard, customer-owned-tooling (database tape, PG tape mask); SILOS netlist	Logic diagram, circuit diagram, breadboard, functional specification, test vectors, customer-owned-tooling
Design Aids	Detailed manuals, device models, logic models, Daisy, Mentor and Tektronix workstations	Silicon compiler, functional simulation, logic simulation, circuit extraction, circuit simulation, design and electrical rule check, test program development	Design rule checks, circuit simulation, logic simulation, schematic capture, test program generation, breadboard assistance
Production	In-house	Procured	In-house
Preferred Delivered Product	Wafers or packaged dice	Wafers or packaged units; specific customer requirements on request	Packaged units, others available
Test Program Generation	Yes	Yes	Yes
Production Test	Yes	Functional, parametric, burn-in	Functional, parametric, burn-in, thermal shock, environmental
Electrical Test Systems Available	Tektronix 32XX Series	Sentry VII, Sentry X, Sentry XX, STS 6120, STS 6060	Sentry VII, Sentry Series 20, Sentry Series 10, Teledyne, LTX
Comments	Custom foundry, semicustom arrays, custom design	Custom and semicustom turn-key design and manufacturing. Structural design using Compile Silicon Compiler with rich cell library of RAM, ROM, FIFO, datapath, $\mu$ Ps, core PC peripherals.	Complete custom capability; from consumer to industrial application; low power, high speed/performance; silicon compiler; hierarchical structured CMOS customer ICs



## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	United Silicon Structures	United Technologies Microelectronics Center	Universal Semiconductor, Inc.
FOR DETAILED DATA SEE:		(Page 4331)	
Customized Standard Circuits		Digital	Digital
Gate Array		3-micron silicon gate CMOS, 1.5-micron silicon gate CMOS	Silicon gate ISO CMOS
Chip Density Range (equiv. gates)		1,000 to 7,500 usable gates (gate array), 3,400 to 11,000 usable gates (standard cells)	99 to 2,400
Cell Library		CMOS	Silicon gate ISO-CMOS
Design Kit Available		Yes	Yes
Full Custom Circuits Digital	2 $\mu$ dual mayer metal CMOS, 1.5 $\mu$ dual layer metal CMOS		Silicon gate ISO-CMOS
Linear	2 $\mu$ dual layer metal/poly CMOS		Same as above
Combined Digital Linear			Same as above
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Netlist and test vectors, logic diagram, functional specification		Logic reconfigured as GATE/FF level; logic diagram, PG tapes, masks
Design Aids	Switch-level circuit simulation, logic simulation, test program generation, automatic circuit layout, design rule check	Schematic entry, design rule checks, logic simulation, testability analysis, layout, test program generation	Logic simulation, breadboard assistance, design rule checks, auto test generation, auto place/route, logic to layout verification
Production	In-house	In-house	In-house
Preferred Delivered Product	Packaged devices (tested or cut and go), dice, wafers (scribed or unscribed)		Package parts, dice probed wafers
Test Program Generation	Yes	Yes	Yes
Production Test	Sentry	MIL 883 screening	Functional, parametric, burn-in, thermal shock, environmental, MIL
Electrical Test Systems Available		Genrad, Trillium	Micro Manipulator, Sentry II, VI, VII, Sentry System 20, pragmatic functional tester, Fairchild Series 10
Comments	Complete silicon engineering product line takes the designer from design concept to working silicon.	Radiation hardened versions available	With smaller random logic circuits, prefer to start with a gate array and convert to full custom when manufacturing volumes justify the conversion

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## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	VLSI Design Associates	VLSI Microsystems, Inc.	VLSI Technology
FOR DETAILED DATA SEE:			(Page 4665)
Customized Standard Circuits	Digital/analog	Digital, combined digital/analog	
Gate Array			
Chip Density Range (equiv. gates)		100 to 12,000	
Cell Library	Silicon-gate CMOS, digital and analog	CMOS 2-metal 2-poly, CMOS 2-metal 1-poly	
Design Kit Available	Yes	No	
Full Custom Circuits			
Digital	Silicon-gate CMOS and NMOS, logic and memory, non-volatile memory	Silicon-gate CMOS	NMOS, HMOS, CMOS
Linear	Silicon-gate CMOS and NMOS, CCD, switched capacitor filters	Silicon-gate CMOS	NMOS, CMOS
Combined Digital Linear	CMOS	Silicon-gate CMOS	NMOS, CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, circuit diagram, functional specification, breadboard	Functional spec, logic diagram, circuit schematic, existing good device, breadboard	Functional specification, logic diagram, breadboard, customer-owned-tooling, data tape, PG tape, mask
Design Aids	In house: Calma GDS II, VAX11/780 and Mentor	Schematic capture, logic simulation, circuit simulation, timing analysis, DRC, ERC, LVS and LPE. Breadboard assistance.	PRISM VLSI design system, including high-level design language, circuit extraction, logic and circuit simulation, design rule checks, plotting, STIX
Production	Procured	Procured	In-house
Preferred Delivered Product	As requested	Packaged devices, scribed dice, others available	Packaged dice preferred; any on request
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric	Functional, parametric, environmental	Functional, parametric, burn-in, thermal shock, environmental, MIL
Electrical Test Systems Available		Testing arranged at silicon foundry	Sentry 20/120, Accutest
Comments	Independent design center, multiple sources, design aids	Complete custom design services of digital, linear, RAM, ROM, EPROM and EEPROM devices. Design instruction available.	Multiple sourcing compatibility, foundry services, training services, training and CAD aids to support user designed VLSI



CUSTOM/SEMICUSTOM (cont.)

Manufacturer	VTC	Waferscale Integration Inc.	Western Design Center
FOR DETAILED DATA SEE:	(Page 4332)		
Customized Standard Circuits	Linear, digital, combined linear/digital	Digital	Digital
Gate Array	2.0 $\mu$ silicon-gate CMOS		
Chip Density Range (equiv. gates)	Up to 6,000 gates	500 to 70,000 gates	Over 1,000
Cell Library	Linear/digital, digital	CMOS	CMOS
Design Kit Available	Yes	Second quarter 1988	Yes
Full Custom Circuits Digital	ECL, TTL, aimed standard cell, CMOS standard cell, VL2000 bipolar digital standard cell, VL5000 CMOS digital standard cell	1.2 $\mu$ silicon-gate CMOS	1.5 to 3 $\mu$ CMOS
Linear	Bipolar cell library and full custom		Limited CMOS
Combined Digital Linear	VL1000 bipolar linear/digital cell library		Limited CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Circuit diagram with test conditions and PG tape; circuit diagram with test conditions and simulated netlist; functional specification	Logic diagram with test vectors	"Idea" or market requirement, functional specification, logic diagram, logic capture file
Design Aids	Logic and circuit simulation, predesigned linear and digital cells, schematic entry, regional design centers	Schematic entry, logic simulation, circuit simulation, test program generation, design rule checks	1. Tool box design system emulation, 2. logic simulation, 3. circuit simulation, 4. test program generation, 5. design rules checks, logic capture, full custom graphics support
Production	Complete mask, wafer fab, packaging test facility	Procured	Procured
Preferred Delivered Product	Packaged devices or die	Packaged devices	Packaged devices
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL	Functional, parametric, burn-in, thermal shock, environmental, hi-rel processing	Functional, parametric, burn-in, device qual, package qual, full Mil
Electrical Test Systems Available	LTX with ESI Laser, Sentry 8, Sentry 80, MCT-2	Sentry Series 20, Teradyne, Trillium	Sentry
Comments	All libraries and gate arrays have full CAD support.	Macro-block modular-cell semicustom library available, high performance bit-slice, EPROM and logic on the same chip	Full custom, microprocessor-core-based technology, technology licensing, WGSC02, WGSC816 core microprocessor with support cores available

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## CUSTOM/SEMICUSTOM (cont.)

Manufacturer	Western Digital	ZyMOS	
FOR DETAILED DATA SEE:			
Customized Standard Circuits	Digital	Digital	
Gate Array	Silicon-gate NMOS	Silicon-gate CMOS	
Chip Density Range (equiv. gates)	Up to 1,000 gates	Up to 25,000 gates	
Cell Library	Yes	Yes	
Design Kit Available			
Full Custom Circuits Digital		CMOS	
Linear			
Combined Digital Linear			
Provide Design Assistance	Yes	Yes	
Acceptable Customer Input (in order of preference)	Functional specification, logic system	Logic input through ZyP CAD system, logic diagram, functional specification, customer-owned-tooling	
Design Aids	Logic simulation, design rule checks, test program development	Circuit simulation, logic simulation, test program generation, design rule checks, breadboard assistance; PC based schematic capture and simulation	
Production	In-house	In-house	
Preferred Delivered Product	Packaged units and test dice	Packaged units preferred, and on request	
Test Program Generation	Yes	Yes	
Production Test	Functional, burn-in	Functional, parametric	
Electrical Test Systems Available		Sentry VII, Series 20, Lomac	
Comments	Uncommitted logic arrays, 20 pin DIP, 130 prefabricated logic elements or 28/40 pin DIP, 400 prefabricated logic elements	ZyP CAD system- logic level design at customer's facility, CMOS silicon level simulation	



## ASIC/CUSTOM—Gate Arrays

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry			Input/Output Cells			Input/Output Compatibility					Comments	Device	Source	Line
				(μm)	Metal	Poly	Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State				
Texas Instruments																		
3200	0.5	208	CMOS	1	2	1			84	x	x	x		x	TGC103	◊° TI	(4314)	
5376	0.5	208	CMOS	1	2	1			118	x	x	x		x	TGC105	◊° TI	(4314)	
8896	0.5	208	CMOS	1	2	1			142	x	x	x		x	TGC108	◊° TI	(4314)	
AMCC																		
250	0.9 *	125	BIP	5μm	2		8		26		x	x	x	x	Speed/Power Programmable	Q720	◊† AMCC	
500	0.9 *	125	BIP	5μm	2		28		28		x	x	x	x	Speed/Power Programmable	Q710	◊† AMCC	
1000	0.9 *	125	BIP	5μm	2		38		38		x	x	x	x	Speed/Power Programmable	Q700	◊† AMCC	
1300	0.3	400	BIP	3μm	2				76		x	x	x		Speed/Power Programmable	Q1300S	† AMCC	
1394	1.0	50	CMOS	2μm	2		6		68	x	x	x		x	Q1400C	◊† AMCC		
	1.3*	60	CMOS	1.8	2		6		68	x	x	x		x	Q1400D	AMCC		
1500	0.9 *	200	BIP	5μm	2		46	38			x	x	x	x	Speed/Power Programmable	Q1500A	◊† AMCC	
1600	0.3	400	BIP	3μm	2				106		x	x	x		Speed/Power Programmable 1280-Bit RAM	QM1600S	† AMCC	
1700	0.9 *	200	BIP	5μm	2		60		60		x	x	x	x	Speed/Power Programmable	QH1500A	† AMCC	
1746	1.0	50	CMOS	2μm	2	1	6		76	x	x	x		x	Q1750C	◊† AMCC		
	1.3*	60	CMOS	1.8	2		6		76	x	x	x		x	Q1750D	◊ AMCC		
2232	1.2*	90	CMOS	1.5	2				82	x	x	x		x	Q2200J	AMCC		
2400	0.3	400	BIP	3μm	2				98		x	x	x		Speed/Power Programmable	Q2400S	† AMCC	
2667	1.0	50	CMOS	2μm	2	1	6		94	x	x	x		x	Q2700C	◊† AMCC		
	1.3*	60	CMOS	1.8	2		6		94	x	x	x		x	Q2700D	AMCC		
3312	1.0	50	CMOS	2μm	2	1	6		104	x	x	x		x	Q3300C	◊† AMCC		
	1.3*	60	CMOS	1.8	2		6		104	x	x	x		x	Q3300D	◊ AMCC		
3432	1.2*	90	CMOS	1.5	2					x	x	x		x	Q3400J	AMCC		
3500	0.3	400	BIP	3μm	2				120		x	x	x		Speed/Power Programmable	Q3500S	† AMCC	
4342	1.0	50	CMOS	2μm	2	1	6		120	x	x	x		x	Q4300C	◊† AMCC		
	1.3*	60	CMOS	1.8	2		6		120	x	x	x		x	Q4300D	AMCC		
4900	1.2*	90	CMOS	1.5	2					x	x	x		x	Q4900J	AMCC		
6206	1.0	50	CMOS	2μm	2	1	8		146	x	x	x		x	Q6200C	◊† AMCC		
	1.3*	60	CMOS	1.8	2		8		146	x	x	x		x	Q6200D	AMCC		
6210	1.2*	90	CMOS	1.5	2					x	x	x		x	Q6200J	AMCC		
8000	1.2*	90	CMOS	1.5	2					x	x	x		x	Q8000J	AMCC		
9250	1.2*	90	CMOS	1.5	2					x	x	x		x	Q9300J	AMCC		
Array Technology																		
150	1.4	35	CMOS	3μm	1	1			30	x	x	x		x	DHS150	ArrayTech		
300	1.4	35	CMOS	3μm	1	1			38	x	x	x		x	DHS300	◊ ArrayTech		
306	1.4	35	CMOS	3μm	1	1			35	x	x	x		x	HCD300	ArrayTech		
450	1.4	35	CMOS	3μm	1	1			48	x	x	x		x	DHS450	ArrayTech		
675	1.4	35	CMOS	3μm	1	1			58	x	x	x		x	DHS675	ArrayTech		
900	1.4	35	CMOS	3μm	1	1			68	x	x	x		x	DHS900	ArrayTech		
1008	1.4	35	CMOS	3μm	1	1			64	x	x	x		x	HCD1000	ArrayTech		
1200	1.4	35	CMOS	3μm	1	1			78	x	x	x		x	DHS1200	ArrayTech		
1500	1.4	35	CMOS	3μm	1	1			88	x	x	x		x	DHS1500	ArrayTech		
			CMOS	3μm	1	1			80	x	x	x		x	HCD1500	ArrayTech		
1800	1.4	35	CMOS	3μm	1	1			94	x	x	x		x	DHS1800	ArrayTech		
2208	1.4	35	CMOS	3μm	1	1			78	x	x	x		x	DHS2200	ArrayTech		
2673	1.4	35	CMOS	3μm	1	1			86	x	x	x		x	DHS2650	◊ ArrayTech		
AT&T																		
2000	0.9 *	200	BIP						84		x	x	x		LS2000	AT&T	(4211)	
Barvon Research, Inc.																		
500	2.2	35	CMOS	2μm	2				45	x	x	x		x	BC305	Barvon		
	4.2	38	CMOS	2μm	2		3		40	x	x	x		x	BC405	Barvon		
	5.0	33	CMOS	2μm	2		3		40	x	x	x		x	BC405	† Barvon		
(Continued)																		

(Continued)

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

**Bold face indicates additional data is provided on the page noted.**

## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State						
Barvon Research, Inc.	500																	(Cont'd)		
	6.0	25	CMOS	2	2		3		40	x	x	x		x			BC505	Barvon		
	7.2	27	CMOS	2	2		3		40	x	x	x		x			BC505	† Barvon		
1000	2.2	35	CMOS	2	2				70	x	x	x		x			BC310	Barvon		
	4.2	38	CMOS	2	2		3		65	x	x	x		x			BC410	Barvon		
	5.0	33	CMOS	2	2		3		65	x	x	x		x			BC410	† Barvon		
	6.0	25	CMOS	2	2		3		65	x	x	x		x			BC510	Barvon		
	7.2	27	CMOS	2	2		3		65	x	x	x		x			BC520	† Barvon		
1500	1.6	50	CMOS	2	2				76	x	x	x		x			BC210	† Barvon		
	2.2	35	CMOS	2	2				80	x	x	x		x			BC315	Barvon		
	4.2	38	CMOS	2	2		3		75	x	x	x		x			BC415	Barvon		
	5.0	33	CMOS	2	2		3		75	x	x	x		x			BC415	† Barvon		
	6.0	25	CMOS	2	2		3		75	x	x	x		x			BC515	Barvon		
	7.2	27	CMOS	2	2		3		75	x	x	x		x			BC515	† Barvon		
2000	2.2	35	CMOS	2	2				95	x	x	x		x			BC320	Barvon		
	4.2	38	CMOS	2	2		3		90	x	x	x		x			BC420	Barvon		
	5.0	33	CMOS	2	2		3		90	x	x	x		x			BC420	† Barvon		
	6.0	25	CMOS	2	2		3		90	x	x	x		x			BC520	Barvon		
	7.2	27	CMOS	2	2		3		90	x	x	x		x			BC520	† Barvon		
2500	1.6	50	CMOS	2	2				108	x	x	x		x			BC225	† Barvon		
California Devices																				
288	0.7	100	CMOS	1.5	2	1			26	x	x	x		x		Channel-less	CSB9003	◊† CalDevices		
864	0.7	100	CMOS	1.5	2	1			42	x	x	x		x		Channel-less	CSB9009	◊† CalDevices		
1512	0.7	100	CMOS	1.5	2	1			56	x	x	x		x		Channel-less	CSB9015	◊† CalDevices		
2430	0.7	100	CMOS	1.5	2	1			68	x	x	x		x		Channel-less	CSB9024	◊† CalDevices		
3528	0.7	100	CMOS	1.5	2	1			66	x	x	x		x		Channel-less	CSB8035	◊† CalDevices		
3816	0.7	100	CMOS	1.5	2	1			84	x	x	x		x		Channel-less	CSB9038	◊† CalDevices		
5400	0.7	100	CMOS	1.5	2	1			100	x	x	x		x		Channel-less	CSB9055	◊† CalDevices		
5712	0.7	100	CMOS	1.5	2	1			84	x	x	x		x		Channel-less	CSB8057	◊† CalDevices		
8085	0.7	100	CMOS	1.5	2	1			100	x	x	x		x		Channel-less	CSB8080	◊† CalDevices		
8316	0.7	100	CMOS	1.5	2	1			122	x	x	x		x		Channel-less	CSB9083	◊† CalDevices		
11592	0.7	100	CMOS	1.5	2	1			144	x	x	x		x		Channel-less	CSB9115	◊† CalDevices		
16848	0.7	100	CMOS	1.5	2	1			190	x	x	x		x		Channel-less	CSB9168	◊† CalDevices		
20574	0.7	100	CMOS	1.5	2	1			190	x	x	x		x		Channel-less	CSB9205	◊† CalDevices		
21336	0.7	100	CMOS	1.5	2	1			162	x	x	x		x		Channel-less	CSB8210	◊† CalDevices		
California Devices																				
200	1.1		CMOS	2μm	2	1	8		30	x	x	x		x		Channel-less	CHA200	CalDevices		
210	2.0	50	CMOS	3μm	2	1	8		22	x	x	x		x		Channel-less	DLM200	◊ CalDevices		
900	1.1		CMOS	2	2				54	x	x	x		x		Channel-less	CHA900	CalDevices		
990	2.0	50	CMOS	3μm	2	1	8		46	x	x	x		x		Channel-less	DLM900	CalDevices		
1224	2.0	50	CMOS	3μm	2	1	8		52	x	x	x		x		Channel-less	DLM1200	CalDevices		
1400	1.1		CMOS	2	2				68	x	x	x		x		Channel-less	CHA1400	CalDevices		
1680	2.0	50	CMOS	3μm	2	1	8		60	x	x	x		x		Channel-less	DLM1600	CalDevices		
2400	1.1		CMOS	2	2				86	x	x	x		x		Channel-less	CHA2400	CalDevices		
2850	2.0	50	CMOS	3μm	2	1	8		78	x	x	x		x		Channel-less	DLM2800	CalDevices		
3200	1.1		CMOS	2	2				96	x	x	x		x		Channel-less	CHA3200	CalDevices		
3600	2.0	50	CMOS	3μm	2	1	8		88	x	x	x		x		Channel-less	DLM3600	CalDevices		
4608	2.0	50	CMOS	3μm	2	1	8		100	x	x	x		x		Channel-less	DLM4600	CalDevices		
4800	1.1		CMOS	2	2				118	x	x	x		x		Channel-less	CHA4800	CalDevices		
6000	1.1		CMOS	2μm	2	1	8		114	x	x	x		x		Channel-less	CHA6000	CalDevices		
7200	2.0	50	CMOS	3μm	2	1	8		124	x	x	x		x		Channel-less	DLM7200	CalDevices		
8800	1.1		CMOS	2	2				156	x	x	x		x		Channel-less	CHA8800	◊ CalDevices		
10152	2.0	50	CMOS	3μm	2	1	8		148	x	x	x		x		Channel-less	DLM10000	CalDevices		
12000	1.1		CMOS	2	2				176	x	x	x		x		Channel-less	CHA12000	CalDevices		
California Micro Devices																				
200	3.1		CMOS	3μm						x	x	x			28 pads	C3002	CMD ASIC (4214)			
400	3.1		CMOS	3μm						x	x	x			40 pads	C3004	CMD ASIC (4214)			
(Continued)																				

(Continued)

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL						
California Micro Devices																			
500 to 2500	70 ps		GaAs	1												GaAs enhancement-depletion process			(Cont'd)
800	3.1		CMOS	3						x	x	x				60 pads	GAL8000	CMD ASIC	
1500	2.2		CMOS	2	2					x	x	x				72 pads	C3008	† CMD ASIC (4214)	
	3.1		CMOS	3						x	x	x				80 pads	C2015	† CMD ASIC (4214)	
																	C3015	CMD ASIC (4214)	
1800	3.1		CMOS	3						x	x	x				126 pads	C3018	CMD ASIC (4214)	5
2200	2.2		CMOS	2	2					x	x	x				88 pads	C2022	◊† CMD ASIC (4214)	
2500	0.97		CMOS	1.2	2					x	x	x				110 pads	C5025	† CMD ASIC (4215)	
2600	1.3		CMOS	1.5	2					x	x	x				90 pads	C1026	† CMD ASIC (4215)	
	3.1		CMOS	3						x	x	x				149 pads	C3026	CMD ASIC (4214)	
2800	2.2		CMOS	2	2					x	x	x				98 pads	C2028	◊† CMD ASIC (4214)	10
3100	3.1		CMOS	3						x	x	x				216 pads	C3031	CMD ASIC (4214)	
3200	1.3		CMOS	1.5	2					x	x	x				98 pads	C1032	† CMD ASIC (4215)	
4500	1.3		CMOS	1.5	2					x	x	x				116 pads	C1045	† CMD ASIC (4215)	
	2.2		CMOS	2	2					x	x	x				156 pads	C2045	† CMD ASIC (4214)	
5500	0.97		CMOS	1.2	2					x	x	x				140 pads	C5055	† CMD ASIC (4215)	15
5800	1.3		CMOS	1.5	2					x	x	x				134 pads	C1058	† CMD ASIC (4215)	
6100	2.2		CMOS	2	2					x	x	x				188 pads	C2061	† CMD ASIC (4214)	
8000	0.97		CMOS	1.2	2					x	x	x				186 pads	C5080	† CMD ASIC (4215)	
			CMOS	1.2	2					x	x	x				208 PADS, + 4K SRAM	C5080M	† CMD ASIC (4215)	
8200	1.3		CMOS	1.5	2					x	x	x				164 pads	C1082	† CMD ASIC (4215)	20
8400	2.2		CMOS	2	2					x	x	x				224 pads	C2084	† CMD ASIC (4214)	
10000	0.97		CMOS	1.2	2					x	x	x				208 pads	C5100	† CMD ASIC (4215)	
10500	1.3		CMOS	1.5	2					x	x	x				196 pads	C1105	† CMD ASIC (4215)	
	2.2		CMOS	2	2					x	x	x				232 pads	C2105	† CMD ASIC (4214)	
14500	1.3		CMOS	1.5	2					x	x	x				236 pads	C1145	† CMD ASIC (4215)	25
15000	0.97		CMOS	1.2	2					x	x	x				240 pads	C5150	† CMD ASIC (4215)	
18500	1.3		CMOS	1.5	2					x	x	x				276 pads	C1185	† CMD ASIC (4215)	
20000	0.97		CMOS	1.2	2					x	x	x				272 pads	C5200	† CMD ASIC (4215)	
25000	0.97		CMOS	1.2	2					x	x	x				304 pads	C5250	† CMD ASIC (4215)	
Cherry Semiconductor																			
192	50	2	I <sup>2</sup> L						24	x	x	x	x	x		Programmable speed/power	CS1200	Cherry	30
Circuit Technology Inc.																			
2436	4.0 *	25	CMOS	4	2		16	16	48	x	x	x		x			MA2024	† Marconi	
CML I/O, Honeywell																			
3500	0.4	100	CML	2.5	2				120		x	x	x	x		Avail. Radiation Hardened	HM3500(R)	Honeywell	
CMOS Programmable Gate Arrays																			
1200	2	70	CMOS	1.2	2	1			58	x		x		x		User Programmable	XC2064	◊† Xilinx (4346)	35
1800	2	70	CMOS	1.2	2	1			74	x		x		x		User Programmable	XC2018	◊† Xilinx (4346)	
2000	2	80	CMOS	1.2	2	1			64	x		x		x		User Programmable	XC3030	◊† Xilinx (4344)	
3000	2	80	CMOS	1.2	2	1			80	x		x		x		User Programmable	XC3030	† Xilinx (4344)	
4200	2	80	CMOS	1.2	2	1			96	x		x		x		User Programmable	XC3042	† Xilinx (4344)	
6400	2	80	CMOS	1.2	2	1			120	x		x		x		User Programmable	XC3064	† Xilinx (4344)	
9000	2	80	CMOS	1.2	2	1			144	x		x		x		User Programmable	XC3090	◊† Xilinx (4344)	
Custom Integrated Circuits																			
11400	30	10	I <sup>2</sup> L		2				62			x	x	x		Programmable speed/power, 7600 equiv. 5-input gates	GAC8000	† CIC	40

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line													
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL																			
Exar																																
140	8.0	8	CMOS	8	1				29	x	x	x		x	32 dedicated flip-flops	XR-CMA	† Exar	5														
156	3	35	CMOS	3	2	1			22	x	x	x		x	Silicon gate	30015	◊ Exar															
192	50	1	I <sup>2</sup> L		1				24	x	x	x		x	Programmable speed/power	XR200	† Exar															
200	8.0	8	CMOS	8	1				34	x	x	x		x	32 dedicated flip-flops	XR-CMB	Exar															
270	8.0	8	CMOS	8	1				40	x	x	x		x	32 dedicated flip-flops	XR-CMC	† Exar															
288	3	35	CMOS	3	2	1			30	x	x	x		x	Silicon gate	30030	◊ Exar															
	50	1	I <sup>2</sup> L		1				28	x	x	x		x	Programmable speed/power	XR300	† Exar															
440	8.0	8	CMOS	8	1				46	x	x	x		x	32 dedicated flip-flops	XR-CMD	† Exar															
460	3	35	CMOS	3	2	1			38	x	x	x		x	Silicon gate	30045	Exar															
520	50	1	I <sup>2</sup> L		1				40	x	x	x		x	Programmable speed/power	XR500	† Exar															
793	3	35	CMOS	3	2	1			50	x	x	x		x	Silicon gate	30080	Exar	10														
1548	3	35	CMOS	3	2	1			70	x	x	x		x	Silicon gate	30155	Exar															
3025	3	35	CMOS	3	2	1			98	x	x	x		x	Silicon gate	30300	Exar															
Exel Microelectronics																																
800	25	50	CMOS	1.5	2	2	22	10	10	x	x	x		x	E <sup>2</sup> Programmable	<b>XL78C800</b>	<b>EXEL</b>	<b>(4228)</b>														
Fairchild																																
100	0.75	600	ECL	1.5	2				21			x	x	x	All CMOS 2-Micron Silicon Gate  On-Chip Test Capability	FGE0050	Fairchild	15														
540	1.1	50	CMOS	2	2	1	0		40	x	x	x		x		FGC0500	◊ Fairchild															
680	0.75	600	ECL	1.5	2		36		36			x	x			FGE0500	◊ Fairchild															
864	1.1	50	CMOS	2	2		23		38	x	x	x		x		FGC0900	◊ Fairchild															
1188	1.1	50	CMOS	2	2	1	27		46	x	x	x		x		FGC1200	◊ Fairchild															
1932	1.1	50	CMOS	2	2		32		57	x	x	x		x		FGC1900	◊ Fairchild															
2500	0.75	600	ECL	1.5	2		60		60			x	x			FGE2000	◊ Fairchild															
2625	1.1	50	CMOS	2	2	1	39		70	x	x	x		x		FGC2400	◊† Fairchild															
2840	0.75	600	ECL	1.5	3		56		64			x	x			FGE2500	Fairchild															
3240	1.1	50	CMOS	2	2		43		78	x	x	x		x		FGC3200	◊ Fairchild															
3960	1.1	50	CMOS	2	2	1	47		86	x	x	x		x	FGC4000	◊† Fairchild																
6000	1.1	50	CMOS	2	2	1	55		106	x	x	x		x	FGC6000	◊† Fairchild																
6300	0.75	600	ECL	1.5	2					x	x	x	x	x	220 Max I/O	FGE6300	Fairchild															
7896	1.1	50	CMOS	2	2	1	63		118	x	x	x		x	181 Max I/O	FGC8000	Fairchild															
Ferranti Interdesign																																
130	2.5	80	CML	3	1				20	x	x	x	x	x	300 μW/gate, autoroutable	ULA1RA	Interdesign	30														
	7.5	20	CML	3	1				20	x	x	x	x	x	100 μW/gate, channel-less	ULA1RB	Interdesign															
	15	10	CML	3	1				20	x	x	x	x	x	30 μW/gate, channel-less	ULA1RC	Interdesign															
	50	10	CML	3	1				20	x	x	x	x	x	5 μW/gate, channel-less	ULA1RD	Interdesign															
140	17	9	CMOS	7	1				29	x	x	x			300 μW/gate, Channel-less	MCA	† Interdesign	35														
200	17	9	CMOS	7	1				34	x	x	x				MCB	† Interdesign															
270	17	9	CMOS	7	1				40	x	x	x				MCC	† Interdesign															
300	2.5	80	CML	3	1				30	x	x	x	x	x		ULA3RA	Interdesign															
	7.5	20	CML	3	1				30	x	x	x	x	x		ULA3RB	Interdesign															
	15	10	CML	3	1				30	x	x	x	x	x		ULA3RC	Interdesign															
	50	10	CML	3	1				30	x	x	x	x	x		ULA3RD	Interdesign															
340	17	9	CMOS	7	1				40	x	x	x			28 dedicated flip-flops	MCE	† Interdesign	40														
440	17	9	CMOS	7	1				46	x	x	x			32 dedicated flip-flops	MCD	† Interdesign															
500	2.5	80	CML	3	1				38	x	x	x	x	x	300 μW/gate, Channel-less	ULA5RA	Interdesign															
	7.5	20	CML	3	1				38	x	x	x	x	x	100 μW/gate, channel-less	ULA5RB	Interdesign															
	15	10	CML	3	1				38	x	x	x	x	x	30 μW/gate, channel-less	ULA5RC	Interdesign	45														
	50	10	CML	3	1				38	x	x	x	x	x	5 μW/gate, channel-less	ULA5RD	Interdesign															
630	17	9	CMOS	7	1				50	x	x	x			300 μW/gate, Channel-less	MCF	† Interdesign	50														
880	17	9	CMOS	7	1				58	x	x	x				MCG	† Interdesign															
900	2.5	80	CML	3	1				48	x	x	x	x	x		ULA9RA	◊ Interdesign															
	7.5	20	CML	3	1				48	x	x	x	x	x		ULA9RB	◊ Interdesign															
	15	10	CML	3	1				48	x	x	x	x	x		ULA9RC	◊ Interdesign															
	50	10	CML	3	1				48	x	x	x	x	x		ULA9RD	◊ Interdesign															
1200	2.5	80	CML	3	1				52	x	x	x	x	x	300 μW/gate, Channel-less	ULA12RA	Interdesign	55														
	7.5	20	CML	3	1				52	x	x	x	x	x	100 μW/gate, channel-less	ULA12RB	Interdesign															
	15	10	CML	3	1				52	x	x	x	x	x	30 μW/gate, channel-less	ULA12RC	Interdesign															
	50	10	CML	3	1				52	x	x	x	x	x	5 μW/gate, channel-less	ULA12RD	Interdesign															
																																(Continued)

(Continued)

† Military Temperature Range (−55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

**Bold face indicates additional data is provided on the page noted.**



## ASIC/CUSTOM—Gate Arrays (Cont'd)

ASICs/CUSTOM

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility				Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL					
Ferranti																		5
Interdesign																		
1600	2.5	80	CML	3	1			62	x	x	x	x	x	300 μW/gate, Channel-less	ULA16RA	Interdesign		
	7.5	20	CML	3	1			62	x	x	x	x	x	100 μW/gate, channel-less	ULA16RB	Interdesign		
	15	10	CML	3	1			62	x	x	x	x	x	30 μW/gate, channel-less	ULA16RC	Interdesign		
	50	5	CML	3	1			62	x	x	x	x	x	5 μW/gate, channel-less	ULA16RD	Interdesign		
2000	2.5	80	CML	3	1			72	x	x	x	x	x	300 μW/gate, Channel-less	ULA20RA	Interdesign		
	7.5	20	CML	3	1			72	x	x	x	x	x	100 μW/gate, channel-less	ULA20RB	Interdesign		
	15	10	CML	3	1			72	x	x	x	x	x	30 μW/gate, channel-less	ULA20RC	Interdesign		
	50	5	CML	3	1			72	x	x	x	x	x	5 μW/gate, channel-less	ULA20RD	Interdesign		
140	6	40	Si-Gate	4	1	1		24	x	x	x	x	x	Supply voltage 3 to 15 V.	MHB	Interdesign		
200	6	40	Si-Gate	4	1	1		30	x	x	x	x	x	Supply voltage 3 to 15 V.	MHC	Interdesign		
330	6	40	Si-Gate	4	1	1		40	x	x	x	x	x	Supply voltage 3 to 15 V.	MHD	Interdesign		
550	6	40	Si-Gate	4	1	1		48	x	x	x	x	x	Supply voltage 3 to 15 V.	MHE	Interdesign		
630	1.0	250	BIP	1.5	2			32	x	x	x	x	x		ULA6DSA	◊ Interdesign		
	1.6	150	BIP	1.5	2			32	x	x	x	x	x		ULA6DSB	◊ Interdesign		
	4.0	75	BIP	1.5	2			32	x	x	x	x	x		ULA6DSC	◊ Interdesign		
660	6	40	Si-Gate	4	1	1		56	x	x	x	x	x	Supply voltage 3 to 15 V.	MHF	Interdesign		
1000	6	40	Si-Gate	4	1	1		68	x	x	x	x	x	Supply voltage 3 to 15 V.	MHG	Interdesign		
1210	1.0	250	BIP	1.5	2			44	x	x	x	x	x		ULA12DSA	Interdesign		
	1.6	150	BIP	1.5	2			44	x	x	x	x	x		ULA12DSB	Interdesign		
	4.0	75	BIP	1.5	2			44	x	x	x	x	x		ULA12DSC	Interdesign		
1600	6	40	Si-Gate	4	1	1		84	x	x	x	x	x	Supply voltage 3 to 15 V.	MHH	Interdesign		
1870	1.0	250	BIP	1.5	2			64	x	x	x	x	x		ULA19DSA	Interdesign		
	1.6	150	BIP	1.5	2			64	x	x	x	x	x		ULA19DSB	Interdesign		
	4.0	75	BIP	1.5	2			64	x	x	x	x	x		ULA19DSC	Interdesign		
2550	1.0	250	BIP	1.5	2			74	x	x	x	x	x		ULA25DSA	Interdesign		
	1.6	150	BIP	1.5	2			74	x	x	x	x	x		ULA25DSB	Interdesign		
	4.0	75	BIP	1.5	2			75	x	x	x	x	x		ELA25DSC	Interdesign		
7920	1.6	150	BIP	1.5	2			138	x	x	x	x	x		ULA80DSB	Interdesign		
70	6	40	Si-Gate	4	1	1		18	x	x	x	x	x	Supply voltage 3 to 15 V.	MHA	Interdesign		
Fujitsu																		30
Microelectronics Inc.																		
336	1.5	125	CMOS	1.5	2	1		60	x	x	x		x	Twin-Tub Isolated CMOS, 24 mA outputs.	C330UHB	◊ Fujitsu (4229, 4233)		
	357	2.1	85	CMOS	1.8	2	1		42	x	x	x		x	Buffered 10 mA outputs.	C350AVB	Fujitsu (4229, 4231)	
		4.3	30	CMOS	2.3	2	1		42	x	x	x		x	Low Voltage Operation, 1.2 to 3.5 Volts.	C350AVL	Fujitsu (4229, 4231)	
360	1.9	120	BIP	2	2	0		40		x	x		x	24 mA outputs optional.	B240	Fujitsu (4230)		
528	3.6	85	BIP	2	2			60		x	x		x	48 mA outputs.	B350B	Fujitsu (4230)		
530	1.5	125	CMOS	1.5	2	1		68	x	x	x		x	Twin-Tub Isolated CMOS, 24 mA outputs.	C530UHB	Fujitsu (4229, 4233)		
540	1.9	120	BIP	2	2	0		48		x	x		x	360 equiv. 3-input gates	B350	Fujitsu (4230)		
549	2.1	85	CMOS	1.8	2	1		50	x	x	x		x	Buffered 10 mA outputs.	C540AVB	Fujitsu (4229, 4231)		
	4.3	30	CMOS	2.3	2	1		50	x	x	x		x	Low Voltage Operation, 1.2 to 3.5 Volts.	C540AVL	Fujitsu (4229, 4231)		
615	1.1	180	BiCMOS	1.5	2	1		52		x	x		x	24 mA output option, 3-input merged logic	BC400	Fujitsu (4230)		
830	1.5	125	CMOS	1.5	2	1		76	x	x	x		x	Twin-Tub Isolated CMOS, 24 mA outputs.	C830UHB	◊ Fujitsu (4229, 4233)		
852	2.1	85	CMOS	1.8	2	1		60	x	x	x		x	Buffered 10 mA outputs.	C850AVB	Fujitsu (4229, 4231)		
	4.3	30	CMOS	2.3	2	1		60	x	x	x		x	Low Voltage Operation, 1.2 to 3.5 Volts.	C850AVL	Fujitsu (4229, 4231)		
(Continued)																		

(Continued)

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL						
Fujitsu Microelectronics Inc.																			(Cont'd)
924	1.9	120	BIP	2	2	0			64		x	x		x	24 mA outputs optional.	B600	Fujitsu	(4230)	5
1002	1.4		CMOS	1.8	2	1			110	x	x	x		x	2K RAM	C1002AVM	Fujitsu	(4230)	
1080	3.6	85	BIP	2	2				72		x	x		x	48 mA outputs.	B700B	Fujitsu	(4230)	
1200	1.5	120	CMOS	1.5	2	1			95	x	x	x		x	Twin Tub Isolated CMOS, High Drive–10mA Outputs	C1200UHB	Fujitsu	(4229, 4231, 4233)	
1218	1.1	180	BiCMOS	1.5	2	1			72		x	x		x	24 mA output option, 3-Input merged logic.	BC800	Fujitsu	(4229, 4231, 4233)	
1245	2.1	85	CMOS	1.8	2	1			68	x	x	x		x	Buffered 10 mA outputs.	C1200AVB	Fujitsu	(4229, 4231, 4233)	10
	4.3	30	CMOS	2.3	2	1			68	x	x	x		x	Low Voltage Operation, 1.2 to 3.5 Volts.	C1200AVL	Fujitsu	(4229, 4231, 4233)	
1296	0.55	800	BIP	1	3		48	80			x	x	x		ECL 10kH, 100k Optional	ET750	Fujitsu	(4230)	
1564	2.1	85	CMOS	1.8	2	1			107	x	x	x		x	2304 bits of RAM (256x9).	C1502AVM	Fujitsu	(4229, 4231)	
1600	1.4		CMOS	1.8	2M	1P			76	x	x	x		x		C1600AVB	Fujitsu	(4229, 4231)	
1674	2.1	85	CMOS	1.8	2	1			76	x	x	x		x	Buffered 10 mA outputs.	C1600AVB	Fujitsu	(4229, 4231)	15
	4.3	30	CMOS	2.3	2	1			76	x	x	x		x	Low Voltage Operation, 1.2 to 3.5 Volts.	C1600AVL	Fujitsu	(4229, 4231)	
1680	1.9 *	150	TTL-LS						88		x	x		x	1120 equiv. 3-input gates	B1100	◊ Fujitsu	(4230)	
1724	1.5	125	CMOS	1.5	2	1			112	x	x	x		x	Twin-Tub Isolated CMOS, 24 mA outputs.	C1700UHB	Fujitsu	(4229, 4233)	
1800	1.1	180	BiCMOS	1.5	2	1			96		x	x		x	24 mA output option, 3-input merged logic	BC1200	Fujitsu	(4230)	
2000			CMOS	1.8	2	1			92	x	x	x		x	Buffered 10 mA outputs.	C2000AVB	Fujitsu	(4229, 4231)	20
	0.55	800	BIP	1	3				120		x	x	x	x	ECL 10kH, 100k optional	ETM2004	Fujitsu		
2052	4.3	30	CMOS	2.3	2	1			92	x	x	x		x	Low Voltage Operation, 1.2 to 3.5 Volts.	C2000AVL	Fujitsu	(4229, 4231)	
2220	1.5	125	CMOS	1.5	2	1			127	x	x	x		x	Twin-Tub Isolated CMOS, 24 mA outputs.	C2200UHB	Fujitsu	(4229, 4233)	
2352	0.55	800	BIP	1	3		48	80			x	x		x	ECL 10kH, 100k Optional	ET1500	Fujitsu	(4230)	
2375	2.1	85	CMOS	1.8	2	1			117	x	x	x		x	1K RAM	C2301AVM	Fujitsu	(4229, 4231)	25
2640	0.22	800	BIP	1	3				120			x	x			ET2009M	Fujitsu	(4230)	
	2.1	85	CMOS	1.8	2	1			106	x	x	x		x	2K RAM	C2600AV	Fujitsu	(4229, 4231)	
3000	0.55	800	BIP	1	3			72	120		x	x	x		ECL 10kH, 100k Optional	ETM2009	Fujitsu		
	1.5	120	CMOS	1.5	2	1			130	x	x	x		x	Twin Tub Isolated CMOS	C3000UHB	Fujitsu	(4229, 4233)	
3120	1.1	180	BiCMOS	1.5	2	1			112		x	x		x	24 mA output option, 3-input merged logic	BC2000	Fujitsu	(4230)	30
3162	0.95	185	TTL-LS						112		x	x		x	2108 equiv. 3-input gates	B2000	Fujitsu	(4230)	
3900	2.1	85	CMOS	1.8	2	1			127	x	x	x		x	2K RAM	C3900AV	Fujitsu	(4229, 4231)	
3960	0.22	800	BIP	1	3				120			x	x			ET3004M	Fujitsu	(4230)	
4087	2.1	85	CMOS	1.8	2	1			120	x	x	x		x	2K RAM	C4002AVM	Fujitsu	(4229, 4231)	
4174	1.5	125	CMOS	1.5	2	1			160	x	x	x		x	Twin-Tub Isolated CMOS, 24 mA outputs.	C4100UHB	Fujitsu	(4229, 4233)	30
4296	0.55	800	BIP	1	3			72	120		x	x	x	x	ECL 10K or 100K optional.	ET3000	Fujitsu	(4230)	
4320	0.55	800	BIP	1	3			72	120		x	x	x	x	ECL 10KH, 100K Optional	ETM3004	Fujitsu		
5022	2.1	85	CMOS	1.8	2	1			127	x	x	x		x	2K RAM	C5000AV	Fujitsu	(4229, 4231)	
(Continued)																			

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL						
Fujitsu Microelectronics Inc.																			
6000	1.5	120	CMOS	1.5	2	1			170	x	x	x		x	Twin Tub Isolated CMOS	C6000UHB	◊ Fujitsu	(4229, 4233)	5
6102	0.55	800	BIP	1	3			84	136		x	x	x	x	ECL 10K or 100K optional.	ET4500	Fujitsu	(4230)	
6664	2.1	85	CMOS	1.8	2	1			160	x	x	x		x	2K RAM	C6600AV	Fujitsu	(4229, 4231)	
8000	1.5	120	CMOS	1.5	3	1			210	x	x	x		x	6K of RAM, 12K of ROM	C80006UM	◊ Fujitsu		
	2.1	85	CMOS	1.8	2	1			160	x	x	x		x	2K RAM	C8000AV	Fujitsu	(4229, 4231)	
8768	1.5	125	CMOS	1.5	2	1			190	x	x	x		x	Twin-Tub Isolated CMOS, 24 mA outputs.	C8700UHB	Fujitsu	(4229, 4233)	10
10080	1.5	120	CMOS	1.5	3				219	x	x	x		x	12K bits of RAM, 24K bits of ROM.	C10012UM	Fujitsu	(4229, 4232)	
10456	0.35	1100	BIP	1	3			120	200		x	x	x	x	ECL 10KH, 100K Optional	ET7000H	Fujitsu		
12000	1.5	120	CMOS	1.5	2	1			229	x	x	x		x	Twin Tub Isolated CMOS	C12000UHB	Fujitsu	(4229, 4233)	
15120	1.5	120	CMOS	1.5	3				219	x	x	x		x	6K bits of RAM, 12K bits of ROM.	C15006UM	Fujitsu	(4229, 4232)	
16000	1.5	120	CMOS	1.5	3	1			220	x	x	x		x	Twin Tub Isolated CMOS.	C16000UH	◊ Fujitsu		15
20160	1.5	120	CMOS	1.5	3	1			220	x	x	x		x	Twin Tub Isolated CMOS.	C20000UH	Fujitsu	(4229, 4232)	
30000	1.0	130	CMOS	1.3	3	1			230	x	x	x		x	75% Usable Gates	C30000AU	Fujitsu		
40000	1.0	130	CMOS	1.3	3	1			260	x	x	x		x	75% Usable Gates	C40000AU	Fujitsu		
50000	1.0	130	CMOS	1.3	3	1			290	x	x	x		x	75% Usable Gates	C50000AU	Fujitsu		
75000	1.0	130	CMOS	1.3	3	1			350	x	x	x		x	75% Usable Gates	C75000AU	Fujitsu		20
100000	1.0	130	CMOS	1.3	3	1			400	x	x	x		x	75% Usable Gates	C100000AU	Fujitsu		
GE Intersil																			
1500	1.8	45	CMOS	4	1				84	x	x	x		x		IGD11500	† GE/Intersil		25
General Electric Semiconductor																			
379	1.7	50	CMOS	2	2	1			44	x	x	x		x	Silicon Gate	IGC20030	GE Semi		
408	6.0	12	CMOS	4	1	1			34	x	x	x		x	Silicon Gate	IGC10408	GE Semi		
756	6.0	12	CMOS	4	1	1			44	x	x	x		x	Silicon Gate	IGC10756	GE Semi		30
1023	1.7	50	CMOS	2	2	1			68	x	x	x		x	Silicon Gate	IGC20100	GE Semi		
1500	6.0	12	CMOS	4	1	1			62	x	x	x		x	Silicon Gate	IGC11500	GE Semi		
1984	1.7	50	CMOS	2	2	1			84	x	x	x		x	Silicon Gate	IGC20190	GE Semi		
3081	1.7	50	CMOS	2	2	1			100	x	x	x		x	Silicon Gate	IGC20290	GE Semi		35
4480	1.7	50	CMOS	2	2	1			120	x	x	x		x	Silicon Gate	IGC20450	GE Semi		
6195	1.7	50	CMOS	2	2	1			140	x	x	x		x	Silicon Gate	IGC20620	GE Semi		
13377	1.7	50	CMOS	2	2	1			200	x	x	x		x	Silicon Gate	IGC21350	GE Semi		
GoldStar																			
272	5.0	25	CMOS	3.5	1	1			36	x	x	x		x		GCL3020	GoldStar	(4242)	40
			CMOS	3.5	1	1			36	x	x	x		x		LL3020	GoldStar		
342	5.0	25	CMOS	3.5	1	1			40	x	x	x		x		GCL3030	GoldStar	(4242)	
			CMOS	3.5	1	1			40	x	x	x		x		LL3030	GoldStar		
420	5.0	25	CMOS	3.5	1	1			44	x	x	x		x		GCL3040	GoldStar	(4242)	45
			CMOS	3.5	1	1			44	x	x	x		x		LL3040	GoldStar		
600	5.0	25	CMOS	3.5	1	1			52	x	x	x		x		GCL3060	GoldStar	(4242)	
			CMOS	3.5	1	1			52	x	x	x		x		LL3060	GoldStar		
812	5.0	25	CMOS	3.5	1	1			60	x	x	x		x		GCL3080	◊ GoldStar	(4242)	
			CMOS	3.5	1	1			60	x	x	x		x		LL3080	GoldStar		50
880	1.4	118	CMOS	2	2	1			68	x	x	x		x		GCL7080	GoldStar	(4242)	
			CMOS	2	2	1			68	x	x	x		x		LL7080	GoldStar		
	2.5	66	CMOS	3	2	1			74	x	x	x		x		GCL5080	GoldStar	(4242)	
			CMOS	3	2	1			74	x	x	x		x		LL5080	GoldStar		
1056	5.0	25	CMOS	3.5	1	1			68	x	x	x		x		GCL3110	GoldStar	(4242)	55
			CMOS	3.5	1	1			68	x	x	x		x		LL3110	GoldStar		
(Continued)																			

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

♦ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State						
GoldStar																				(Cont'd)
1332	5.0	25	CMOS	3.5	1	1			76	x	x	x		x		GCL3130	GoldStar	(4242)		
			CMOS	3.5	1	1			76	x	x	x		x		LL3130	GoldStar			
1404	2.5	66	CMOS	3	2	1			92	x	x	x		x		GCL5140	GoldStar	(4242)		
			CMOS	3	2	1			92	x	x	x		x		LL5140	GoldStar			
1433	1.4	118	CMOS	2	2	1			86	x	x	x		x		GCL7140	GoldStar	(4242)	5	
			CMOS	2	2	1			86	x	x	x		x		LL7140	GoldStar			
1722	5.0	25	CMOS	3.5	1	1			86	x	x	x		x		GCL3170	GoldStar	(4242)		
			CMOS	3.5	1	1			86	x	x	x		x		LL3170	GoldStar			
2162	5.0	25	CMOS	3.5	1	1			96	x	x	x		x		GCL3210	GoldStar	(4242)	10	
			CMOS	3.5	1	1			96	x	x	x		x		LL3210	GoldStar			
2224	1.4	118	CMOS	2	2	1			106	x	x	x		x		GCL7220	GoldStar	(4242)		
			CMOS	2	2	1			106	x	x	x		x		LL7220	GoldStar			
	2.5	66	CMOS	3	2	1			114	x	x	x		x		GCL5220	GoldStar	(4242)		
			CMOS	3	2	1			114	x	x	x		x		LL5220	GoldStar			
2550	5.0	25	CMOS	3.5	1	1			104	x	x	x		x		GCL3250	GoldStar	(4242)	15	
			CMOS	3.5	1	1			104	x	x	x		x		LL3250	GoldStar			
3192	1.4	118	CMOS	2	2	1			128	x	x	x		x		GCL7320	GoldStar	(4242)		
			CMOS	2	2	1			128	x	x	x		x		LL7320	GoldStar			
	2.5	66	CMOS	3	2	1			138	x	x	x		x		GCL5320	GoldStar	(4242)	20	
			CMOS	3	2	1			138	x	x	x		x		LL5320	GoldStar			
4202	2.5	66	CMOS	3	2	1			156	x	x	x		x		GCL5420	GoldStar	(4242)		
			CMOS	3	2	1			156	x	x	x		x		LL5420	GoldStar			
4242	1.4	118	CMOS	2	2	1			150	x	x	x		x		GCL7420	GoldStar	(4242)		
			CMOS	2	2	1			150	x	x	x		x		LL7420	GoldStar			
6000	2.5	66	CMOS	3	2	1			180	x	x	x		x		GCL5600	GoldStar	(4242)	25	
			CMOS	3	2	1			180	x	x	x		x		LL5600	GoldStar			
6072	1.4	118	CMOS	2	2	1			186	x	x	x		x		GCL7600	GoldStar	(4242)		
			CMOS	2	2	1			186	x	x	x		x		LL7600	GoldStar			
8370	1.4	118	CMOS	2	2				222	x	x	x		x		GCL7840	GoldStar	(4242)	30	
			CMOS	2	2				222	x	x	x		x		LL7840	GoldStar			
10013	1.4	118	CMOS	2	2				232	x	x	x		x		GCL71000	GoldStar	(4242)		
			CMOS	2	2				232	x	x	x		x		LL71000	GoldStar			
Gould Inc.																				
500	3.5 *	25	CMOS						46	x	x	x				GA500	Gould		35	
540	3.0	125	CMOS	3	2	2			46	x	x	x		x		GA500D	Gould			
1120	1.5	35	CMOS	2	2	2			60	x	x	x		x		GB1000D	Gould	(4244)		
1152	3.0	30	CMOS	3	2	2			62	x	x	x		x		GA1000D	Gould			
2070	3.0	125	CMOS	3	2	2			84	x	x	x		x		GA2000D	Gould		40	
2128	1.5	35	CMOS	2	2	2			76	x	x	x		x		GB2000D	Gould			
3080	3.0	125	CMOS	3	2	2			102	x	x	x		x		GA3000D	Gould			
3264	1.5	35	CMOS	2	2	2			96	x	x	x		x		GB3000D	Gould			
4012	3.0	125	CMOS	3	2	2			120	x	x	x		x		GA4000D	Gould		45	
4256	1.5	35	CMOS	2	2	2			108	x	x	x		x		GB4000D	Gould			
5880	1.5	35	CMOS	2	2	2			132	x	x	x		x		GB6000D	Gould			
7872	1.5	35	CMOS	2	2	2			168	x	x	x		x		GB8000D	Gould			
9776	1.5	35	CMOS	2	2	2			192	x	x	x		x		GB10000D	Gould	(4244)		
Gould Inc.																				
5280	0.5		CMOS	1.2	2				50	x				x		GC5000	Gould	(4244)	50	
7488	0.5		CMOS	1.2	2				64	x				x		GC7500	Gould			
10320	0.5		CMOS	1.2	2				72	x				x		GC10000	Gould	(4244)		
15000	0.5		CMOS	1.2	2				84	x				x		GC15000	Gould			
19840	0.5		CMOS	1.2	2				100	x				x		GC20000	Gould	(4244)		
25344	0.5		CMOS	1.2	2				112	x				x		GC25000	Gould			
30000	0.5		CMOS	1.2	2				118	x				x		GC30000	Gould	(4244)	55	
38976	0.5		CMOS	1.2	2				138	x				x		GC35000	Gould			
GTE Microcircuits																				
504	3.5	10	CMOS	4μm	1	1			42	x	x	x		x		G50500B	CMD Micro			
960	3.5	10	CMOS	4μm	1	1			52	x	x	x		x		G51000B	CMD Micro			
																				(Continued)

(Continued)

† Military Temperature Range (−55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (µm)	Metal	Poly	Input/Output Cells		Input/Output Compatibility							Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State					
GTE																		(Cont'd)	
Microcircuits																			
1512	3.5	10	CMOS	4	1	1			68	x	x	x		x		G51500B	◊ CMD Micro		
2024	3.5	10	CMOS	4	1	1			80	x	x	x		x		G52000B	◊ CMD Micro		
Harris																			
600	3.0	10	CMOS	3					54	x	x	x		x		Radiation Hardened	HSG0600RH ‡ Harris	(2721)	
648	3.0	85	CMOS	3	1	1			56	x	x	x		x			HGAC00600RH	† Harris	
	3.5	75	CMOS	3	1	1			56	x	x	x		x			HGAC00600RH	† Harris	
1200	3.0	10	CMOS	3					78	x	x	x		x		Radiation Hardened	HSG1200RH ‡ Harris	(2721)	
1296	3.0	85	CMOS						80	x	x	x		x			HGAC01200RH	† Harris	
	3.5	75	CMOS						80	x	x	x		x			HGAC01200RH	† Harris	
2500	3.0	10	CMOS	3					100	x	x	x		x		Radiation Hardened	HSG2500RH ‡ Harris	(2721)	
2520	3.0	85	CMOS						102	x	x	x		x			HGAC02500RH	† Harris	
	3.5	75	CMOS						102	x	x	x		x			HGAC02500RH	† Harris	
Hitachi																			
America																			
200	4.0 *	20	Bi-CMOS													High Drive Capability, Low Power Dissipation	HD27K	Hitachi	
				3	2	1	18	18			x	x		x			HG61H04	Hitachi	
448	2.0 *	25	CMOS	2	2	1			54	x	x	x		x			HD61J	◊ Hitachi	
504	3.5 *	15	CMOS	3	2	1			50	x	x	x							
528	4.0 *	20	Bi-CMOS													High Drive Capability, Low Power Dissipation	HD27L	Hitachi	
				3	2	1	30	30			x	x		x			HG28E06	Hitachi	
630	2.0 *	25	BiCMOS	2	2	1			48	x	x	x		x			HG61H06	Hitachi	
660	2.0 *	25	CMOS	2	2	1			66	x	x	x		x					
864	2.0 *	25	BiCMOS	2	2	1			58	x	x	x		x					
966	4.0 *	20	Bi-CMOS													High Drive Capability, Low Power Dissipation	HD27P	Hitachi	
				3	2	1	40	40			x	x		x			HG61H09	◊ Hitachi	
968	2.0 *	25	CMOS	2	2	1			80	x	x	x		x			HG62E10	Hitachi	
1000	1.0 *		CMOS	1.3	2				68	x				x					
1008	2.0 *	25	BiCMOS	2	2	1			58	x	x	x		x					
1080	3.5 *	15	CMOS	3	2	1			68	x	x	x		x					
1326	2.0 *	25	BiCMOS	2	2	1			66	x	x	x		x					
1500	1.0 *		CMOS	1.3	2				78	x				x					
1530	4.0 *	20	Bi-CMOS													High Drive Capability, Low Power Dissipation	HD27Q	Hitachi	
				3	2	1	50	50			x	x		x			HG61H15	◊ Hitachi	
1560	2.0 *	25	CMOS	2	2	1			84	x	x	x		x			HD61L	◊ Hitachi	
1584	3.5 *	15	CMOS	3	2	1			68	x	x	x		x					
1800	2.0 *	25	BiCMOS	2	2	1			90	x	x	x		x					
2000	1.0 *		CMOS	1.3	2				80	x				x					
2010	2.0 *	25	CMOS	2	2	1			96	x	x	x		x					
2496	3.5 *	15	CMOS	3	2	1			104	x	x	x		x		Optional 512-bit RAM	HD61MM	◊ Hitachi	
2550	2.0 *	25	BiCMOS	2	2	1			114	x	x	x		x					
2560	2.0 *	25	CMOS	2	2	1			108	x	x	x		x					
2600	1.0 *		CMOS	1.3	2				88	x				x					
3600	1.0 *		CMOS	1.3	2				94	x				x					
4800	1.0 *		CMOS	1.3	2				114	x				x					
6200	1.0 *		CMOS	1.3	2				126	x				x					
8400	1.0 *		CMOS	1.3	2				154	x				x					
11000	1.0		CMOS	1.3	2				170	x				x					
20000	1.0 *		CMOS	1.3	2				240	x				x					
Honeywell																			
1000	1.0	400	BIP	5	2				60		x			x		Radiation Hardened ECL 10K compatible 1K RAM (256x9 or 512x4)	HM1000R	† Honeywell	
2000	0.3	500	BIP	2.5	3		76	44	20					x			HE2000	Honeywell	
3000	0.4	600	BIP	2.5	3				114					x			HM3000/RAM	† Honeywell	
3784	2.0	50	CMOS	1.8	2				120	x						Radiation Hardened	HC3500R	† Honeywell	
5000	0.6	150	BIP	2.5	2		44		76					x			HT5000	† Honeywell	
																		(Continued)	

(Continued)

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

◊ Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Comments	Device	Source	Line																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
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°Macrocell

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (µm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line		
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL								
Integrated Circuit Design Centre																					
560	10	15	CMOS	5	1				38	x	x	x		x	150 Cell Generic Library	C5M005G1	◊ ICDC	5			
960	10	15	CMOS	5	1				50	x	x	x		x		C5M010G1	ICDC				
1120	3	40	CMOS	3	2	1			48	x	x	x		x		C3M011G2	ICDC				
	4.0	20	CMOS	4	2				48	x	x	x		x		C4M010G2	ICDC				
1440	10	15	CMOS	5	1				62	x	x	x		x	150 Cell Generic Library	C5M015G1	ICDC	5			
1632	3	40	CMOS	3	2	1			56	x	x	x		x		C3M016G2	ICDC				
	4.0	20	CMOS	4	2		16	16	32	x	x	x		x		C4M012G2	ICDC				
2436	3	40	CMOS	3	2	1			72	x	x	x		x	150 Cell Generic Library	C3M024G2	ICDC	10			
	4.0	20	CMOS	4	2		16	16	48	x	x	x		x		C4M024G2	ICDC				
3876	3	40	CMOS	3	2	1			96	x	x	x		x	150 Cell Generic Library	C3M038G2	ICDC	10			
	4.0	20	CMOS	4	2		4	4	88	x	x	x		x		C4M038G2	ICDC				
6864	4.0	20	CMOS	4	2				128	x	x	x		x		C4M068G2	ICDC				
Integrated Circuit Systems																					
864	2.0	—	CMOS	2	2	1	23		38	x	x	x		x	150 Cell Generic Library	VGC0900	IntCirSys (4256)	15			
1188	2.0	—	CMOS	2	2	1	27		46	x	x	x		x		VGC1200	IntCirSys (4256)				
1242	2.5	—	CMOS	2	2	1	27		46	x	x	x		x		VGC0500	IntCirSys (4256)				
1932	2.0	—	CMOS	2	2	1	35		58	x	x	x		x		VGC1900	◊ IntCirSys (4256)				
2592	2.5	—	CMOS	2	2	1	39		70	x	x	x		x		VGC2400	◊ IntCirSys (4256)				
3240	2.0	—	CMOS	2	2	1	43		78	x	x	x		x		VGC3200	IntCirSys				
4020	2.5	—	CMOS	2	2	1	47		86	x	x	x		x		VGC4000	IntCirSys (4256)				
5930	1.9	85	CMOS	2	2		66		88	x	x	x		x		HD6000	IntCirSys (4256)				
6000	2.5	—	CMOS	2	2	1	55		106	x	x	x		x		VGC6000	◊ IntCirSys (4256)				
Interconics																					
112	18	3	CMOS						32	x	x	x		x		Metal Gate	INTERCHIP A		Interconics	25	
162	18	3	CMOS						38	x	x	x		x		Metal Gate	INTERCHIP B		Interconics		
216	18	3	CMOS						44	x	x	x		x		Metal Gate	INTERCHIP C		Interconics		
352	18	3	CMOS						53	x	x	x		x		Metal Gate	INTERCHIP D		Interconics		
504	4.0	20	CMOS						38	x	x	x		x		Silicon Gate	Interchip 50 †		Interconics		
560	18	3	CMOS						68	x	x	x		x	Metal Gate	INTERCHIP E	Interconics				
656	18	3	CMOS						68	x	x	x		x	Metal Gate	INTERCHIP F	Interconics				
960	4.0	20	CMOS						48	x	x	x		x	Silicon Gate	Interchip 100 †	Interconics				
1444	4.0	20	CMOS						62	x	x	x		x		Interchip 150 †	Interconics				
International Microcircuits Inc.																					
75	30	2	CMOS	5	1				23	x	x	x	x	x	Metal Gate	G4060	† IMI	35			
135	4.0	38	CMOS	3.5	1		8		20	x	x	x		x	Silicon Gate	G70090	◊† IMI				
140	30	2	CMOS	5	1				29	x	x	x	x	x	Metal Gate	G4112	† IMI				
200	30	2	CMOS	5	1				35	x	x	x	x	x	Metal Gate	G4160	† IMI				
275	30	2	CMOS	5	1				38	x	x	x	x	x	Metal Gate	G4220	† IMI				
330	30	2	CMOS	5	1				41	x	x	x	x	x	Metal Gate	G4264	† IMI				
375	3.3	42	CMOS	3.5	1	1	8		32	x	x	x		x	Silicon Gate	G70250	† IMI				
390	30	2	CMOS	5	1				43	x	x	x		x	Metal Gate	G4312	† IMI				
455	30	2	CMOS	5	1				47	x	x	x	x	x	Metal Gate	G4364	† IMI				
525	3.3	42	CMOS	3.5	1	1	11		37	x	x	x		x	Silicon Gate	G70350	† IMI				
	30	2	CMOS	5	1				49	x	x	x	x	x	Metal Gate	G4420	† IMI				
600	30	2	CMOS	5	1				53	x	x	x	x	x	Metal Gate	G4480	† IMI	45			
735	3.3	42	CMOS	3.5	1	1	8		44	x	x	x		x	Silicon Gate	G70490	◊† IMI				
820	1.4	60	CMOS	2	2	1			60	x	x	x	x	x		IMI6080	† IMI				
945	3.3	42	CMOS	3.5	1	1	11		48	x	x	x		x	Silicon Gate	G70630	† IMI				
1215	3.3	42	CMOS	3.5	1	1	8		56	x	x	x		x	Silicon Gate	G70810	◊† IMI				
1394	1.4	60	CMOS	2	2	1			74	x	x	x	x	x		IMI6140	† IMI				
1740	3.4	56	CMOS	2.5	2	1			64	x	x	x	x	x		G91160	† IMI				
1746	1.4	60	CMOS	2	2	1			82	x	x	x	x	x		IMI6170	◊† IMI				
1815	3.3	42	CMOS	3.5	1	1	8		68	x	x	x			Silicon Gate	G71210	† IMI				
2160	2.3	56	CMOS	2.5	2	1			100	x	x	x				G71440	◊† IMI				
2535	6.0	42	CMOS	3.5	1	1	8		88	x	x	x	x	x	Silicon gate	G71690	† IMI	50			
2646	2.3	56	CMOS	2.5	2	1			76	x	x	x	x	x		G91764	† IMI				
2667	1.4	60	CMOS	2	2	1			94	x	x	x	x	x		IMI6270	† IMI				
3312	1.4	60	CMOS	2	2	1			110	x	x	x	x	x		IMI6330	† IMI				

(Continued)

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‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility						Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL							
International Microcircuits Inc.																			(Cont'd)	
4342	1.4	60	CMOS	2	2	1			126	x	x	x	x	x			IMI6430	◊† IMI	5	
5250	2.3	56	CMOS	2.5	2	1			104	x	x	x		x			G93500	† IMI		
6200	1.4	60	CMOS	2	2	1			158	x	x	x	x	x			IMI6620	† IMI		
Laserpath Corp.																				
880	2.4	25	CMOS	2	2	0			66	x	x	x				Prototype in 5 days	LP5080A	Laserpath	10	
			CMOS	2	2	0			60	x	x	x				Prototype in 5 days	LP7080C	Laserpath		
			CMOS	2	2	0			44	x	x	x				Prototype in 5 days	LP7080P	Laserpath		
1400	2.4	25	CMOS	2	2	0			84	x	x	x				Prototype in 5 days	LP5140A	Laserpath	15	
			CMOS	2	2	0			78	x	x	x				Prototype in 5 days	LP7140C	Laserpath		
			CMOS	2	2	0			58	x	x	x				Prototype in 5 days	LP7140P	Laserpath		
2200	2.4	25	CMOS	2	2	0			106	x	x	x				Prototype in 5 days	LP5220A	◊ Laserpath	20	
			CMOS	2	2	0			98	x	x	x				Prototype in 5 days	LP7220C	Laserpath		
			CMOS	2	2	0			70	x	x	x				Prototype in 5 days	LP7220P	Laserpath		
3200	2.4	25	CMOS	2	2	0			130	x	x	x				Prototype in 5 days	LP5320A	Laserpath	25	
			CMOS	2	2	0			112	x	x	x				Prototype in 5 days	LP7320C	Laserpath		
			CMOS	2	2	0			80	x	x	x				Prototype in 5 days	LP7320P	Laserpath		
4200	2.4	25	CMOS	2	2	0			144	x	x	x				Prototype in 5 days	LP5420A	Laserpath	30	
			CMOS	2	2	0			134	x	x	x				Prototype in 5 days	LP7420C	Laserpath		
			CMOS	2	2	0			98	x	x	x				Prototype in 5 days	LP7420P	Laserpath		
6100	2.4	25	CMOS	2	2	0			168	x	x	x				Prototype in 5 days	LP5600A	Laserpath	35	
			CMOS	2	2	0			170	x	x	x				Prototype in 5 days	LP7600C	Laserpath		
			CMOS	2	2	0			122	x	x	x				Prototype in 5 days	LP7600P	Laserpath		
8400	1.7	50	CMOS	1.5	2	0			206	x	x	x					LP7840C	Laserpath	40	
			CMOS	1.5	2	0			150	x	x	x					LP7840P	Laserpath		
10000	1.7	50	CMOS	1.5	2	0			216	x	x	x				Available December 1987	LP71000C	Laserpath		
			CMOS	1.5	2	0			158	x	x	x				Available December 1987	LP71000P	Laserpath	25	
LSI Logic																				
	0.57		HCMOS	1.5	2	1			168	x	x	x		x		Rad Hard Library, 500k RADs (Si), No Latch Up	LRH10026	‡ LSI Logic	30	
			HCMOS	1.5	2	1			204	x	x	x		x		Rad Hard Library, 500k RADs (Si), No Latch Up	LRH10038	‡ LSI Logic		
			HCMOS	1.5	2	1			234	x	x	x		x		Rad Hard Library, 500k RADs (Si), No Latch Up	LRH10051	‡ LSI Logic		
			HCMOS	1.5	2	1			282	x	x	x		x		Rad Hard Library, 500k RADs (Si), No Latch Up	LRH10075	‡ LSI Logic	35	
			HCMOS	1.5	2	1			326	x	x	x		x		Rad Hard Library, 500k RADs (Si), No Latch Up	LRH10100	‡ LSI Logic		
			HCMOS	1.5	2	1			368	x	x	x		x		Rad Hard Library, 500k RADs (Si), No Latch Up	LRH10129	‡ LSI Logic		
	1.1		HCMOS	1.5	2	1			232	x	x	x		x		Rad Hard Library, 200k RADs (Si), No Latch Up	LRH91000	‡ LSI Logic	40	
			HCMOS	1.5	2	1			86	x	x	x		x		Rad Hard Library, 200k RADs (Si), No Latch Up	LRH9140	◊‡ LSI Logic		
			HCMOS	1.5	2	1			128	x	x	x		x		Rad Hard Library, 200k RADs (Si), No Latch Up	LRH9320	‡ LSI Logic		
			HCMOS	1.5	2	1			186	x	x	x		x		Rad Hard Library, 200k RADs (Si), No Latch Up	LRH9600	‡ LSI Logic	35	
554	1.4	CMOS	2	2	1			46	x	x	x		x				LL7050	LSI Logic	40	
880	1.1	CMOS	1.5	2	1				68	x	x	x		x			LL9080	† LSI Logic		
	1.4	CMOS	2	2	1				68	x	x	x		x			LL7080	† LSI Logic		
	2.5	CMOS	3	2	1				74	x	x	x		x			LL5080	† LSI Logic	40	
1404	2.5	66	CMOS	3	2	1			92	x	x	x		x			LL5140	◊† LSI Logic	45	
1443	1.1	CMOS	1.5	2	1				86	x	x	x		x			LL9140	† LSI Logic		
	1.4	118	CMOS	2	2	1			86	x	x	x		x			LL7140	† LSI Logic		
			CMOS	2	2	1			90	x	x	x		x		High Drive (10 mA Output)	LL8140	† LSI Logic	45	
1708	2.5	66	CMOS	3	2	1			96	x	x	x		x			LL5170	† LSI Logic	45	
1968	0.57		HCMOS	0.9	2					x		x		x			<b>LMb6020</b>	<b>LSI Logic (4268)</b>		
			HCMOS	0.9	2					x		x		x			<b>LMA9020</b>	<b>LSI Logic (4269)</b>		
2224	1.1	CMOS	1.5	2	1				106	x	x	x		x			LL9220	† LSI Logic	45	
	1.4	118	CMOS	2	2	1			106	x	x	x		x			LL7220	† LSI Logic		
			CMOS	2	2	1			110	x	x	x		x		High Drive (10 mA Output)	LL8220	◊† LSI Logic		
																			(Continued)	

(Continued)

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

\*Macrocell

◊ Available in Surface Mount Package

Bold face indicates additional data is provided on the page noted.



## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (µm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State				
LSI Logic																		
2224	2.5	66	CMOS	3	2	1			114	x	x	x		x		LL5220	† LSI Logic	(Cont'd)
3192	1.1		CMOS	1.5	2	1			128	x	x	x		x		LL9320	† LSI Logic	5
	1.4	118	CMOS	2	2	1			128	x	x	x		x		LL7320	† LSI Logic	
			CMOS	2	2	1			132	x	x	x		x	High Drive (10 mA Output)	LL8320	† LSI Logic	
	2.5	66	CMOS	3	2	1			138	x	x	x		x		LL5320	† LSI Logic	
3268	0.57		HCMOS	0.9	2					x		x		x		LMB6033	LSI Logic (4268)	10
3286	0.57		HCMOS	0.9	2					x		x		x		LMA9033	LSI Logic (4268)	
4202	2.5	66	CMOS	3	2	1			156	x	x	x		x		LL5420	† LSI Logic	
4242	1.1		CMOS	1.5	2	1			150	x	x	x		x		LL9420	† LSI Logic	
4992	1.4	118	CMOS	2	2	1			150	x	x	x		x		LL7420	† LSI Logic	15
	0.57		HCMOS	0.9	2					x		x		x		LMB6050	LSI Logic (4268)	
			HCMOS	0.9	2					x		x		x		LMA9050	LSI Logic (4268)	
6000	2.5	66	CMOS	3	2	1			180	x	x	x		x		LL5600	† LSI Logic	20
6072	1.1		CMOS	1.5	2	1			186	x	x	x		x		LL9600	† LSI Logic	
	1.4	118	CMOS	2	2	1			186	x	x	x		x		LL7600	† LSI Logic	
7238	0.57		HCMOS	0.9	2					x		x		x		LMB6072	LSI Logic (4268)	
			HCMOS	0.9	2					x		x		x		LMA9072	LSI Logic (4268)	25
8370	1.1		CMOS	1.5	2	1			222	x	x	x		x		LL9840	† LSI Logic	
	1.4	118	CMOS	2	2				222	x	x	x		x		LL7840	† LSI Logic	
9504	0.57		HCMOS	0.9	2					x		x		x		LMB6095	LSI Logic (4268)	
			HCMOS	0.9	2					x		x		x		LMA9095	† LSI Logic (4268)	30
10013	1.1		CMOS	1.5	2	1			232	x	x	x		x		LL91000	♦† LSI Logic	
	1.4	118	CMOS	2	2				232	x	x	x		x		LL71000	† LSI Logic	
14121	0.57		HCMOS	0.9	2					x		x		x		LMA9141	LSI Logic (4268)	
14124	0.57		HCMOS	0.9	2					x		x		x		LMB6141	LSI Logic (4268)	35
19000	0.57		HCMOS	0.9	2					x		x		x		LMB6190	LSI Logic (4268)	
			HCMOS	1.5	2					x		x		x		LMA9190	LSI Logic (4269)	
23408	0.57		HCMOS	0.9	2					x		x		x		LMA9239	† LSI Logic (4269)	
25710	0.7		CMOS	1.5	2	1			148	x	x	x		x	Channel-Free Array	LCA10026	LSI Logic (4270)	40
28388	0.57		HCMOS	0.9	2					x		x		x		LMA9284	† LSI Logic (4268)	
34944	0.57		HCMOS	0.9	2					x		x		x		LMA9350	† LSI Logic (4268)	
37932	0.7		CMOS	1.5	2	1			184	x	x	x		x	Channel-Free Array	LCA10038	LSI Logic (4270)	
50904	0.7		CMOS	1.5	2	1			214	x	x	x		x	Channel-Free Array	LCA10051	♦ LSI Logic (4270)	45
74970	0.7		CMOS	1.5	2	1			256	x	x	x		x	Channel-Free Array	LCA10075	LSI Logic (4270)	
100182	0.7		CMOS	1.5	2	1			256	x	x	x		x	Channel-Free Array	LCA10100	LSI Logic (4270)	
129042	0.7		CMOS	1.5	2	1			256	x	x	x		x	Channel-Free Array	LCA10129	LSI Logic (4270)	
Marconi Electronic Devices																		
392	3	35	CMOS	3	1	1			26	x	x	x		x		MA8304	† Marconi	50
560	10.0	15	CMOS	5	1	1			38	x	x	x		x		MA8505	† Marconi	
960	10.0	15	CMOS	5	1	1			50	x	x	x		x		MA8510	♦† Marconi	
1120	1.6 *	60	CMOS	3	2				48	x	x	x		x		MA2010A	† Marconi	
	4.0 *	25	CMOS	4	2				48	x	x	x		x		MA2010	† Marconi	55
1300	4 *	25	CMOS	4	2				28	x	x	x		x		MA2013	† Marconi	
1440	10.0	15	CMOS	5	1	1			62	x	x	x		x		MA8515	♦† Marconi	
1632	1.6 *	60	CMOS	3	2		16	16	32	x	x	x		x		MA2016A	† Marconi	
	3	35	CMOS	3	2		16	16	32	x	x	x		x		MA3016	† Marconi	55
	4.0 *	25	CMOS	4	2		16	16	32	x	x	x		x		MA2016	Marconi	
2436	1.6 *	60	CMOS	3	2		16	16	48	x	x	x		x		MA2024A	† Marconi	
	3	35	CMOS	3	2		16	16	48	x	x	x		x		MA3024	† Marconi	
2464	2.0 *	40	CMOS/SOS	3	2				80	x	x	x		x	Radiation Hardened	MA9024	♦‡ Marconi	55
3876	1.6 *	60	CMOS	3	2				96	x	x	x		x		MA2038A	† Marconi	
	2.0 *	40	CMOS/SOS	3	2				96	x	x	x		x	Radiation Hardened	MA9038	♦‡ Marconi	
	3	35	CMOS	3	2				96	x	x	x		x		MA3038	† Marconi	
	4	25	CMOS	4	2				96	x	x	x		x		MA2038	† Marconi	55
3904	0.9 *	100	CMOS	2	2				96	x	x	x		x		MA4039	† Marconi	
5510	0.9 *	100	CMOS	2	2				112	x	x	x		x		MA4055	† Marconi	
6864	1.6 *	60	CMOS	3	2				128	x	x	x		x		MA2068A	† Marconi	
(Continued)																		

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† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

♦ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL						
Marconi Electronic Devices 6864																			
	3	35	CMOS	3	2			128	x	x	x		x			MA3068	† Marconi	(Cont'd)	
	4	25	CMOS	4	2			128	x	x	x		x			MA2068	† Marconi		
	7544	0.9 *	100	CMOS	2	2			136	x	x	x		x			MA4075	† Marconi	
10044	0.9 *	100	CMOS	2	2			160	x	x	x		x			MA4100	† Marconi		
Matra Design Systems	228	2.0	20	CMOS	3	1	1		28	x	x	x		x			MA0250	Matra	5
	380	2.0	20	CMOS	3	1	1		36	x	x	x		x			MA0400	Matra	
	754	2.0	20	CMOS	3	1	1		50	x	x	x		x			MA0800	Matra	
	1139	3.0	25	CMOS					62	x	x	x					MA1200	Matra	
	1920	1.5	45	CMOS	2	2	1		78	x	x	x		x			MA2000	Matra	
	2660	1.5	45	CMOS	2	2	1		96	x	x	x		x			MA2700	Matra	10
	3900	1.5	45	CMOS	2	2	1		116	x	x	x		x			MA4000	Matra	
	4800	1.5	45	CMOS	2	2	1		132	x	x	x		x			MA5000	Matra	
Matra-Harris Semiconductor	228	2	40	HCMOS	3	1											MA0250	Matra-Harris	15
	380	2	40	HCMOS	3	1	36			x	x	x					MA0400	Matra-Harris	
	754	2	40	HCMOS	3	1	50									MA0800	Matra-Harris		
	810	1.5	45	Si-Gate CMOS															
				2	2	50				x	x	x					MB850	Matra-Harris	
	1139	2	40	HCMOS	3	1	62			x	x	x					MA1200	Matra-Harris	
	1300	1.5	45	Si-Gate CMOS															
				2	2	64				x	x	x					MB1300	Matra-Harris	
	1920	1.5	45	Si-Gate CMOS															
				2	2	78				x	x	x					MB2000	Matra-Harris	
	2600	1.5	45	Si-Gate CMOS															
				2	2	96				x	x	x					MB2700	◊ Matra-Harris	20
	3900	1.5	45	Si-Gate CMOS															
			2	2	110				x	x	x					MB4000	Matra-Harris		
4800	1.5	45	Si-Gate CMOS																
			2	2	132				x	x	x					MB5000	◊ Matra-Harris		
7500	1.5	45	Si-Gate CMOS																
			2	2	168				x	x	x					MB7500	Matra-Harris		
MCE Semiconductor	220	25	12	CMOS			8	10		x	x	x					MGA220	† MCE	25
	288	50	2	CMOS					28	x	x	x			Programmable speed/power		D15A	† MCE	
Mitsubishi Electronics America	224	0.9	175	CMOS	1.3	2	1	0	0	22	x	x	x		x	Gate Isolation Process	M60020	◊ Mitsubishi	30
	500	1.4	100	CMOS	2	2	1	0	0	64	x	x	x		x	Gate Isolation Process	M60011	◊ Mitsubishi	
	507	0.9	175	CMOS	1.3	2	1	0	0	32	x	x	x		x	Gate Isolation Process	M60021	◊ Mitsubishi	
	800	0.9	175	CMOS	1.3	2	1	0	0	42	x	x	x		x	Gate Isolation Process	M60022	◊ Mitsubishi	
	810	1.4	100	CMOS	2	2	1	0	0	82	x	x	x		x	Gate Isolation Process	M60012	◊ Mitsubishi	
	1100	1.4	100	CMOS	2	2	1	0	0	96	x	x	x		x	Gate Isolation Process	M60013	◊ Mitsubishi	
	1104	0.9	175	CMOS	1.3	2	1	0	0	45	x	x	x		x	Gate Isolation Process	M60023	◊ Mitsubishi	
	1680	1.4	100	CMOS	2	2	1	0	0	116	x	x	x		x	Gate Isolation Process	M60014	◊ Mitsubishi	
	1773	0.9	175	CMOS	1.3	2	1	0	0	62	x	x	x		x	Gate Isolation Process	M60024	◊ Mitsubishi	
	2400	0.9	175	CMOS	1.3	2	1	0	0	72	x	x	x		x	Gate Isolation Process	M60025	◊ Mitsubishi	
	2666	1.4	100	CMOS	2	2	1	0	0	132	x	x	x		x	Gate Isolation Process	M60015	◊ Mitsubishi	
	3608	1.4	100	CMOS	2	2	1	0	0	148	x	x	x		x	Gate Isolation Process	M60016	◊ Mitsubishi	
	4750	0.9	175	CMOS	1.3	2	2	1	0	88	x	x	x		x	Gate Isolation Process	M60030	◊ Mitsubishi	
	4814	1.4	100	CMOS	2	2	1	0	0	176	x	x	x		x	Gate Isolation Process	M60017	◊ Mitsubishi	
	6233	1.4	100	CMOS	2	2	1	0	0	178	x	x	x		x	Gate Isolation Process	M60018	◊ Mitsubishi	
	7300	0.9	175	CMOS	1.3	2	2	1	0	110	x	x	x		x	Gate Isolation Process	M60031	◊ Mitsubishi	
	8096	1.4	100	CMOS	2	2	1	0	0	190	x	x	x		x	Gate Isolation Process	M60019	◊ Mitsubishi	
	10800	0.9	175	CMOS	1.3	2	2	1	0	132	x	x	x		x	Gate Isolation Process	M60032	◊ Mitsubishi	
	20400	0.9	175	CMOS	1.3	2	2	1	0	180	x	x	x		x	Gate Isolation Process	M60034	◊ Mitsubishi	
																			(Continued)

(Continued)

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\* Typical Value

° Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State						
(Cont'd)																				
Mitsubishi Electronics America	25200	0.9	175	CMOS	1.3	2	2	1	0	196	x	x	x		x	Gate Isolation Process	M60035	◊ Mitsubishi	5	
	47375	0.9	175	CMOS	1.3	2	2	1	0	256	x	x	x		x	Gate Isolation Process	M60037	◊ Mitsubishi		
Monolithic Memories Inc.	720	0.9	150	CMOS	2	2	1			48	x	x	x		x	User-Programmable	MLA700	MMI	10	
	1008	0.9	150	CMOS	2	2	1			58	x	x	x		x		MLA1000	MMI		
	1200		70	CMOS	1.5	2	1			58	x	x	x		x		M2064	MMI		
	1376	0.9	150	CMOS	2	2	1			68	x	x	x		x	User-Programmable	MLA1400	MMI	10	
	1800		70	CMOS	1.5	2	1			74	x	x	x		x		M2018	MMI		
	1872	0.9	150	CMOS	2	2	1			84	x	x	x		x		MLA1800	MMI		
	2400	0.9	150	CMOS	2	2	1			98	x	x	x		x		MLA2400	◊ MMI	10	
	3212	0.9	150	CMOS	2	2	1			116	x	x	x		x		MLA3200	MMI		
	4032	0.9	150	CMOS	2	2	1			130	x	x	x		x		MLA4000	MMI	10	
	4968	0.9	150	CMOS	2	2	1			144	x	x	x		x		MLA5000	MMI		
	6032	0.9	150	CMOS	2	2	1			164	x	x	x		x		MLA6000	◊ MMI		
Mostek	1120	1.5	125	CMOS	2	2				56	x	x	x		x		GB1000D	† Thomson	15	
		1.5 *	125	CMOS	2	2				56	x	x	x		x		MKGB1000D	† Thomson		
	1152	2.5 *	40	CMOS	2	2				64	x	x	x		x		MKGA1000D	Thomson	20	
	2016	2.5 *	40	CMOS	2	2				84	x	x	x		x		MKGA2000D	Thomson		
	2128	1.5	125	CMOS	2	2				76	x	x	x		x		GB2000D	† Thomson	20	
		1.5 *	125	CMOS	2	2				76	x	x	x		x		MKGB2000D	† Thomson		
	3016	2.5 *	40	CMOS	2	2				104	x	x	x		x		MKGA3000D	Thomson	20	
	3264	1.5	125	CMOS	2	2				96	x	x	x		x		GB3000D	† Thomson		
		1.5 *	125	CMOS	2	2				96	x	x	x		x		MKGB3000D	† Thomson		
	4080	2.5 *	40	CMOS	2	2				120	x	x	x		x		MKGA4000D	Thomson	25	
	4256	1.5	125	CMOS	2	2				108	x	x	x		x		GB4000D	◊† Thomson		
		1.5 *	125	CMOS	2	2				108	x	x	x		x		MKGB4000D	† Thomson		
	5880	1.5	125	CMOS	2	2				132	x	x	x		x		GB6000D	† Thomson	30	
		1.5 *	125	CMOS	2	2				132	x	x	x		x		MKGB6000D	† Thomson		
	7872	1.5	125	CMOS	2	2				168	x	x	x		x		GB8000D	† Thomson	30	
		1.5 *	125	CMOS	2	2				168	x	x	x		x		MKGB8000D	† Thomson		
	9776	1.5	125	CMOS	2	2				192	x	x	x		x		GB10000D	† Thomson	30	
		1.5 *	125	CMOS	2	2				192	x	x	x		x		MKGB10000D	† Thomson		
Motorola	533	1.8	80	ECL	1	2		30	15	12	x	x	x		x	Macrocell array	MCA500ALS	Motorola (4282)	35	
	625	0.7	250	ECL	1	2		28		18				x		Macrocell array	MCA600ECL	Motorola (4282)		
	648	1.1	85	CMOS	2	2					x	x	x				HCA62A06	Motorola (4282, 4289)	35	
		1.9	85	CMOS	2	2				35	x	x	x		x		HCA6206	Motorola		
		2.5	40	CMOS	3	2		2		33	x	x			x		HCA6306	Motorola		
	704	1.7	135	BiMOS	2	2				44	x	x	x	x	x		BCA700ETL	Motorola (4285)	40	
	902	0.3	600	MOSAIC	2	2		28		18				x			MCA800ECL	Motorola (4282)		
	957	1.1	85	CMOS	2	2					x	x	x				HCA62A10	Motorola (4282, 4289)	40	
	1192	0.7	250	ECL	1	2		34		26				x		Macrocell array	MCA1200ECL	Motorola (4282)		
	1200	1.9	85	CMOS	2	2		17		42	x	x	x		x		HCA6212	Motorola	40	
		2.5	70	CMOS	3	2		17		42	x	x	x		x		HCA6312	Motorola		
	1280	1.8	80	ECL	1	2		36		40	x	x	x		x	Macrocell array	MCA1300ALS	Motorola (4282)	45	
	1638	1.1	85	CMOS	2	2					x	x	x				HCA62A17	Motorola (4282, 4289)		
	1708	0.75 *	100	MOSAIC II		3				120				x		Macrocell Array	MCA1500M	Motorola (4282, 4287)	45	
	1792	1.7	135	BiMOS	2	2				92	x	x	x	x	x		BCA1800ETL	Motorola (4285)		
	1800	1.1	125	ECL	2	2				120		x	x	x		RAM included	MCA2800RAM	Motorola (4282)	50	
	2295	2.5	70	CMOS	3	2		55		56	x	x	x		x		HCA6324	Motorola		
	2412	0.3	600	ECL	2	3		52		68				x		Macrocell array	MCA2500ECL	Motorola (4282)	50	
	2430	1.9	85	CMOS	2	2		8		80	x	x	x		x		HCA6225	Motorola		
(Continued)																				

(Continued)

† Military Temperature Range (−55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL						
Motorola																		(Cont'd)	
2448	1.1	85	CMOS	2	2					x	x	x				HCA62A25	Motorola	(4282, 4289)	
2958	0.6	125	MOSAIC	2	3				120	x	x	x	x	x	Macrocell array	MCA2900ETL	Motorola		
2980	0.6	125	ECL	2	3				120	x	x	x		x		MCA2800ALS	Motorola	(4282)	
3000	0.15	1200	ECL	1	1				120				x			MCA3000ECL	Motorola	(4287)	
3600	1.1	85	CMOS	2	2					x	x	x				HCA62A36	Motorola	(4282, 4289)	
3796	1.9	85	CMOS	2	2				95	x	x	x		x		HCA6238	Motorola		
4032	1.7	135	BiMOS	2	2				136	x	x	x	x	x		BCA4000ETL	Motorola	(4285)	
4860	1.9	85	CMOS	2	2		53		54	x	x	x		x		HCA6248	Motorola		
	2.5	70	CMOS	3	2		53		54	x	x	x		x		HCA6348	Motorola		
4968	1.1	85	CMOS	2	2					x	x	x				HCA62A50	Motorola	(4282, 4289)	
5670	0.25		CMOS	1	3				96	x		x		x	Bipolar and MOS Macrocell Array	HDC005	Motorola	(4286)	
6000	1	—	BiMOS								x	x	x			MCA600ETL	Motorola	(4282)	
6708	1.1	85	CMOS	2	2				146	x	x	x		x		HCA62A67	Motorola	(4282, 4289)	
7000	0.15	1200	ECL	1	1				180				x			MCA7000ECL	Motorola	(4287)	
7500	0.15	1200	ECL	1	1				256				x			MCA7500RAM	Motorola	(4287)	
	1.7	135	BiMOS	2	2				228	x	x	x	x	x		BCA8000RAM	Motorola	(4285)	
8208	0.25		CMOS	1	3				108	x		x		x		HDC008	Motorola	(4286)	
8568	2.8		HCMOS	2	2		168			x	x	x				HCA62A85	Motorola	(4282, 4289)	
10000	0.3	600	ECL	2	2		224	200					x			MCA10000ECL	Motorola	(4287, 4290)	
11208	0.25		CMOS	1	3				120	x		x		x		HDC012	Motorola	(4286)	
16416	0.25		CMOS	1	3				136	x		x		x		HDC016	Motorola	(4286)	
26112	0.25		CMOS	1	3				168	x		x		x		HDC025	Motorola	(4286)	
31290	0.25		CMOS	1	3				180	x		x		x		HDC031	Motorola	(4286)	
47214	0.25		CMOS	1	3				212	x		x		x		HDC045	Motorola	(4286)	
63900	0.25		CMOS	1	3				240	x		x		x		HDC062	Motorola	(4286)	
80304	0.25		CMOS	1	3				264	x		x		x		HDC080	Motorola	(4286)	
104832	0.25		CMOS	1	3				300	x		x		x		HDC100	Motorola	(4286)	
Motorola Semiconductor Products																			
6144	0.8	200	BiMOS	2	2		202			x	x	x	x	x		BCA6000ETL	Motorola	(4285, 4291)	
National Semiconductor																			
600	2.1	110	CMOS	2	2		8		40	x	x	x		x		SCX6206	◊ National		
648	3.5	66	CMOS	3	2	1			37	x	x	x		x		SCX6306	National		
1260	2.1	110	CMOS	2	2		17		42	x	x	x		x		SCX6212	◊ National		
	3.5	66	CMOS	3	2	1	17		42	x	x	x		x		SCX6312	National		
1806	2.1	110	CMOS	2	2		3		70	x	x	x		x		SCX6218	◊ National		
2385	2.1	110	CMOS	2	2		55		56	x	x	x		x		SCX6224	National		
	3.5	66	CMOS	3	2	1	55		56	x	x	x		x		SCX6324	National		
2430	2.1	110	CMOS	2	2		12		76	x	x	x		x		SCX6225	◊ National		
	3.5	66	CMOS	3	2	1	12		76	x	x	x		x		SCX6325	◊ National		
3180	2.1	110	CMOS	2	2		3		101	x	x	x		x		SCX6232	◊ National		
4380	2.1	110	CMOS	2	2		3		110	x	x	x		x		SCX6244	◊ National		
4860	2.1	110	CMOS	2	2		53		54	x	x	x		x		SCX6248	National		
	3.5	66	CMOS	3	2	1	54		54	x	x			x		SCX6348	National		
6090	3.5	66	CMOS	3	2	1	66		88	x	x			x		SCX6360	National		
6260	2.1	110	CMOS	2	2		66		88	x	x	x		x		SCX6260	◊ National		
NCM Corp.																			
3001	10	5	CMOS	7.5	1				42	x	x	x		x	48 pads	NCM300XZ	NCM		
3002	10	5	CMOS	7.5	1M				39	x	x	x		x	44 pads	NCM300XZ	NCM		
3003	10	5	CMOS	7.5	1M				35	x	x	x		x	40 pads	NCM300XZ	NCM		
70013	1.5	20	CMOS	3	1	1			58	x	x	x		x	62 pads	NCM7001XZ	NCM		
70015	3	12	CMOS	5	1M	1P			58	x	x	x		x	62 pads	NCM7001XZ	NCM		

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL								
NCR																					
648	1.8	85	CMOS	2	2				44x	x	x	x		x	I/Os are user defined	NCR62A06	NCR	5			
957	1.8	85	CMOS	2	2				52x	x	x	x		x	I/Os are user defined	NCR62A10	NCR				
1638	1.8	85	CMOS	2	2				68x	x	x	x		x	I/Os are user defined	NCR62A17	NCR				
2448	1.8	85	CMOS	2	2				84x	x	x	x		x	I/Os are user defined	NCR62A25	NCR				
3600	1.8	85	CMOS	2	2				100	x	x	x		x	All I/Os are user defined	NCR62A36	◊ NCR				
4968	1.8	85	CMOS	2	2				124x	x	x	x		x	I/Os are user defined	NCR62A50	NCR				
NEC																					
888	2	50	CMOS	2	2				60	x	x	x		x		μPD65004	◊ NEC	10			
1200	1.0	200	ECL-3	2	2		40		48				x			μPB6311	NEC				
1600	2	50	CMOS	2	2		2		69	x	x	x		x		μPD65001	NEC				
2000	1.0	200	ECL-3	2	2		60		48				x			μPB6321	◊ NEC				
2128	1.4	70	CMOS	1.5	2				84	x	x	x		x		μPB65022	NEC				
2160	2	50	CMOS	2	2		2		69	x	x	x		x		μPD65021	NEC				
3000	1.0	200	ECL-3	2	2		100		80				x			μPB6330	◊ NEC	15			
3312	2	50	CMOS	2	2		7		94	x	x	x		x		μPD65030	NEC				
3725	1.4	70	CMOS	1.5	2				108	x	x	x		x		μPD65031	NEC				
4000	0.7	300	ECL-3A	2	2		84		72		x	x	x	x		μPB6340	NEC				
4104	2.0	50	CMOS	2	2		4		116	x	x	x		x		μPD65040	◊ NEC				
4727	1.4	70	CMOS	1.5	2				124	x	x	x		x		μPD65042	◊ NEC				
5000	0.7	300	ECL-3A	2	2		92		80		x	x	x	x		μPB6350	NEC	20			
6528	2.0	50	CMOS	2	2		8		136	x	x	x		x		μPD65060	NEC				
7164	1.4	70	CMOS	1.5	2				152	x	x	x		x		μPD65070	◊ NEC				
8028	1.4	70	CMOS	1.5	2				168	x	x	x		x		μPD65081	◊ NEC				
8056	2	50	CMOS	2	2		12		148	x	x	x		x		μPD65080	NEC				
10406	1.4	70	CMOS	1.5	2				196	x	x	x		x		μPD65101	NEC				
11250	2.0	50	CMOS	2	2		20		168	x	x	x		x		μPD65100	NEC	25			
14637	1.4	70	CMOS	1.5	2				240	x	x	x		x		μPD65150	NEC				
19551	1.4	70	CMOS	1.5	2					x	x	x		x		μPD65200	◊ NEC				
OKI Semiconductor																					
386				3	2											MSM71000	OKI	30			
770				3	2											MSM72000	OKI				
1440				3	2											MSM73000	OKI				
2000				3	2											MSM74000	OKI				
3000				2	2											MSM79H000	OKI				
4000				2	2											MSM75H000	◊ OKI				
				3	2											MSM7500	◊ OKI	35			
6000				2	2											MSM76H000	OKI				
8000				2	2											MSM77H000	OKI				
10000				2	2											MSM78H000	OKI				
700	1.9	150	CMOS	1.5	2				x	x		x		x	Output buffers can sink/source up to 16 mA.	70V000	◊ OKI	40			
	2.5	100	CMOS	2	2				x	x		x		x		70HB000	◊ OKI				
			CMOS	2	2				x	x		x		x		70H000	◊ OKI				
1000	1.9	150	CMOS	1.5	2				x	x		x		x	Output buffers can sink/source up to 16 mA.	71V000	◊ OKI				
	2.5	100	CMOS	2	2				x	x		x		x		71HB000	◊ OKI				
			CMOS	2	2				x	x		x		x		71H000	◊ OKI				
1568	1.9	150	CMOS	1.5	2				x	x		x		x	Output buffers can sink/source up to 16 mA.	72V000	◊ OKI	45			
	2.5	100	CMOS	2	2				x	x		x		x		72HB000	◊ OKI				
			CMOS	2	2				x	x		x		x		72H000	◊ OKI				
2000	1.9	150	CMOS	1.5	2				x	x		x		x	Output buffers can sink/source up to 16 mA.	73V000	◊ OKI				
	2.5	100	CMOS	2	2				x	x		x		x		73HB000	◊ OKI				
			CMOS	2	2				x	x		x		x		73H000	◊ OKI				
2400	1.9	150	CMOS	1.5	2				x	x		x		x	Output buffers can sink/source up to 16 mA.	74V000	◊ OKI	50			
	2.5	100	CMOS	2	2				x	x		x		x		74HB000	◊ OKI				
			CMOS	2	2				x	x		x		x		74H000	◊ OKI				
3289	1.9	150	CMOS	1.5	2				x	x		x		x		79V000	◊ OKI				
	2.5	100	CMOS	2	2				x	x		x		x		79H000	◊ OKI				

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† Military Temperature Range (−55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State						
OKI Semiconductor																		(Cont'd)		
4290	1.9	150	CMOS	1.5	2				x	x			x		x		75V000	◊° OKI	5	
	2.5	100	CMOS	2	2				x	x			x		x		75H000	◊° OKI		
6000	1.9	150	CMOS	1.5	2				x	x			x		x		76V000	◊° OKI		
	2.5	100	CMOS	2	2				x	x			x		x		76H000	◊° OKI		
			CMOS	2	2				x	x			x		x	5.5K GATES + 2 (32x8) RAMS	92H600	◊ OKI		
8118	1.9	150	CMOS	1.5	2				x	x			x		x		77V000	◊° OKI	10	
	2.5	100	CMOS	2	2				x	x			x		x		77H000	◊° OKI		
10008	1.9	150	CMOS	1.5	2				x	x			x		x		78V000	◊° OKI		
	2.5	100	CMOS	2	2				x	x			x		x		78H000	◊° OKI		
			CMOS	2	2				x	x			x		x	8.9K GATES + 5 (32x8) RAMS	92H800	◊ OKI		
Panatech																				
560	1.5 *		CMOS	2	2	1			40	x	x	x					RP5GH05	Panatech	15	
1600	1.5 *		CMOS	2	2	1			72	x	x	x					RP5GH16	Panatech		
2300	1.5 *		CMOS	2	2	1			88	x	x	x					RP5GH23	Panatech		
2900	1.5 *		CMOS	2	2	1			98	x	x	x					RP5GH29	Panatech		
3800	1.5 *		CMOS	2	2	1			108	x	x	x					RP5GH38	Panatech		
5500	1.5 *		CMOS	2	2	1			120	x	x	x					RP5GH55	Panatech		
Performance Semiconductor																				
11000	0.5	250	CMOS	0.8	2	1	x	x	x	x			x		x	CMOS I/O Now TTL I/O Later	P9CG11000	◊ Performance		
Plessey																				
640	1.2	100	CMOS	2	2	1			36	x	x	x		x			CLA5100	Plessey	20	
840	2.1	50	CMOS	3	2				40	x	x	x		x			CLA3100	Plessey		
1232	1.2	100	CMOS	2	2	1			48	x	x	x		x			CLA5200	Plessey		
1440	2.1	50	CMOS	3	2				52	x	x	x		x			CLA3300	Plessey		
2016	1.2	100	CMOS	2	2	1			64	x	x	x		x			CLA5300	Plessey		
2400	2.1	50	CMOS	3	2				64	x	x	x		x			CLA3500	Plessey		
	2.9	40	CMOS	2	2				64	x	x	x		x			CLA4500	Plessey		
3060	1.2	100	CMOS	2	2	1			80	x	x	x		x			CLA5400	Plessey	25	
4200	2.1	50	CMOS	3	2				84	x	x	x		x			CLA3700	◊ Plessey		
	2.9	40	CMOS	2	2				80	x	x	x		x			CLA4700	Plessey		
4404	1.2	100	CMOS	2	2	1			96	x	x	x		x			CLA5500	◊ Plessey	30	
5984	1.2	100	CMOS	2	2	1			112	x	x	x		x			CLA5600	Plessey		
6000	2.1	50	CMOS	3	2	1			108	x	x	x		x			CLA3900	Plessey		
	3.0	100	CMOS						120	x	x	x					CLA4000	Plessey		
7104	1.2	100	CMOS	2	2	1			128	x	x	x		x			CLA5700	Plessey		
8856	1.2	100	CMOS	2	2	1			144	x	x	x		x			CLA5800	Plessey		
10440	1.2	100	CMOS	2	2	1			160	x	x	x		x			CLA5900	Plessey		
Raytheon																				
836	3.5	50	ISL	2	2				48		x	x		x		Gate delay 2.5 ns max with active pull-up	CGA8L48	◊‡ Raytheon	35	
880	1.4	118	CMOS	2	2	1			68	x	x	x		x			RL7080	‡ Raytheon		
1196	3.5	50	ISL	2	2				60		x	x		x		Gate delay 2.5 ns max with active pull-up	CGA12L60	‡ Raytheon		
1443	1.4	118	CMOS	2	2	1			86	x	x	x		x			<b>RL7140</b>	<b>‡ Raytheon (4297)</b>	40	
1620	3.5	50	ISL	2	2				68		x	x		x		Gate delay 2.5 ns max with active pull-up	CGA16L68	◊‡ Raytheon		
1984	3.5	50	ISL	2	2				76		x	x		x		Gate delay 2.5 ns max with active pull-up	CGA20L76	◊‡ Raytheon		
2224	1.4	118	CMOS	2	2	1			106	x	x	x		x			<b>RL7220</b>	<b>‡ Raytheon (4297)</b>		
2376	3.5	50	ISL	2	2				84		x	x		x		Gate delay 2.5 ns max with active pull-up	CGA24L84	◊‡ Raytheon		
3048	4.0	50	CMOS	2	2	2			90		x	x		x			CGA30L90	‡ Raytheon		
3192	1.4	118	CMOS	2	2	1			128	x	x	x		x			<b>RL7320</b>	<b>‡ Raytheon (4297)</b>		
3500	1.7	110	ISL	2	2				124		x	x		x		Gate delay 1.4ns max. with active pull-up	CGA35L12	◊‡ Raytheon	45	
4242	1.4	118	CMOS	2	2	1			150	x	x	x		x			<b>RL7420</b>	<b>‡ Raytheon (4297)</b>		
5000	1.7	110	ISL	2	2				150		x	x		x		Gate delay 1.4ns max. with active pull-up	CGA50L15	‡ Raytheon		
5504	4.0	50	CMOS	2	2	2			118		x	x		x			CGA55L12	‡ Raytheon		
																		(Continued)		

(Continued)

† Military Temperature Range (−55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State				
Raytheon																		(Cont'd)
5670	0.4	250	HCMOS	2	2			90	x		x		x		RVG5	Raytheon (4296)	5	
6072	1.4	118	CMOS	2	2	1		186	x	x	x		x		RL7600	Raytheon (4297)		
7828	4.0	50	CMOS	2	2	2		142		x	x		x		CGA78L14	Raytheon		
8001	0.3	1200	BIP	2	2			120			x	x			CGA40E12	Raytheon (4298)		
8370	1.4	118	CMOS	2	2	1		222	x	x	x		x		RL7840	Raytheon (4297)		
10013	1.4	118	CMOS	2	2	1		232	x	x	x		x		RL71000	Raytheon (4297)		
10360	0.4	250	HCMOS	2	2			118	x		x		x		RVG10	Raytheon (4296)		
14640	0.4	250	HCMOS	2	2			142	x		x		x		RVG15	Raytheon (4296)		
20440	0.4	250	HCMOS	2	2			160	x		x		x		RVG20	Raytheon (4296)		
RCA																		
264	3		CMOS	3	1	1		46	x	x	x	x	x		PA40250	GE/RCA (2659)	10	
440	3		CMOS	3	1	1		62	x	x	x	x	x		PA40450	GE/RCA (2659)		
640	2.5	10	CMOS	4	1	1		102	x	x	x		x		PA61200	GE/RCA (2659)	15	
	3.0	40	CMOS	3	1	1		74	x	x	x		x		PA40650	GE/RCA (2659)		
840	3.0	40	CMOS	3	1	1		86	x	x	x		x		PA40850	GE/RCA (2659)	20	
880	2.5	40	CMOS	3	2	1		74	x	x	x		x		PA50800	GE/RCA (2659)		
1008	3.0	40	CMOS	3	1	1		78	x	x	x		x		PA41000	GE/RCA (2659)	25	
1176	2.5	10	CMOS	4	1	1		102	x	x	x		x		PA60650	GE/RCA (2659)		
	3.0	40	CMOS	3	1	1		86	x	x	x		x		PA41200	GE/RCA (2659)		
1404	2.5	40	CMOS	3	2	1		92	x	x	x		x		PA51400	GE/RCA (2659)	30	
2224	2.5	40	CMOS	3	2	1		114	x	x	x		x		PA52200	GE/RCA (2659)		
3192	2.5	40	CMOS	3	2	1		138	x	x	x		x		PA53200	GE/RCA (2659)	35	
4202	2.5	40	CMOS	3	2	1		156	x	x	x		x		PA54200	GE/RCA (2659)		
6000	2.5	40	CMOS	3	2	1		180	x	x	x		x		PA56000	GE/RCA (2659)		
Ricoh																		
560	1.5		Si-Gate CMOS	2	2			40	x	x	x		x		RP5GH05	Ricoh	25	
1000	1.5		Si-Gate CMOS	2	2			60	x	x	x		x		RP5GH10	Ricoh		
1600	1.5		Si-Gate CMOS	2	2			72	x	x	x		x		RP5GH16	Ricoh	30	
2300	1.5		Si-Gate CMOS	2	2			88	x	x	x		x		RP5GH23	Ricoh		
2900	1.5		Si-Gate CMOS	2	2			98	x	x	x		x		RP5GH29	Ricoh	35	
3800	1.5		Si-Gate CMOS	2	2			108	x	x	x		x		RP5GH38	Ricoh		
5500	1.5		Si-Gate CMOS	2	2			120	x	x	x		x		RP5GH55	Ricoh		
S-MOS Systems																		
413	3.0		CMOS	3	2	1	8	38	x	x	x		x	Silicon gate	SLA5040	S-MOS (4305)	35	
790	3.0		CMOS	3	2	1	8	52	x	x	x		x	Silicon gate	SLA5080	S-MOS (4305)		
820	2.0	60	CMOS	3	2	1	6	54	x	x	x		x	Silicon gate	SLA6080	S-MOS (4305)	40	
1264	3.0		CMOS	3	2	1	8	66	x	x	x		x	Silicon gate	SLA5120	S-MOS (4305)		
1394	2.0	60	CMOS	3	2	1	6	68	x	x	x		x	Silicon gate	SLA6140	S-MOS (4305)	45	
1746	2.0	60	CMOS	3	2	1	6	76	x	x	x		x	Silicon gate	SLA6170	S-MOS (4305)		
2140	3.0		CMOS	3	2	1	8	84	x	x	x		x	Silicon gate	SLA5210	S-MOS (4305)	50	
2667	2.0	60	CMOS	3	2	1	6	94	x	x	x		x	Silicon gate	SLA6270	S-MOS (4305)		
3082	3.0		CMOS	3	2	1	8	100	x	x	x		x	Silicon gate	SLA5300	S-MOS (4305)	55	
3312	2.0	60	CMOS	3	2	1	6	104	x	x	x		x	Silicon gate	SLA6330	S-MOS (4305)		
4342	2.0	60	CMOS	3	2	1	6	120	x	x	x		x	Silicon gate	SLA6430	S-MOS (4305)	60	
5304	0.5		CMOS	1.2	2			78	x		x		x		SLA827S	S-MOS		
6204	2.0	60	CMOS	2	2	1	6	148	x	x	x		x		SLA6620	S-MOS (4305)	65	
9416	0.5		CMOS	1.2	2			104	x		x		x		SLA847S	S-MOS (4305)		
14336	0.5		CMOS	1.2	2			132	x		x		x		SLA872S	S-MOS (4305)	70	
22680	0.5		CMOS	1.2	2			164	x		x		x		SLA8B3S	S-MOS (4305)		
30000	0.5		CMOS	1.2	2			190	x		x		x		SLA8F0S	S-MOS (4305)	75	
38550	0.5		CMOS	1.2	2			218	x		x		x		SLA8J3S	S-MOS (4305)		
Samsung																		
210	4.2	40	CMOS	3	1				x	x	x		Silicon Gate		KG10200	Samsung	80	
400	4.2	40	CMOS	3	1				x	x	x		Silicon Gate		KG10400	Samsung		

(Continued)

(Continued)

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line	
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL							
(Cont'd)																				
Samsung	600	4.2	40	CMOS	3	1				x	x	x				KG10600	Samsung	5		
	840	4.2	40	CMOS	3	1				x	x	x				KG10800	Samsung			
	1190	4.2	40	CMOS	3	1				x	x	x				KG11200	Samsung			
	1600	4.2	40	CMOS	3	1				x	x	x				KG11600	Samsung			
	1980	4.2	40	CMOS	3	1				x	x	x				KG12000	Samsung			
Sharp Electronics	300	2.8	50	CMOS	3				14	x	x	x		x		LZ92300	Sharp	10		
	450	2.8	50	CMOS	3				14	x	x	x		x		LZ92450	Sharp			
	600	2.8	50	CMOS	3				14	x	x	x		x		LZ92600	Sharp			
	630	2.8		CMOS	2.5	2						x		x		LZ92630	Sharp			
	810	2.8	50	CMOS	3				14	x	x	x		x		LZ92800	Sharp			
	1010	2.8	50	CMOS	3				14	x	x	x		x		LZ921000	Sharp			
	1100	2.8		CMOS	2.5	2						x		x		LZ92110	Sharp			
	1500	2.8	50	CMOS	3				14	x	x	x		x		LZ921500	Sharp			
	1600	2.8		CMOS	2.5	2						x		x		LZ921600	Sharp			
	2240	2.8	50	CMOS	3				14	x	x	x		x		LZ922200	Sharp			
	3145	2.8	50	CMOS	3				14	x	x	x		x		LZ923000	Sharp	15		
	4009	2.8	50	CMOS	3				14	x	x	x		x		LZ924000	Sharp			
	5000	2.8	50	CMOS	3				14	x	x	x		x		LZ925000	Sharp			
Signetics	330	16	6 *	CMOS	4	2	2		38	x	x	x		x		SCC0330M	Signetics		20	
	448	16	6 *	CMOS	4	2	2		26	x	x	x		x		SCC0450M	Signetics			
	638	0.5	450	ECL	3		30		28			x		x		ACE600	Signetics (4302)			
	660	0.35	600	ECL			30		28					x		ACE6T00	Signetics (4301)			
		0.45	450	ECL			30		28					x		ACE6LP00	Signetics (4301)	25		
	704	16	6 *	CMOS	4	2	2		38	x	x	x		x		SCC0700M	Signetics			
	878	0.5	450	ECL	3		42		32			x		x		ACE900	Signetics (4302)			
	910	0.35	600	ECL			30		28					x		ACE9T04	Signetics			
		0.45	450	ECL			30		28					X		ACE9LP00	Signetics (4301)			
	1000	0.5	450	ECL	3				96			x		x		320-bit RAM on-chip	ACE1320M	Signetics (4301)	30	
	1106	16	6 *	CMOS	4	2	2		66	x		x		x		SCC1100M	Signetics			
	1192	4.0	25	ISL		2			36			x		x		8A1200	Signetics			
				ISL		2			60			x		x		8A1260	Signetics			
	6.0	20	ISL		2				36			x		x		8A1200	† Signetics			
				ISL		2			60			x		x		8A1260	† Signetics	35		
	1414	0.5	450	ECL	3				96			x		x		ACE1400	Signetics (4302)			
	1450	0.35	600	ECL					128					x		ACE30T00	Signetics (4301, 4303)			
	1472	4.0	25	ISL		2			42			x		x		8A1542	Signetics			
	6.0	20	ISL		2				42			x		x		8A1542	† Signetics			
	1620	4.0	25	ISL		2			64			x		x		8A1664	Signetics	40		
		6.0	20	ISL		2			64			x		x		8A1664	† Signetics			
	1650	0.5	450	ECL					112					x		ACE1320	Signetics (4301)			
	1740	4.0	25	ISL		2			64			x		x		8A1864	Signetics			
		6.0	20	ISL		2			64			x		x		8A1864	† Signetics			
	1750	0.35	600	ECL					96					x		ACE14T00	Signetics (4301)	45		
		0.45	450	ECL					96					x		ACE14LP00	Signetics (4301)			
	2088	4.0	25	ISL		2			76			x		x		8A2176	Signetics			
		6.0	20	ISL		2			76			x		x		8A2176	† Signetics			
	2204	0.5	450	ECL	3				128			x		x		ACE2200	Signetics			
	2700	0.35	600	ECL					128					x		ACE22T00	Signetics (4301)	50		
		0.45	450	ECL					128					x		ACE22LP00	Signetics (4301)			
Siliconix	360	2.4	50	CMOS	3	1			36	x	x	x		x		IS03A	† Siliconix			
		4.4	30	CMOS	5	1			36	x	x	x		x		IS05A	† Siliconix			
(Continued)																				

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

ASICs/CUSTOM

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL						
Siliconix																			(Cont'd)
513	1.7 *		CMOS	2	2		6		48	x	x	x				Si6050	Siliconix	5	
540	2.4	50	CMOS	3μm	1				48	x	x	x		x		IS03B	† Siliconix		
	4.4	30	CMOS	5μm	1				48	x	x	x		x		IS05B	† Siliconix		
720	2.4	50	CMOS	3μm	1				54	x	x	x		x		IS03C	† Siliconix	10	
	4.4	30	CMOS	5μm	1				54	x	x	x		x		IS05C	† Siliconix		
820	1.7 *		CMOS	2	2		6		60	x	x	x				Si6080	◊ Siliconix		
960	2.4	50	CMOS	3μm	1				62	x	x	x		x		IS03D	† Siliconix	15	
	4.4	30	CMOS	5μm	1				62	x	x	x		x		IS05D	† Siliconix		
1148	1.7 *		CMOS	2	2		6		68	x	x	x				Si6110	Siliconix		
1200	2.4	50	CMOS	3μm	1				68	x	x	x		x		IS03E	† Siliconix	20	
	4.4	30	CMOS	5μm	1				68	x	x	x		x		IS05E	† Siliconix		
1394	1.7 *		CMOS	2	2		6		74	x	x	x				Si6140	Siliconix		
1500	2.4	50	CMOS	3μm	1				70	x	x	x		x		IS03F	† Siliconix	25	
	4.4	30	CMOS	5μm	1				70	x	x	x		x		IS05F	† Siliconix		
1746	1.7 *		CMOS	2	2		6		82	x	x	x				Si6170	Siliconix		
1800	2.4	50	CMOS	3μm	1				82	x	x	x		x		IS03G	† Siliconix	30	
	4.4	30	CMOS	5μm	1				82	x	x	x		x		IS05G	† Siliconix		
2240	1.7 *		CMOS	2	2		6		92	x	x	x				Si6220	Siliconix		
2400	2.4	50	CMOS	3μm	1				82	x	x	x		x		IS03H	† Siliconix	35	
	4.4	30	CMOS	5μm	1				82	x	x	x		x		IS05H	† Siliconix		
2667	1.7 *		CMOS	2	2		6		100	x	x	x				Si6270	Siliconix		
3312	1.7 *		CMOS	2	2		6		110	x	x	x				Si6330	◊ Siliconix	40	
4342	1.7 *		CMOS	2	2		6		126	x	x	x				Si6430	Siliconix		
6206	1.7 *		CMOS	2	2		8		154	x	x	x				Si6620	Siliconix		
Thomson-Mostek																			
1120	1.5	40	HCMOS	2	2				56	x	x	x			x	TSGB01000	Thomson	45	
2128	1.5	40	HCMOS	2	2				76	x	x	x			x	TSGB02000	Thomson		
3264	1.5	40	HCMOS	2	2				96	x	x	x			x	TSGB03000	Thomson		
4256	1.5	40	HCMOS	2	2				108	x	x	x			x	TSGB04000	Thomson	50	
5880	1.5	40	HCMOS	2	2				132	x	x	x			x	TSGB06000	Thomson		
7872	1.5	40	HCMOS	2	2				168	x	x	x			x	TSGB08000	Thomson		
Thomson-Mostek																			
1120	1.0	65	HCMOS	1.2	2				56	x	x	x			x	TSGC01000	◊ Thomson (4322)	55	
2128	1.0	65	HCMOS	1.2	2				76	x	x	x			x	TSGC02000	Thomson (4322)		
3264	1.0	65	HCMOS	1.2	2				96	x	x	x			x	TSGC03000	Thomson (4322)		
4256	1.0	65	HCMOS	1.2	2				108	x	x	x			x	TSGC04000	Thomson (4322)	60	
5880	1.0	65	HCMOS	1.2	2				132	x	x	x			x	TSGC06000	Thomson (4322)		
7872	1.0	65	HCMOS	1.2	2				168	x	x	x			x	TSGC08000	Thomson (4322)		
9776	1.0	65	HCMOS	1.2	2				192	x	x	x			x	TSGC10000	Thomson (4322)	65	
	1.5	40	HCMOS	2	2				192	x	x	x			x	TSGB10000	Thomson		
Thomson-Mostek																			
8000	0.3 *		HCMOS	1.2	2				76	x		x			x	ISB12008	Thomson	70	
11520	0.3 *		HCMOS	1.2	2				92	x		x			x	ISB12011	Thomson		
15680	0.3 *		HCMOS	1.2	2				108	x		x			x	ISB12015	Thomson		
20480	0.3 *		HCMOS	1.2	2				120	x		x			x	ISB12020	Thomson	75	
25920	0.3 *		HCMOS	1.2	2				136	x		x			x	ISB12025	Thomson		
38720	0.3 *		HCMOS	1.2	2				164	x		x			x	ISB12038	Thomson		
54080	0.3 *		HCMOS	1.2	2				200	x		x			x	ISB12054	Thomson	80	
76880	0.3 *		HCMOS	1.2	2				232	x		x			x	ISB12076	◊ Thomson		
103680	0.3 *		HCMOS	1.2	2				256	x		x			x	ISB12103	Thomson		
128000	0.3 *		HCMOS	1.2	2				256	x		x			x	ISB12128	Thomson	85	
TLSI																			
300	10	15	CMOS	5μm	1	1	1		37	x	x	x				TA1	† TLSI	90	
400	10	15	CMOS	5μm	1	1	1		43	x	x	x			x	TA2	† TLSI		
540	4.0	36	CMOS	3μm	1	1			38	x	x	x			x	TA500	† TLSI		
	10	15	CMOS	5μm	1	1	1		49	x	x	x			x	TA3	† TLSI	95	
770	10	15	CMOS	5μm	1	1	1		59	x	x	x			x	TA4	† TLSI		
1000	10	15	CMOS	5μm	1	1	1		67	x	x	x			x	TA5	† TLSI		
1020	4.0	36	CMOS	3μm	1	1			50	x	x	x			x	TA1000	◊† TLSI	100	
1024	3.0	40	CMOS	3μm	2	1			62	x	x	x			x	TA1000D	◊† TLSI		
1260	10	15	CMOS	5μm	1	1	1		75	x	x	x			x	TA6	† TLSI		
1500	4.0	36	CMOS	3μm	1	1			62	x	x	x			x	TA1500	◊† TLSI	105	
(Continued)																			

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‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Comments	Device	Source	Line
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State						
TSLI																			(Cont'd)	
2025	4.0	36	CMOS	3	1	1			72	x	x	x		x		TA2000	† TSLI	5		
2070	3.0	40	CMOS	3	2	1			82	x	x	x		x		TA2000D	† TSLI			
2500	4.0	36	CMOS	3	1	1			82	x	x	x		x		TA2500	† TSLI			
3080	3.0	40	CMOS	3	2	1			100	x	x	x		x		TA3000D	† TSLI			
4012	3.0	40	CMOS	3	2	1			118	x	x	x		x		TA4000D	† TSLI			
Toshiba																				
540	1.5 *	100	CMOS		2				52	x	x	x				TC17G005	Toshiba	10		
880	1.5 *	100	CMOS		2				68	x	x	x				TC17G008	Toshiba			
	2.5 *	5.0	CMOS		2					x	x	x				TC15G008	Toshiba			
1400	1.5 *	100	CMOS		2				86	x	x	x				TC17G14	Toshiba			
	2.5 *	5.0	CMOS		2					x	x	x				TC15G014	Toshiba			
2200	1.5 *	100	CMOS		2				106	x	x	x				TC17G032	Toshiba	15		
	2.5 *	5.0	CMOS		2					x	x	x				TC15G022	Toshiba			
3200	1 *	120	CMOS	1.5	2				128	x	x	x		x		TC19G032	Toshiba			
	2.5 *	5.0	CMOS		2					x	x	x				TC15G032	Toshiba			
4200	1 *	120	CMOS	1.5	2				150	x	x	x		x		TC19G042	Toshiba			
	1.5 *	100	CMOS		2				150	x	x	x				TC17G042	Toshiba	20		
	2.5 *	5.0	CMOS		2					x	x	x				TC15G042	Toshiba			
5330	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G05	Toshiba			
6000	1 *	120	CMOS	1.5	2				186	x	x	x		x		TC19G060	Toshiba			
	1.5 *	100	CMOS		2				186	x	x	x				TC17G064	Toshiba			
	2.5 *	5.0	CMOS		2					x	x	x				TC15G060	◊ Toshiba			
8000	1 *	120	CMOS	1.5	2				222	x	x	x		x		TC19G080	Toshiba	25		
	1.5 *	100	CMOS		2				222	x	x	x				TC17G080	Toshiba			
8262	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G08	Toshiba			
10000	1 *	120	CMOS	1.5	2				232	x	x	x		x		TC19G100	Toshiba			
	1.5 *	100	CMOS		2				232	x	x	x				TC17G100	◊ Toshiba			
11400	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G11	Toshiba	30		
17464	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G17	Toshiba			
25920	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G26	Toshiba			
37932	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G38	Toshiba			
50904	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G51	Toshiba			
74970	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110G75	Toshiba			
100182	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110GA0	Toshiba			
129042	0.7	120	HC <sup>2</sup> MOS	1.5	2					x	x	x	x		Programmable I/O cells with slew rate control.	TC110GC9	Toshiba			
TriQuint Semiconductor																				
3000	0.12	1000	GaAs	1	2				64	x	x	x	x			TQ3000	◊ TriQuint (3309)	35		
United Microelectronics (UMC)																				
300	4.5	40	CMOS, Si-Gate	3	2				36	x		x				UM1203	UMC (4329)	(Continued)		
600	4.5	40	CMOS, Si-Gate	3	2				48	x		x				UM1206	UMC (4329)			

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

Bold face indicates additional data is provided on the page noted.



## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (µm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility					Three State	Comments	Device	Source	Line	
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL							
United Microelectronics (UMC)																			(Cont'd)	
900	4.5	40	CMOS, Si-Gate 3	2					58	x		x				UM1209	UMC	(4239)	5	
1100	4.5	40	CMOS, Si-Gate 3	2					65	x		x				UM1211	UMC	(4329)		
1320	2.5		CMOS, Si-Gate 2	2					50	x		x				UM1313	UMC	(4330)		
1820	2.5		CMOS, Si-Gate 2	2					66	x		x				UM1318	UMC	(4330)		
2240	2.5		CMOS, Si-Gate 2	2					80	x		x				UM1322	UMC	(4330)		
3060	2.5		CMOS, Si-Gate 2	2					92	x		x				UM1330	UMC	(4330)		
United Technologies Microelectronics Center																				
1000	2.2		CMOS	3.0	2				38	x	x	x		x		UT040B	UTMC	(4331)	10	
			CMOS	3.0	2				36	x	x	x		x	Radiation Hardened	UT040BR	± UTMC	(4331)		
2400	2.2		CMOS	3.0	2				64	x	x	x		x		UT068B	UTMC	(4331)		
			CMOS	3.0	2				60	x	x	x		x	Radiation Hardened	UT068BR	± UTMC	(4331)		
3200	2.2		CMOS	3.0	2				80	x	x	x		x		UT084B	UTMC	(4331)		
			CMOS	3.0	2				76	x	x	x		x	Radiation Hardened	UT084BR	± UTMC	(4331)		
3400	1.0		CMOS	1.5	2				96	x	x	x		x		UT116D	UTMC	(4331)	15	
5100	2.2		CMOS	3.0	2				116	x	x	x		x		UT124B	UTMC	(4331)		
			CMOS	3.0	2				112	x	x	x		x	Radiation Hardened	UT124BR	± UTMC	(4331)		
6000	1.0		CMOS	1.5	2				136	x	x	x		x		UT160D	UTMC	(4331)		
7600	2.2		CMOS	3.0	2				136	x	x	x		x		UT144B	UTMC	(4331)		
			CMOS	3.0	2				132	x	x	x		x	Radiation Hardened	UT144BR	± UTMC	(4331)		
7800	1.0		CMOS	1.5	2				156	x	x	x		x		UT180D	UTMC	(4331)	20	
11000	1.0		CMOS	1.5	2				188	x	x	x		x		UT212D	UTMC	(4331)		
Universal Semiconductor																				
99	0.9	50	CMOS	2	1	1			18	x	x	x		x	24 pads	IS02J	Universal			
	2.5	30	CMOS	3	1	1			18	x	x	x		x	24 pads	IS03J	Universal			
180	0.9	50	CMOS	2	1	1			30	x	x	x		x	40 pads	IS02I	Universal			
	2.5	30	CMOS	3	1	1			30	x	x	x		x	40 pads	IS03I	Universal			
360	0.9	50	CMOS	2	1	1			36	x	x	x		x	46 pads	IS02A	Universal			
	2.4	30	CMOS	3	1	1			36	x	x	x		x	46 pads	IS03A	† Universal			
	4.4	20	CMOS	5	1	1			36	x	x	x		x	46 pads	IS05A	† Universal			
540	0.9	50	CMOS	2	1	1			48	x	x	x		x	58 pads	IS02B	Universal			
	2.4	30	CMOS	3	1	1			48	x	x	x		x	58 pads	IS03B	† Universal			
	4.4	20	CMOS	5	1	1			48	x	x	x		x	58 pads	IS05B	† Universal			
720	0.9	50	CMOS	2	1	1			54	x	x	x		x	64 pads	IS02C	Universal			
	2.4	30	CMOS	3	1	1			54	x	x	x		x	64 pads	IS03C	† Universal			
	4.4	20	CMOS	5	1	1			54	x	x	x		x	64 pads	IS05C	† Universal			
960	0.9	50	CMOS	2	1	1			62	x	x	x		x	72 pads	IS02D	Universal			
	2.4	30	CMOS	3	1	1			62	x	x	x		x	72 pads	IS03D	† Universal			
	4.4	20	CMOS	5	1	1			62	x	x	x		x	72 pads	IS05D	† Universal			
1200	0.9	50	CMOS	2	1	1			68	x	x	x		x	78 pads	IS02E	Universal			
	2.4	30	CMOS	3	1	1			68	x	x	x		x	78 pads	IS03E	† Universal			
	4.4	20	CMOS	5	1	1			68	x	x	x		x	78 pads	IS05E	† Universal			
1500	0.9	50	CMOS	2	1	1			76	x	x	x		x	86 pads	IS02F	Universal			
	2.4	30	CMOS	3	1	1			70	x	x	x		x	86 pads	IS03F	† Universal			
	4.4	20	CMOS	5	1	1			70	x	x	x		x	78 pads	IS05F	† Universal			
1800	0.9	50	CMOS	2	1	1			82	x	x	x		x	92 pads	IS02G	Universal			
	2.4	30	CMOS	3	1	1			82	x	x	x		x	92 pads	IS03G	† Universal			
	4.4	20	CMOS	5	1	1			82	x	x	x		x	92 pads	IS05G	† Universal			
2400	0.9	50	CMOS	2	1	1			90	x	x	x		x	100 pads	IS02H	Universal			
	2.4	30	CMOS	3	1	1			82	x	x	x		x	100 pads	IS03H	† Universal			
	4.4	20	CMOS	5	1	1			82	x	x	x		x	100 pads	IS05H	† Universal			

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

\*Macrocell

◇ Available in Surface Mount Package

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## ASIC/CUSTOM—Gate Arrays (Cont'd)

Mfr/ Equiv. 2-Input Gates	max Gate Delay (ns)	Toggle Freq (MHz)	Device Process Tech.	Geometry (μm)	Metal	Poly	Input/Output Cells			Input/Output Compatibility							Comments	Device	Source	Line		
							Input Only	Out- put Only	Un- com- mitted	C- MOS	TTL- LS	TTL	ECL	Three State								
VLSI Technology																						
864	2.0	—	CMOS	2	2	1	23		38	x	x	x		x		VGC0900	VLSI Tech (4665)	5				
1188	2.0	—	CMOS	2	2	1	27		46	x	x	x		x		VGC1200	VLSI Tech (4665)					
1242	2.5	—	CMOS	2μm	2	1	27		46	x	x	x		x		VGC0500	† VLSI Tech (4665)					
1932	2.0	—	CMOS	2	2	1	35		58	x	x	x		x		VGC1900	VLSI Tech (4665)					
2592	2.5	—	CMOS	2μm	2	1	39		70	x	x	x		x		VGC2400	† VLSI Tech (4665)					
3240	2.0	—	CMOS	2	2	1	43		78	x	x	x		x		VGC3200	VLSI Tech (4665)					
4020	2.5	—	CMOS	2μm	2	1	47		86	x	x	x		x		VGC4000	◊† VLSI Tech (4665)					
6000	2.5	—	CMOS	2μm	2	1	55		106	x	x	x		x		VGC6000	† VLSI Tech (4665)					
Xilinx																						
1200	10	70	CMOS	1.2	2	1				x		x		x	User-programmable	XC2064-70	Xilinx (4346)	10				
1800	10	70	CMOS	1.2	2	1				x		x		x	User-programmable	XC2018-70	Xilinx (4346)					
AT&T																						
1000	0.9	200	ECL/EFL				96	48			x		x			TE1000	‡ AT&T (4211)	15				
2000	0.9	200	ECL/EFL				84	84			x		x			TE2000	AT&T (4211)					
3000	0.9	200	ECL/EFL				168	84			x		x			TE3000	‡ AT&T (4211)					
Raytheon																						
7128	0.3 *	600	ECL						180			x	x	x		CGA70E18	‡ Raytheon (4298)					

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‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## ASIC/CUSTOM—Linear & Linear/Digital Arrays

Manufacturer	Technology	Total Bonding Pads	Linear Dedicated Op Amps, A/D, etc.	Total Other Lin. Components	Digital Equiv. 2-Input Gates	Gate Delay ns @ V	Uncommitted Transistors NPN	PNP	Number Capacitors	Supply Voltage, V	Comments	Device	Source	Line
Advanced Micro Devices	BIP/ECL	92			1800	1.2	5340			-7/-8	ECL/TTL I/O	AMMPA1850	AMD	
		150			5228	0.9	15160			-7/-7	ECL/TTL I/O	AMMPA3550	AMD	
		154			4988	0.9	12768			-7	ECL only	AMMPA3500B	AMD	
		158			3718	0.9	9776			-7	ECL only, 1152-bits of ECL RAM	AMMPA3525	AMD	
AT&T	BIP	30		142			13	15	3	90	Complementary npn and pnp	ALA300	AT&T	(4208)
		32		528			52	60	12	90	Complementary npn and pnp	ALA301	AT&T	(4208)
		44		1260			133	85	22	12	Complementary npn and pnp; ft = 2 to 4 GHz	ALA200	AT&T	(4207)
Barvon Research	Bi-CMOS		1	2292	400	7	104	76		15/6	4 to 16 decades, combination bipolar and CMOS	BC3G02	Barvon	
		58	—	585	250	7	92	52		15/6	Combination bipolar and CMOS	BC3G01	Barvon	
Cherry Semiconductor	BIP	16		333			60	25		20	Flip-chip	CS2800	Cherry	10
		18		187			48	15		20		CS2000E	Cherry	
				325			60	18		20		CS2500G	Cherry	
		22		299			61	24		20	Photosensor on-chip	CS3500	Cherry	
				479			88	36		20	Enhanced CS31000	CS3000X	Cherry	
				479			88	36		20	Micropower	CS3100	Cherry	
				479			88	36		20		CS3200L	Cherry	
		23		522						50	Programmable Bandgap Reference	CS8000	Cherry	
		24		437			96	36		20		CS3000F	Cherry	
		25		533			142	26		15	LSTTL	CS7600	Cherry	
				695			123	52		20		CS3600	Cherry	
		28		801			153	56		20		CS4000	Cherry	
I <sup>2</sup> L		26		490	64	50				12	143 NPN/PNP Transistors	CS1100	Cherry	
		30										CS1500	Cherry	
		40		300	256					12	69 NPN/PNP transistors, 18 input/output cells	CS1400	Cherry	
Custom Arrays Corp.	BIP	14		96			27	14	1	20	High-Current NPN Transistors	MMA	CustomArrays	25
		18		175			46	20	1	20	High-Current NPN Transistors	MMB	CustomArrays	
		20		254			60	30	1	20	High-Current NPN Transistors	MMC	CustomArrays	
		25		366			78	36	2	20	High-Current NPN Transistors	MMD	CustomArrays	
		28		479			90	46	2	20	High-Current NPN Transistors	MME	CustomArrays	
		30		627			116	60	3	20	High-Current NPN Transistors	MMF	CustomArrays	
		38		775			134	70	3	20	High-Current NPN Transistors	MMG	CustomArrays	
		42		925			256	84	3	20	High-Current NPN Transistors	MMH	CustomArrays	
		46		1073			178	98	3	20	High-Current NPN Transistors	MMJ	CustomArrays	
Custom Integrated Circuits	BIP	10		38			25	8	33	20	1 cell, often used in multiples, PNPs have 4 collectors	MSA1	CIC	
		38		124			84	40	124	20	1 cell can be used in multiples	MSB1	CIC	
		50		800			561	164	725	20	15 cells	MSA15	CIC	
		56		148			168	80	148	20	2 cells	MSB2	CIC	
ECI Semiconductor	BIP	14		107			23	8		20		S20C	ECISemi	
		18		140			38	12		20		S20J	ECISemi	
				225			71	22		20		S20H	ECISemi	
				227			59	18		20		S20G	ECISemi	
		24		277			78	24		20		S20L	ECISemi	
				387			94	41		20		S20F	ECISemi	
		28		562			150	52		20		S20M	ECISemi	
CMOS		22			125	15@5				15	1 Metal	ECIML50	ECISemi	45
		32			290	15@5				15	1 Metal	ECIMCA	ECISemi	
		38			405	15@5				15	1 Metal	ECIMCB	ECISemi	
		46			540	15@5				15	1 Metal	ECIMCC	ECISemi	
		53			560	15@5				15	1 Metal, Dedicated Flip-Flops.	ECIMCD	ECISemi	
		69			1280	15@5				15	1 Metal, Dedicated Flip-Flops.	ECIFE600	ECISemi	
		80			1280	15@5				15	1 Metal, Dedicated Flip-Flops.	ECIFE500	ECISemi	

<sup>1</sup> Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

## ASIC/CUSTOM—Linear &amp; Linear/Digital Arrays (Cont'd)

Manufacturer	Technology	Linear Total Bonding Pads	Dedicated Op Amps, A/D, etc.	Total Other Lin. Components	Digital Equiv. 2-Input Gates	Gate Delay ns @ V	Uncommitted Transistors NPN	PNP	Number Capacitors	Supply Voltage, V	Comments	Device	Source	Line
Exar	BIP	14		110			23	8		20	6 Shottky diodes	XR-C100	◊ Exar	5
		16		209			50	16		36		XR-D100	◊ Exar	
				260			60	18		20	15 Shottky diodes	XR-A100	◊ Exar	
				300			69	12		20	16 Shottky diodes	XR-B100	◊ Exar	
		18		200			48	15		20		XR-E100	◊ Exar	
				230			34	16		75	High voltage array	XR-X100	◊ Exar	
				260			38	12		20		XR-J100	◊ Exar	
				309			60	18		20		XR-G100	◊ Exar	
				401			72	22		20		XR-H100	◊ Exar	
		24					95	43		36	4 JFETs, ion implant resistors	XR-U100	Exar	10
				251			80	26		20		XR-L100	◊ Exar	
				472			97	36		20		XR-F100	◊ Exar	
	28			127			102	62		20	Ion implant resistors, low noise	XR-CA600	Exar	15
							127	127	28	26	Transistors are programmable as NPN or PNP	BETA100	Exar	
				539			144	64	8	36	8 JFETs, ion implant resistors	XR-V100	◊ Exar	
				812			148	56		20		XR-M100	Exar	
	38			218			218	218	38	26	Transistors are programmable as NPN or PNP	BETA180	Exar	
	40			901			224	70		36	8 JFETs, ion implant resistors	XR-W100	Exar	
	48			290			290	290	48	26	Transistors are programmable as NPN or PNP	BETA240	◊ Exar	
I <sup>2</sup> L	40			401	256	50/20 μA	45	12		7	18 I/O cells	XR400	Exar	20
Ferranti Interdesign	CML	18		530	30	230	199		2	1-5.5	Gate Current 2.4μA	ULA03G	Interdesign	25
		24		1012	98	230	441		2	1-5.5	Gate Current 2.4μA	ULA1G	Interdesign	
		28		1408	162	230	649		2	1-5.5	Gate Current 2.4μA	ULA2G	Interdesign	
		32		1868	242	230	897		2	1-5.5	Gate Current 2.4μA	ULA3G	Interdesign	
		36		2392	338	230	1185		2	1-5.5	Gate Current 2.4μA	ULA4G	Interdesign	
		40		2980	450	230	1329		2	1-5.5	Gate Current 2.4μA	ULA5G	Interdesign	
		44		3632	578	230	1977		2	1-5.5	Gate Current 2.4μA	ULA6G	◊ Interdesign	
	CMOS	30		602			155	148	84	15		MLB	Interdesign	
BIP	15			162			27	14	1	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMA	Interdesign	30
	19			264			48	20	1	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMB	Interdesign	
	21			378			60	30	1	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMC	Interdesign	
BIP	26			285	128	40 to 500	150		2	16.5	All arrays have dedicated bandgap reference	ULA 1P	◊ Interdesign	35
	27			522			80	36	2	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMD	Interdesign	
	30			663			87	46	2	20	Repeat cell structure to facilitate macros and design transfer between arrays	MME	Interdesign	
	33			867			116	60	3	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMF	Interdesign	
	34			405	338	40 to 500	214		2	16.5	All arrays have dedicated bandgap reference	ULA 3P	◊ Interdesign	
	41			1058			134	70	3	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMG	Interdesign	

(Continued)

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Linear & Linear/Digital Arrays (Cont'd)

Manufacturer	Technology	Total Bonding Pads	Linear Dedicated Op Amps, A/D, etc.	Total Other Lin. Components	Digital Equiv. 2-Input Gates	Gate Delay ns @ V	Uncommitted Transistors NPN	PNP	Number Capacitors	Supply Voltage, V	Comments	Device	Source	Line
Ferranti-Interdesign BIP														
		42		525	578	40 to 500	278		2	16.5	All arrays have dedicated bandgap reference	ULA 6P	Interdesign	(Cont'd)
		49		1455			178	98	3	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMJ	Interdesign	
		50		645	882	40 to 500	342		2	16.5	All arrays have dedicated bandgap reference	ULA 9P	Interdesign	
		54		705	1152	40 to 500	374		2	16.5	All arrays have dedicated bandgap reference	ULA 11P	Interdesign	
		45		1264			164	84	3	20	Repeat cell structure to facilitate macros and design transfer between arrays	MMH	Interdesign	5
Gennum Corporation BIP		14		106			27	9	3	20	Component Array	LA204	Gennum (4239)	
		18		177			48	14	3	20	Component Array	LA202	Gennum (4239)	
		24		224			70	20	4	20	Modula Series Library	LA253	Gennum (4239)	
				301			85	26	3	20	Component Array	LA201	Gennum (4239)	
		32		380			116	34	4	20	Modula Series Library	LA252	Gennum (4239)	10
		40		483			152	49	4	20	Modula Series Library	LA251	Gennum (4239)	
Holt CMOS		52	4	877	45		24		145	0.3–18	Breadboard component array, SCF, Wilson current source, 271 PFET, 211 NFET	HI5100	Holt	
Interconics BIP		14		109			62	8	0	20		IMC20C	Interconics	
		16		194			50	16	0	40		IMC40D	Interconics	
				245			60	28	0	40		IMC40A	Interconics	15
				259			59	18	0	20		IMC20A	Interconics	
		18		170			38	12	0	20		IMC20J	Interconics	
				187			48	15	0	20		IMC20E	Interconics	
				308			60	18	0	20		IMC20G	Interconics	20
				382			72	22	0	20		IMC20H	Interconics	
		20		218			62	10	0	40		IMC40B	Interconics	
		24		301			69	12	0	20		IMC20B	Interconics	
				416			80	26	0	20		IMC20L	Interconics	
				437			96	36	0	20		IMC20F	Interconics	
				464			96	50	0	20		IMC20W	Interconics	25
		28		812			149	56	0	20		IMC20M	Interconics	
Interdesign BIP		14		110			22	8		20		MOC	Interdesign	
		16		194			50	16		36		MOD	Interdesign	
				260			59	18		20		MOA	Interdesign	
		18		170			38	12		20		MOJ	Interdesign	30
				187			48	15		20		MOE	Interdesign	
				314			56	22		20		MOQ	Interdesign	
				382			72	22		20		MOH	Interdesign	
		20		310			60	18		20		MOG	Interdesign	
		24								20		MOR	Interdesign	35
				300			69	12		20		MOB	Interdesign	
				416			80	26		20		MOL	Interdesign	
				437			96	36		20		MOF	Interdesign	
				571			72	57		20		MOP	Interdesign	
		28		812			141	56		20		MOM	Interdesign	40
		40		1072			182	70		20		MON	Interdesign	
CMOS		42		930	199		414	398	84	15	16 dedicated flip-flops, switched capacitor array	MLA	Interdesign	

<sup>1</sup> Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

## ASIC/CUSTOM—Linear &amp; Linear/Digital Arrays (Cont'd)

Manufacturer	Technology	Total Bonding Pads	Linear Dedicated Op Amps, A/D, etc.	Total Other Lin. Components	Digital Equiv. 2-Input Gates	Gate Delay ns @ V	Uncommitted Transistors NPN PNP	Number Capacitors	Supply Voltage, V	Comments	Device	Source	Line
MCE Semiconductor	BIP	14		109			16 18	2	20	Power array	MCEP20A	MCE	5
						22 8		20	MCEA20C		MCE		
				109		62 8		20	MCEA20CS		MCE		
	16			194			100 16		40		MCEA40D	MCE	10
				194			50 16		40		MCEA40DS	MCE	
				245			60 28		40		MCEA40AS	MCE	
				259			59 18		20		MCEA20A	MCE	
				259			59 18		20		MCEA20AS	MCE	
	18			170			38 12		20		MCEA20J	MCE	15
				170			38 12		20		MCEA20JS	MCE	
				187			48 15		20		MCEA20E	MCE	
				187			48 15		20		MCEA20ES	MCE	
			308			60 18		20		MCEA20G	MCE		
			308			60 18		20		MCEA20GS	MCE		
			382			72 22		20		MCEA20H	MCE		
			382			74 22		20		MCEA20HS	MCE		
20		—			27 12		40	5 op amps, power array	MCEP40A	MCE	20		
		218			62 10		40		MCEA40BS	MCE			
24			301			69 12		20		MCEA20B	MCE	25	
			301			69 12		20		MCEA20BS	MCE		
			416			80 26		20		MCEA20L	MCE		
			416			80 26		20		MCEA20LS	MCE		
			437			96 36		20		MCEA20F	MCE		
			437			96 36		20		MCEA20FS	MCE		
28			464			96 36		20		MCEA20WS	MCE	30	
			812			149 56		20		MCEA20M	MCE		
CMOS	18		2								MCEA20MS	MCE	35
			2					2	8	2 op amps, dedicated logic	MGA255	MCE	
			2			8@15		2	12	2 op amps, dedicated logic	MGA255	MCE	
Micrel	CMOS/DMOS	78	4	180	200	200		2	20–100	CMOS/DMOS High Voltage Array.	MPD8020	Micrel (4276)	
Micro Linear	BIP	18		188			38 12		20		FB900J	MicroLinear	35
				327			60 18		20		FB900G	MicroLinear	
				400			72 22		20		FB900H	MicroLinear	
	24		440			80 26		20		FB900L	MicroLinear	40	
			461			96 36		20		FB900F	MicroLinear		
			926			178 78	8	12	ft ± 1GHz	FB3610	♦† MicroLinear		
	28	2	993			173 79	7	12	ft = 1 GHz	FB308	MicroLinear	45	
			840			149 56		20		FB900H	MicroLinear		
			1643	50	2	330 82	14	12	ft ± 1GHz	FB324	♦† MicroLinear		
	32	2	1426			238 138	10	12	ft = 1 GHz	FB312	MicroLinear	50	
			564			116 36	4	40	ft ± 1GHz	FB3410	♦† MicroLinear		
			1348			268 124	12	12	ft ± 1GHz	FB3620	♦† MicroLinear		
42	2	1168	142	4	188 108	.8	12	ft = 1 GHz	FB330	MicroLinear	55		
	2	1847			307 181	13	12	ft = 1 GHz	FB315	MicroLinear			
	46	2392			424 232	24	12	ft ± 1GHz	FB3630	♦† MicroLinear			
NCM Corp.	Planar	24					100 39		25		NCM5001Z	NCM	60
		28					149 52		25		NCM5002Z	NCM	
Plessey Semiconductor	BIP	24		278			81 28		24		BAA1000	Plessey	65
				572			159 58		24		BAA2000	Plessey	
Polycore	BIP	9		30			9 3		80	1A. Darlington and 1A Diode	MX21	Polycore	70
		40		280			100 25		12	Ft = 1 GHz	MX60	Polycore	
Polycore Electronics													
Gold Doped Bipolar		24			32	10/5	60 8	0	5 to 24	RTL, DTL, TTL Emulation	MX40	Polycore	

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

♦ Available in Surface Mount Package

Bold face indicates additional data is provided on the page noted.



## ASIC/CUSTOM—Linear & Linear/Digital Arrays (Cont'd)

Manufacturer	Total Bonding Pads	Linear Dedicated Op Amps, A/D, etc.	Total Other Lin. Components	Digital Equiv. 2-Input Gates	Gate Delay ns @ V	Uncommitted Transistors	Number Capacitors	Supply Voltage, V	Comments	Device	Source	Line
Raytheon BIP	24	12	170			49 39	19 16	2-32 ± 18	Four 100 mA NPN transistors, 148 aluminum feedthroughs, 176 thin-film resistors, dual-layer metal.	RLA80 RLA120 RLA160	Raytheon (2984, 4299) Raytheon (2984, 4299) Raytheon (2984, 4299)	
	44		312			46	10	2-32				
Reticon NMOS	60	31					2500	± 11	14 filter sections, 3 extra op amps, 20 state cells, min. package size 24 pins, switched capacitor filter array	RU5626	EG&G-Reticon	
S-MOS Systems Inc. CMOS	48 80 112 136 158 178 196			513 2232 3432 4900 6210 8000 9250	2.0 1.0 1.0 1.0 1.0 1.0 1.0			7.0 7.0 7.0 7.0 7.0 7.0 7.0		SLA6050 SLA7220 SLA7340 SLA7490 SLA7620 SLA7800 SLA7930	S-MOS (4305) S-MOS (4305) S-MOS (4305) S-MOS (4305) S-MOS (4305) S-MOS (4305) S-MOS	5 10
Silicon Systems Inc. CMOS	28	24					396	15	12 op amps, 210 switches, 4 buffers, 8 flip-flops, switched capacitor filter array	SCA6	SiliconSys	
Tektronix BIP	22 24 28 36 66 70		324 626 996 966 1356 2136			78 150 198 214 294 524	38 82 48 110 174 240	10 24 16 20 16 72	QuickChip 2 with Schottky's Array, ft = 6.5 GHz Array, ft = 2.4 GHz Array, ft = 6.5 GHz Array, ft = 6.5 GHz	QuickChip 2K-30 QuickChip 2S QuickChip 3 QuickChip 2 QuickChip 4 QuickChip 2L	Tektronix Tektronix Tektronix Tektronix Tektronix Tektronix	15
Thomson-Mostek BIP	40		906			188	28	4	15	TSK09 Series	Thomson	
VTC Inc. Bipolar	20 28 40 50 52 68		206 382 444 1400 872 984 200 1160 1796			80 182 164 550 382 354 656	24 48 24 36 126 54 96	16 32 8 18 64 18 32	NPN ft = 6 GHz, PNP ft = 500 MHz. Two-micron geometry. NPN ft = 1 GHz, PNP ft = 80 MHz. ± 5, ± 12 Two-micron geometry. Three-micron geometry. 6 GHz Cell Library Three-micron geometry.	VJ910 VJ930 VJ830 VJ800 VJ960 VJ860 VL3000 VJ970 VJ890	VTC VTC VTC VTC (4343) VTC VTC VTC (4336) VTC VTC	20 25

<sup>1</sup> Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

## ASIC/CUSTOM—Programmable Logic

Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line
CMOS, E <sup>2</sup> Programmable	25 nsF	TS	5	18CP210	Gould		Electrically Erasable Programmable Logic, CMOS, 18						
				18CV8	Gould		Inputs, 8 Outputs, 74 Product Terms,						
				22CP210	Gould		Programmable AND, Fixed OR						
				22CV10	Gould		40 nsF TS	5			PEEL18CV8-40	ICT (4259, 4266)	
							50 nsF TS	5			PEEL18CV8-50	ICT (4259, 4266)	35
CMOS Field Programmable Array Logic for Bus Interface Applications, Integrated 24 mA and 48 mA Drivers.	25 nsF	TS	-0.5 to 7	PLX448-25C	PLXTechnology	5	Electrically Erasable Programmable Logic, CMOS, 20						
				PLX448-25M	† PLXTechnology		Inputs, 10 Outputs, 92 Product Terms,						
	35 nsF	TS	-0.5 to 7	PLX448-35C	PLXTechnology		Programmable AND, Fixed OR, ' ' Zero Power						
				PLX448-35M	† PLXTechnology		Mode'' (100μA)						
							15 nsF TS	5			PEEL20CG10Z	ICT (4259)	
							25 nsF TS	5			PEEL20CG10-25	ICT (4259)	
	45 nsF	TS	-0.5 to 7	PLX448-45C	PLXTechnology	10	35 nsF TS	5			PEEL20CG10-35	ICT (4259)	
				PLX448-45M	† PLXTechnology								
CMOS Programmable Array Logic	35 nsF	TS	5	20RA10Z	SEEQ (2991)		Electrically Erasable Programmable Logic, CMOS, 22						
CMOS Programmable Electrically Erasable Logic (PEEL), 8 Inputs	40 nsF	TS	5	PEEL253	ICT (4259, 4264)		Inputs, 10 Outputs, 132 Product Terms,						
CMOS Programmable Electrically Erasable Logic, 12 Inputs	40 nsF	TS	5	PEEL273	ICT (4259, 4262)		Programmable AND, Fixed OR						
CMOS Reprogrammable	20 nsF	TS	5	PLDC20RA10-20	Cypress (4218)	15	25 nsF TS	5			PEEL22CV10-25	ICT (4259)	
			5	PALC16L8-20M	† Cypress (4217)		35 nsF TS	5			PEEL22CV10Z	ICT (4259, 4265)	40
				PALC16R4-20M	† Cypress (4217)						PEEL22CV10-35	ICT (4259)	
				PALC16R8-20M	† Cypress (4217)		Electrically Erasable Programmable Logic, CMOS, 74						
CMOS Reprogrammable Asynchronous Registered EPLD.	25 nsF	TS	5	CY7C331-25WC	° Cypress (4220)		Product Terms, 36 Inputs						
	30 nsF	TS	5	CY7C331-30WM	*† Cypress (4220)		18 nsF TS	5			PEEL 18CV8	Gould	
	35 nsF	TS	5	CY7C331-35WC	° Cypress (4220)	20	Electrically Erasable Programmable Logic, CMOS, 8						
	40 nsF	TS	5	CY7C331-40WM	*† Cypress (4220)		Dedicated Inputs, 10 I/O Pins, Programmable AND						
							(42 product terms), Programmable OR (20 sum						
							terms)						
							30 nsF TS	5			PEEL153-30	ICT (4259, 4263)	
											PEEL18CP210-30	ICT	
CMOS Reprogrammable, Low Power, Variable Product Terms (2x8 through 2x16)	25 nsF	TS	5	PALC22V10L-25	Cypress (4217)		Electrically-Reprogrammable ASIC device, E <sup>2</sup> CMOS,						
CMOS Reprogrammable Synchronous State Machine.	15 nsF	TS	5	CY7C330-50WC	° Cypress (4219)		28-pin, 65K-way programmable I/O macrocell, 20						
	20 nsF	TS	5	CY7C330-33WC	° Cypress (4219)		buriable JK/T/D flip-flops, latchable inputs, logic						
				CY7C330-40WM	*† Cypress (4219)	25	cascadable internally.						
	25 nsF	TS	5	CY7C330-28WM	*† Cypress (4219)		25 nsF TS	5			XLE78C1600-25		45
Electrically Erasable Field Programmable Logic Array, 16 Inputs, 72 Product Terms, 8 Outputs	35 ns *	TS	5	PLC16V8	Signetics						EXEL		
				PLC20V8	Signetics						XLE78C800-25	EXEL	
Electrically Erasable Programmable Logic, CMOS, 12 Dedicated Inputs, 10 I/O Pins, Programmable AND (42 product terms), Programmable OR (20 sum terms)	30 nsF	TS	5	PEEL173-30	ICT (4259, 4261)						XLE78H800-25	EXEL	
				PEEL22CP210-30	ICT	30					XLM78H800-25	EXEL	
Electrically Erasable Programmable Logic, CMOS, 18 Inputs, 8 Outputs, 74 Product Terms, Programmable AND, Fixed OR, ' ' Zero Power Mode ' '(100μA)	15 nsF	TS	5	PEEL18CV8Z	ICT (4259, 4266)						XLS78C1600-25	EXEL	
	25 nsF	TS	5	PEEL18CV8-25	ICT (4259, 4266)						EXEL		
	35 nsF	TS	5	PEEL18CV8-35	ICT (4259, 4266)						XLS78C800-25	EXEL	50
											EXEL		
											XLE78C1600-35		55
											EXEL		
											XLM78C800-35	EXEL	
											XLM78H800-35	EXEL	
											EXEL		
											XLS78C1600-35		60
											EXEL		
											XLS78C800-35	EXEL	
											XLS78H800-35	EXEL	
											EXEL		
											XLE78C1600-45		65
											EXEL		
											XLE78C800-45	EXEL	
											XLM78C1600-45	EXEL	
											EXEL		
											XLM78C800-45	EXEL	
											† EXEL		
											XLS78C1600-45		
											EXEL		
											XLS78C800-45	EXEL	

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† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Programmable Logic (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line	Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line
E <sup>2</sup> CMOS Array Logic, In-System (Re-)Programmable, Re-Configurable architecture, Electrically re-programmable	15 nsR	TS	5	ispGAL16Z8-15L	Lattice	5	E <sup>2</sup> CMOS Quarter-Power Field re-Programmable Array Logic, Bipolar Compatible Generic Re-programmable replacement for Series 24 Programmable Array Logic	35 nsF	TS	5	GAL20V8-35Q	Lattice	(Cont'd) 35
				ispGAL20Z8-15L	Lattice						VP16V8E-35	VLSI Tech	
											VP20V8E-35	VLSI Tech	
	25 nsF	TS	5	ispGAL16Z8-25L	Lattice	10	Field Programmable aArray Logic, Half Power, Quad 16-Input Registered AND-OR array.	25 nsF	TS	5	PAL16R4B2C	National	40
				ispGAL20Z8-25L	Lattice								
	35 nsF	TS	5	ispGAL16Z8-35L	Lattice	15	Field Programmable Array Device, 12 Inputs, 9 Outputs	20 ns*	TS	5	PLS163	Signetics	(3155, 3171)
				ispGAL20Z8-35L	Lattice								
E <sup>2</sup> CMOS Field Programmable Array Logic, Bipolar Compatible Generic Re-programmable replacement for Series 20 Programmable Array Logic	15 nsR	TS	5	GAL16V8-15L	Lattice	20	Field Programmable Array Device, 16 Inputs, 5 Outputs	20 ns*	TS	5	PLS162	Signetics	(3155, 3170)
				GAL20V8-15L	Lattice								
	25 nsF	TS	5	GAL16V8-25L	Lattice	25	Field Programmable Array Logic	—	TS	5	TIBPAL16L6	TI	45
				GAL20V8-25L	Lattice		3 ns*	ECL	-5.2	PAL10H20P8	MMI		
							4 nsF	TS	5	XC2018-50PC68C	Xilinx		
	35 nsF	TS	5	GAL16V8-35L	Lattice	30				XC2018-50PC84C	Xilinx	(4346)	
				GAL20V8-35L	Lattice					XC2064-50PC68C	Xilinx		
										XC2064-50PD48C	Xilinx		
E <sup>2</sup> CMOS Field Programmable Array Logic, Electrically Erasable and Re-programmable Replacement for Series 20 & 24 Programmable Array Logic	15 nsR	TS	5	GAL16V8-25L	Lattice	35	6 nsF	ECL	-5.2	PL1016P8C	National	50	
				GAL20V8-15L	Lattice			TS	-4.5	AMPAL100L20EV8	AMD		
				RAL20R8-15	Lattice					AMPAL100R20EV8	AMD		
	25 nsF	TS	5	GAL16V8-25L	Lattice	40				AMPAL10L20EV8	AMD	55	
				GAL20V8-25L	Lattice					AMPAL10R20EV8	AMD		
	35 nsF	TS	5	GAL16V8-35L	Lattice	45	10 nsF	TS	5	16P8D	Fairchild	60	
				GAL20V8-35L	Lattice					16RP4D	Fairchild		
				RAL16L8-35	Lattice					16RP6D	Fairchild		
E <sup>2</sup> CMOS Programmable Electrically Erasable Logic (replacement for series 20 Logic)	25 nsF	TS	5	18CV8	ICT	50				16RP8D	Fairchild	65	
										PAL16L8DC	MMI		
										PAL16R4DC	MMI		
E <sup>2</sup> CMOS, 20-Inputs, 10 Outputs	35 nsF	TS	5	20RA10Z-35	SEEQ	55				PAL16R6DC	MMI	70	
	45 nsF	TS	5	20RA10Z-45	↑ SEEQ					PAL16R8DC	MMI		
E <sup>2</sup> CMOS Field Programmable Array Logic, Electrically Erasable & Re-programmable Replacement for Series 20 & 24 Programmable Array Logic	30 nsF	TS	5	GAL16V8-30LM	† Lattice	60				TIBPAL16L8-10	TI	(4320)	
				GAL20V8-30LM	† Lattice					TIBPAL16R4-10	TI		
											TIBPAL16R6-10		TI
						65				TIBPAL16R8-10	TI	(4320)	
							12 ns	TS	5	TIBPAL16L8-12	TI		
										TIBPAL16R4-12	TI		
E <sup>2</sup> CMOS Field Programmable Array Logic Re-Programmable	30 nsF	TS	5	GAL39V18	◊ Lattice	70				TIBPAL16R6-12	TI	(4320)	
										TIBPAL16R8-12	TI		
E <sup>2</sup> CMOS Programmable Array Logic Bipolar Compatible Re-Programmable for Series 20 PALs.	10 nsF	TS	5	GAL16V8-10	◊ Lattice	75	12 nsF	TS	5	TIBPAL16L8-12M	† TI	(4320)	
				GAL20V8-10	◊ Lattice					TIBPAL16R4-12M	† TI		
										TIBPAL16R6-12M	† TI		
E <sup>2</sup> CMOS Quarter-Power Field re-Programmable Array Logic, Bipolar Compatible Generic Re-programmable replacement for Series 20 Programmable Array Logic	25 nsF	TS	5	GAL16V8-25Q	Lattice	30				TIBPAL16R8-12M	† TI	(4320)	
				GAL16V8-35Q	Lattice		15 ns*	TS	5	TIBPAL20L10-20	TI		
				GAL20V8-25Q	Lattice					TIBPAL20X10-20	TI		
				VP16V8E-25	VLSI Tech	35				TIBPAL20X4-20	TI	(4320)	
				VP20V8E-25	VLSI Tech					TIBPAL20X8-20	TI		
						40				AMPAL16HD8BC	AMD	75	
										AMPAL16H8BC	AMD		
										AMPAL16L8BC	AMD		

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† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

◊ Macrocell

◊ Available in Surface Mount Package

**Bold face indicates additional data is provided on the page noted.**

## ASIC/CUSTOM—Programmable Logic (Cont'd)

Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	
Field Programmable Array Logic							Field Programmable Array Logic							
15 nsF	TS		5	(Cont'd)			20 nsF	TS		5	(Cont'd)			
				AMPAL16R4BC	AMD	5					PAL20RA10C	National	60	
				AMPAL16R6BC	AMD						PAL20RA10M	National		
				AMPAL16R8BC	AMD						TIBPAL16L8-20M			
				AMPAL18P8BC	AMD						† TI	(4320)		
				16L8B	◊ Fairchild						TIBPAL16R4-20	TI		(4320)
				16P8B	Fairchild						TIBPAL16R4-20M			
				16RP4B	Fairchild						† TI	(4320)		
				16RP6B	Fairchild						TIBPAL16R6-20M			
				16RP8B	Fairchild						† TI	(4320)		
				16R4B	Fairchild		10					TIBPAL16R8-20M		
				16R6B	Fairchild	15					† TI	(4320)		
				16R8B	Fairchild						TIBPAL20L8-20M			
				20L8B	Fairchild						† TI	(4320)		
				20P8B	Fairchild						TIBPAL20R4-20M			
				20RP4B	Fairchild						◊† TI	(4320)		
				20RP6B	Fairchild						TIBPAL20R6-20M			
				20RP8B	Fairchild						◊† TI	(4320)		
				20R4B	Fairchild						TIBPAL20R8-20M			
				20R6B	Fairchild						† TI	(4320)		
				20R8B	Fairchild		20							
				PAL16L8BC	◊ MMI	25	25 nsF	TS		5	AMPAL16HD8AC	AMD	70	
				PAL16R4BC	MMI						AMPAL16HD8ALC	AMD		
				PAL16R6BC	MMI						AMPAL16H8AC	AMD		
				PAL16R8BC	MMI						AMPAL16H8ALC	AMD		
				PAL20L8BC	MMI						AMPAL16LD8AC	AMD		
				PAL20R4BC	MMI						AMPAL16LD8ALC	AMD		
				PAL20R6BC	MMI						AMPAL16L8AC	AMD		
				PAL20R8BC	MMI						AMPAL16L8ALC	AMD		
				TIBPAL16L8-15	TI (4320)						AMPAL16R4AC	AMD		
				TIBPAL16L8-15M							AMPAL16R4ALC	AMD		
				† TI	(4320)	30					AMPAL16R6AC	AMD		
				TIBPAL16R4-15	TI (4320)						AMPAL16R6ALC	AMD		
				TIBPAL16R4-15M							AMPAL16R8AC	AMD		
				† TI	(4320)						AMPAL16R8ALC	AMD		
				TIBPAL16R6-15	TI (4320)						AMPAL16R8AC	AMD		
				TIBPAL16R6-15M							AMPAL16R8ALC	AMD		
				† TI	(4320)		35					AMPAL16R8AC	AMD	
				TIBPAL16R8-15	TI (4320)							AMPAL16R8ALC	AMD	
				TIBPAL16R8-15M								AMPAL16R8AC	AMD	
				† TI	(4320)							AMPAL16R8ALC	AMD	
				TIBPAL20L8-15	TI (4320)					AMPAL16R8AC	AMD			
				TIBPAL20R4-15	◊ TI (4320)					AMPAL16R8ALC	AMD			
				TIBPAL20R6-15	◊ TI (4320)					AMPAL16R8AC	AMD			
				TIBPAL20R8-15	TI (4320)					AMPAL16R8ALC	AMD			
						40						AMPAL16R8AC	AMD	
												AMPAL16R8ALC	AMD	
16 ns*	TS		5	TIBPALR19L8	TI (4320)	45					AMPAL16R8AC	AMD		
				TIBPALR19R4	TI (4320)						AMPAL16R8ALC	AMD		
				TIBPALR19R6	TI (4320)						AMPAL16R8AC	AMD		
				TIBPALR19R8	TI (4320)						AMPAL16R8ALC	AMD		
				TIBPALT19L8	TI (4320)						AMPAL16R8AC	AMD		
				TIBPALT19R4	TI (4320)						AMPAL16R8ALC	AMD		
				TIBPALT19R6	TI (4320)						AMPAL16R8AC	AMD		
				TIBPALT19R8	TI (4320)						AMPAL16R8ALC	AMD		
20 nsF	TS		5	AMPAL16HD8BM		50					AMPAL16R8AC	AMD		
				† AMD							AMPAL16R8ALC	AMD		
				AMPAL16H8BM							AMPAL16R8AC	AMD		
				† AMD							AMPAL16R8ALC	AMD		
				AMPAL16LD8BM							AMPAL16R8AC	AMD		
				† AMD							AMPAL16R8ALC	AMD		
				AMPAL16L8BM							AMPAL16R8AC	AMD		
				† AMD							AMPAL16R8ALC	AMD		
				AMPAL16R6BM							AMPAL16R8AC	AMD		
				† AMD							AMPAL16R8ALC	AMD		
				AMPAL16R8BM		55					AMPAL16R8AC	AMD		
				† AMD							AMPAL16R8ALC	AMD		
				AMPAL18P8BM							AMPAL16R8AC	AMD		
				† AMD							AMPAL16R8ALC	AMD		
											AMPAL16R8AC	AMD		
											AMPAL16R8ALC	AMD		
											AMPAL16R8AC	AMD		
											AMPAL16R8ALC	AMD		
											AMPAL16R8AC	AMD		
											AMPAL16R8ALC	AMD		
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			
										AMPAL16R8ALC	AMD			
										AMPAL16R8AC	AMD			

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

Bold face indicates additional data is provided on the page noted.



ASIC/CUSTOM—Programmable Logic (Cont'd)

Organi- zation	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	Organi- zation	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line
Field Programmable Array Logic 25 nsF TS 5 (Cont'd)							Field Programmable Array Logic 25 nsF TS 5 (Cont'd)						
				PAL16R6AC	MMI						PAL20R4AM	† National	
				PAL16R6B-2C	MMI						PAL20R6AC	National	
				PAL16R8AC	MMI						PAL20R6AM	† National	
				PAL16R8B-2C	MMI						PAL20R8AC	National	65
				PAL20L8AC	MMI	5					PAL20R8AM	† National	
				PAL20L8B-2	MMI						PAL16L8A	◊ TI	
				PAL20R4AC	MMI						PAL16L8AM	† TI	
				PAL20R4B-2	MMI						PAL16R4A	◊ TI	70
				PAL20R6AC	MMI						PAL16R6A	◊ TI	
				PAL20R6B-2	MMI	10					PAL16R6AM	† TI	
				PAL20R8AC	MMI						PAL16R8A	TI	
				PAL20R8B-2	MMI						PAL16R8A-2M		
				PAL22RX8A	MMI						† TI		
				PAL32VX10A	MMI						PAL16R8AM	† TI	
				PAL6L16AC	MMI	15					PAL1644AM	† TI	75
				PAL8L14AC	MMI						PAL20L8A	TI	
				PAL10H8AC	National						PAL20R4A	TI	
				PAL10H8A2C	National						PAL20R6A	TI	
				PAL10H8A2M							PAL20R8A	TI	
				† National							TIBPAL16L8-25	TI (4320)	80
				PAL10L8AC	National	20					TIBPAL16R4-25	TI (4320)	
				PAL10L8A2C	National						TIBPAL16R6-25	TI (4320)	
				PAL10L8A2M	† National						TIBPAL16R8-25	TI (4320)	
				PAL12H6AC	National						TIBPAL20L10-25M		
				PAL12H6A2C	National						† TI	(4320)	
				PAL12H6A2M							TIBPAL20L8-25	TI (4320)	85
				† National		25					TIBPAL20R4-25	◊ TI (4320)	
				PAL12L6AC	National						TIBPAL20R6-25	◊ TI (4320)	
				PAL12L6A2C	National						TIBPAL20X10-25M		
				PAL12L6A2M	† National						† TI	(4320)	
				PAL14H4AC	National						TIBPAL20X4-25M		
				PAL14H4A2C	National	30					† TI	(4320)	
				PAL14H4A2M							TIBPAL20X8-25M		
				† National							† TI	(4320)	90
				PAL14L4A2C	National						TIBPAL22VP10-25M		
				PAL14L4A2M	† National						*† TI		
				PAL16C1AC	National						TIBPAL22V10AM		
				PAL16C1A2C	National	35					*† TI	(4320)	
				PAL16C1A2M	† National						VP16RP8M	VLSI Tech	
				PAL16H2AC	National						TIBPAL20L10-20	TI (4320)	
				PAL16H2A2C	National						AMPALR8ALM		
				PAL16H2A2M							† AMD		95
				† National							AMPAL16H8ALM		
				PAL16L2AC	National	40					† AMD		
				PAL16L2A2C	◊ National						AMPAL16H8ALM		
				PAL16L2A2M							† AMD		
				◊† National							AMPAL16H8AM		
				PAL16L8AC	National						† AMD		
				PAL16L8A2C	National						AMPAL16L8ALM		
				PAL16L8A2M	† National	45					† AMD		
				PAL16P8A	National						AMPAL16L8AM		
				PAL16RP4A	National						† AMD		100
				PAL16RP6A	National						AMPAL16L8ALM		
				PAL16RP8A	National						† AMD		
				PAL16R4AC	National	50					AMPAL16L8AM		
				PAL16R4A2C	National						† AMD		
				PAL16R4A2M	† National						AMPAL16R4AM		
				PAL16R6AC	National						† AMD		
				PAL16R6A2C	National						AMPAL16R6AM		
				PAL16R6A2M	† National	55					† AMD		
				PAL16R8AC	National						AMPAL16R8AM		
				PAL16R8A2C	National						† AMD		105
				PAL16R8A2M	† National						AMPAL18P8ALM		
				PAL20L8AC	National						† AMD		
				PAL20L8AM	† National	60					AMPAL18P8AM		
				PAL20R4AC	National						† AMD		
(Continued)							(Continued)						

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

**Bold face indicates additional data is provided on the page noted.**

## ASIC/CUSTOM—Programmable Logic (Cont'd)

Organ- ization	Pro- paga- tion Time	Output	Supply Voltage, V	Device	Source	Line	Organ- ization	Pro- paga- tion Time	Output	Supply Voltage, V	Device	Source	Line
Field Programmable Array Logic 30 nsF TS 5 (Cont'd)							Field Programmable Array Logic 35 nsF TS 5 (Cont'd)						
				AMPAL22V10AM							AMPAL16R6LC AMD		
				† AMD							AMPAL16R6QC AMD		60
				CYPAL22V10-30MC							AMPAL16R8C AMD		
				† Cypress							AMPAL16R8LC AMD		
				PAL16L8AM ♦ MMI							AMPAL16R8QC AMD		
				PAL16P8AM † MMI		5					AMPAL18P8LC AMD		
				PAL16RA8C MMI							AMPAL18P8QC AMD		65
				PAL16RP4AM † MMI							AMPAL22V10C AMD		
				PAL16RP6AM † MMI							CYPAL22V10-35CC		
				PAL16RP8AM † MMI							Cypress		
				PAL16R4AM † MMI		10					CYPAL22V10-40MC		
				PAL16R6AM † MMI							Cypress		
				PAL16R8AM † MMI							PAL10H8C ♦ MMI		
				PAL20L10AC MMI		15					PAL10L8C ♦ MMI		70
				PAL20L8AM † MMI							PAL12H6C ♦ MMI		
				PAL20RA10C ♦ MMI							PAL12L6C ♦ MMI		
				PAL20R4AM † MMI							PAL14H4C ♦ MMI		
				PAL20R6AM † MMI		20					PAL14L4C ♦ MMI		
				PAL20R8AM † MMI							PAL16H2C ♦ MMI		75
				PAL20X10AC MMI							PAL16L2C ♦ MMI		
				PAL20X4AC ♦ MMI							PAL16L8A-2C ♦ MMI		
				PAL20X8AC ♦ MMI		25					PAL16L8B-4C ♦ MMI		
				PAL32VX10 MMI							PAL16R4A-2C MMI		80
				PAL10H8AM † National							PAL16R4B-4C MMI		
				PAL10L8AM † National							PAL16R6A-2C MMI		
				PAL12H6AM † National							PAL16R6B-4C MMI		
				PAL12L6AM † National		30					PAL16R8A-2C MMI		
				PAL14H4AM † National							PAL16R8B-4C MMI		
				PAL14L4AM † National							PAL20L8A-2C MMI		
				PAL16C1AM † National							PAL20RA10M		
				PAL16H2AM † National							♦ MMI		85
				PAL16L2AM † National							PAL20RS10C ♦ MMI		
				PAL16L8AM † National							PAL20RS4C ♦ MMI		
				PAL16R4AM † National		35					PAL20RS8C ♦ MMI		
				PAL16R6AM † National							PAL20R4A-2C MMI		
				PAL16R8AM † National							PAL20R4B-2C MMI		90
				TIBPAL16L8-30M							PAL20R6A-2C MMI		
				† TI (4320)							PAL20R6B-2C MMI		
				TIBPAL16R4-30M							PAL20R8A-2C MMI		
				† TI (4320)							PAL20R8B-2C MMI		
				TIBPAL16R6-30M							PAL20S10C ♦ MMI		95
				† TI (4320)							PAL10H8C National		
				TIBPAL16R8-30M							PAL10L8C National		
				† TI (4320)							PAL12H6C National		
				TIBPAL20X10-30 TI (4320)							PAL12L6C National		
				TIBPAL20X4-30 TI (4320)		40					PAL14H4C National		100
				TIBPAL20X8-30 TI (4320)							PAL14L4C National		
35 nsF TS 5				AMPAL16HD8C AMD							PAL16C1C National		
				AMPAL16HD8LC							PAL16H2C National		
				AMD							PAL16L2C National		
				AMPAL16HD8QC							PAL16L8C National		105
				AMD							PAL16R4C National		
				AMPAL16H8C AMD		45					PAL16R6C National		
				AMPAL16H8LC AMD							PAL16R8C National		
				AMPAL16H8QC AMD							10P8BP-35 Panatech		
				AMPAL16LD8C AMD							12P6BP-35 Panatech		110
				AMPAL16LD8LC AMD							14P4BP-35 Panatech		
				AMPAL16LD8QC							16P2BP-35 Panatech		
				AMD		50					16RP4BP-35 Panatech		
				AMPAL16L8C AMD							16RP6BP-35 Panatech		
				AMPAL16L8LC AMD							16RP8BP-35 Panatech		115
				AMPAL16L8QC AMD							PAL16L8A-2 TI		
				AMPAL16R4C AMD							PAL16L8A-2M		
				AMPAL16R4LC AMD		55					† TI		
				AMPAL16R4QC AMD							PAL16R4A-2 TI		
				AMPAL16R6C AMD							(Continued)		

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

♦ Available in Surface Mount Package

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## ASIC/CUSTOM—Programmable Logic (Cont'd)

ASICs/CUSTOM

Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line
Field Programmable Array Logic 35 nsF TS 5 (Cont'd)							Field Programmable Array Logic 40 nsF TS 5 (Cont'd)						
				PAL16R4A-2M	† TI						PAL20RS8M	◊† MMI	40
				PAL16R6A-2	TI						PAL20S10M	◊† MMI	
				PAL16R6A-2M	† TI						PAL32R16C	◊† MMI	
				PAL16R8A-2	TI						PAL12L10C	◊ National	
40 nsF TS 5				AMPAL16HD8LM	† AMD	5					PAL12L10M	◊† National	
				AMPAL16HD8M	† AMD						PAL14L8C	National	45
				AMPAL16HD8QM	† AMD						PAL14L8M	† National	
				AMPAL16H8LM	† AMD						PAL16L6C	National	
				AMPAL16H8M	† AMD						PAL16L6M	National	
				AMPAL16H8QM	† AMD						PAL18L4C	National	
				AMPAL16LD8LM	† AMD	10					PAL18L4M	† National	50
				AMPAL16LD8M	† AMD						PAL20C1C	National	
				AMPAL16LD8QM	† AMD		45 nsF OC 5				PAL20C1M	† National	
				AMPAL16L8LM	† AMD			TS 5			PAL20L2C	National	
				AMPAL16L8M	† AMD	15					93Z458C	Fairchild	
				AMPAL16L8QM	† AMD						93Z459C	Fairchild	55
				AMPAL16P8LM	† AMD						PAL10H8M	◊† MMI	
				AMPAL16R4LM	† AMD						PAL10L8M	◊† MMI	
				AMPAL16R4M	† AMD						PAL12H6M	◊† MMI	
				AMPAL16R4QM	† AMD						PAL12L10M	◊† MMI	60
				AMPAL16R6LM	† AMD						PAL12L6M	◊† MMI	
				AMPAL16R6M	† AMD						PAL14H4M	◊† MMI	
				AMPAL16R6QM	† AMD						PAL14L4M	◊† MMI	
				AMPAL16R8LM	† AMD						PAL14L8M	◊† MMI	
				AMPAL16R8M	† AMD	20					PAL16A4M	◊† MMI	
				AMPAL16R8QM	† AMD						PAL16C1M	◊† MMI	65
				AMPAL18P8QM	† AMD						PAL16H2M	◊† MMI	
				AMPAL22V10M	† AMD						PAL16L2M	◊† MMI	
				PAL12L10C	MMI						PAL16L6M	◊† MMI	
				PAL14L8C	◊ MMI	30					PAL16X4M	† MMI	
				PAL16A4C	MMI						PAL18L4M	◊† MMI	70
				PAL16C1C	◊ MMI						PAL20C1M	◊† MMI	
				PAL16L6C	◊ MMI						PAL20L2M	† MMI	
				PAL16X4C	MMI						PAL10H8M	† National	
				PAL18L4C	MMI	35					PAL10L8M	† National	
				PAL20C1C	MMI						PAL12H6M	† National	75
				PAL20L2C	◊ MMI						PAL12L6M	† National	
				PAL20RS10M	◊† MMI						PAL14H4M	† National	
				PAL20RS4M	◊† MMI						PAL14L4M	† National	
											PAL16C1M	† National	
											PAL16H2M	† National	80
											PAL16L2M	† National	
											PAL16L8M	† National	
											PAL16R4M	† National	
											PAL16R6M	† National	85
											PAL16R8M	† National	
											PAL20L2M	† National	
							50 nsF TS 5				PAL16L8A-2M	◊† MMI	
											PAL16R4A-2M	† MMI	
											PAL16R6A-2M	† MMI	
											PAL16R8A-2M	† MMI	90
											PAL20L10C	◊ MMI	
											PAL20X10C	◊ MMI	
											PAL20X4C	◊ MMI	
											PAL20X8C	◊ MMI	
											PAL64R32C	◊ MMI	95
											PAL20L10C	National	
											PAL20L10M	National	
											PAL20X10C	National	
											PAL20X4C	National	

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Programmable Logic (Cont'd)

Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	Organiza- tion	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line
Field Programmable Array Logic							Field Programmable Array Logic, CMOS						
50 nsF	TS		5			(Cont'd)	25 nsF	TS		5			(Cont'd)
				PAL20X8C	National						PALC16L8Q-25	MMI	60
				PAL209X4C	National						PALC16RQ-45	MMI	
55 nsF	TS		5	PAL16L8A-4C	MMI	5					PALC16R6Q-25	MMI	
				PAL16R4A-4C	MMI						PALC16R8Q-25	MMI	
				PAL16R6A-4C	MMI						PALC22V10H-25		
				PAL16R8A-4C	MMI						MMI		
				ASP6AP-55	Panatech		30 nsF	TS		5	PALC16L8-30M	† Cypress (4217)	65
				10P8AP-55	Panatech						PALC16R4-30M	† Cypress (4217)	
				14P4AP-55	Panatech						PALC16R6-30M	† Cypress (4217)	
				16P2AP-55	Panatech	10					PALC16R8-30M	† Cypress (4217)	
				16RP4AP-55	Panatech		35 nsF	TS		5	PALC16L8-35C	Cypress (4217)	70
				16RP6AP-55	Panatech						PALC16R4-35C	Cypress (4217)	
				16RP8AP-55	Panatech						PALC16R6-35C	Cypress (4217)	
60 nsF	TS		5	PAL10H8-2C	MMI	15					PALC16R8-35C	Cypress (4217)	
				PAL10L8-2C	MMI						PALC20L8Z-35	MMI	75
				PAL12H6-2C	MMI						PALC20R4Z-35	MMI	
				PAL12L6-2C	MMI						PALC20R6Z-35	MMI	
				PAL14H4-2C	MMI						PALC20R8Z-35	MMI	
				PAL14L4-2C	MMI	20					PALC22V10H-35		
				PAL16C1-2C	MMI		40 nsF	TS		5	PALC16L8-40M	† Cypress (4217)	80
				PAL16H2-2C	MMI						PALC16R4-40M	† Cypress (4217)	
				PAL16L2-2C	MMI						PALC16R6-40M	† Cypress (4217)	
				PAL20L10M	† MMI						PALC16R8-40M	† Cypress (4217)	
				PAL20X10M			45 nsF	TS		5	PALC20L8Z-45	MMI	
				† MMI		25					PALC20R4Z-45	MMI	
				PAL20X4M	† MMI						PALC20R6Z-45	MMI	
				PAL20X8M	† MMI						PALC20R8Z-45	MMI	
				PAL20X10M	† National		Field Programmable Array Logic, CMOS, Erasable.						
				PAL20X4M	† National		20 nsF	TS		5	PALC16R4-20WM		
				PAL20X8M	† National						† Cypress (4217)		
65 nsF	OC		5	93Z458M	† Fairchild	30					PALC16L8-20WM		
	TS		5	93Z459M	† Fairchild						† Cypress (4217)		
75 nsF	TS		5	PAL16L8A-4M							PALC16R6-20WM		
				† MMI							† Cypress (4217)		
				PAL16R4A-4M							PALC16R8-20WM		
				† MMI							† Cypress (4217)		
				PAL16R6A-4M									
				† MMI			Field Programmable Array Logic, CMOS, Erasable						
				PAL16R8A-4M			25 nsF	TS		5	PALC16L8-25WC	Cypress (4217)	90
				† MMI		35					PALC16L8L-25WC	Cypress (4217)	
80 nsF	TS		5	PAL10H8-2M	† MMI						PALC16R4-25WC	Cypress (4217)	
				PAL10L8-2M	† MMI						PALC16R6-25WC	Cypress (4217)	
				PAL12H6-2M	† MMI						PALC16R8-25WC	Cypress (4217)	
				PAL12L6-2M	† MMI						PALC16R8L-25WC	Cypress (4217)	95
				PAL14H4-2M									
				† MMI		40							
				PAL14L4-2M	† MMI		30 nsF	TS		5	PALC16L8-30WM		
				PAL16C1-2M	† MMI						† Cypress (4217)		
				PAL16H2-2M	† MMI						PALC16R4-30WM		
				PAL16L2-2M							† Cypress (4217)		
				† MMI							PALC16R6-30WM		
125 nsF	TS		5	HPL16LC8-2	† Harris (2768)	45					† Cypress (4217)		
				HPL16LC8-9	† Harris (2768)						PALC16R8-30WM		
				HPL16RC4-2	† Harris (2768)						† Cypress (4217)		
				HPL16RC4-9	† Harris (2768)		35 nsF	TS		5	PALC16L8-35WC	Cypress (4217)	100
				HPL16RC6-2	† Harris (2768)						PALC16L8L-35WC	Cypress (4217)	
				HPL16RC6-9	† Harris (2768)	50					PALC16R4-35WC	Cypress (4217)	
				HPL16RC8-2	† Harris (2768)						PALC16R4L-35WC	Cypress (4217)	
				HPL16RC8-9	† Harris (2768)						PALC16R6-35WC	Cypress (4217)	
Field Programmable Array Logic, CMOS											PALC16R6L-35WC	Cypress (4217)	105
20 usF	TS		5	PALC16R6-20M	† Cypress (4217)						PALC16R8-35WC	Cypress (4217)	
25 nsF	TS		5	PALC16L8-25C	Cypress (4217)						PALC16R8L-35WC	Cypress (4217)	
				PALC16R4-25C	Cypress (4217)	55							
				PALC16R6-25C	Cypress (4217)								
				PALC16R8-25C	Cypress (4217)								

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

Bold face indicates additional data is provided on the page noted.



## ASIC/CUSTOM—Programmable Logic (Cont'd)

ASICs/CUSTOM

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line	Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line	
Field Programmable Array Logic, CMOS, Erasable 40 nsF TS 5							(Cont'd)	Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 30 nsF TS 5						(Cont'd)
				PALC16L8-40WM							PAL16L8B2M † National			
				† Cypress	(4217)						PAL16R8B2M † National			
				PALC16R4-40WM										
				† Cypress	(4217)									
				PALC16R6-40WM										
				† Cypress	(4217)									
				PALC16R8-40WM										
				† Cypress	(4217)									
Field Programmable Array Logic, CMOS Erasable, 64 Inputs, 480 Product Terms, 48 Outputs 50 nsF TS 5							5	Field Programmable Array Logic, Low Power CMOS TS 5						45
				EP1800-1C	Altera						55 nsF TS 5	TICPAL16L8-55 TI	(4320)	
				EP1800-1M † Altera								TICPAL16R4-55 † TI	(4320)	
				EP1800-2C	Altera							TICPAL16R6-55 † TI	(4320)	
				EP1800-2M † Altera								TICPAL16R8-55 † TI	(4320)	
				EP1800-3C	Altera									
				EP1800-3M † Altera		10								
				EP1800C	Altera									
				EP1800M † Altera										
Field Programmable Array Logic, CMOS, Generic Replacement for PAL24, Quarter Power 25 nsF TS 5								Field Programmable Array Logic, Macrocell, 22 Inputs, 10 Outputs 25 nsF TS 5						
				PLDC20G10-25C	Cypress	(4218)						TIBPAL22VP10A-20 TI		
				PLDC20G10-25WC	Cypress	(4218)						TIBPAL22V10A † TI	(3217, 4320)	
				PLDC20G10-30M										
				† Cypress	(4218)									
				PLDC20G10-30WM										
				† Cypress	(4218)									
				PLDC20G10-35C	Cypress	(4218)								
				PLDC20G10-35WC	Cypress	(4218)								
				PLDC20G10-40M										
				† Cypress	(4218)									
				PLDC20G10-40WM										
				† Cypress	(4218)									
Field Programmable Array Logic, CMOS, Quarter Power 25 nsF TS 5								Field Programmable Array Logic, Power, Octal 16-Input Registered AND-OR array. 45 nsF TS 5						
				PALC16L8L-25C	Cypress	(4217)						PAL16R8B4M † National		
				PALC16R4L-25C	Cypress	(4217)								
				PALC16R6L-25C	Cypress	(4217)								
				PALC16R8L-25C	Cypress	(4217)								
				PALC16L8L-35C	Cypress	(4217)								
				PALC16R4L-35C	Cypress	(4217)								
				PALC16R6L-35C	Cypress	(4217)								
				PALC16R8L-35C	Cypress	(4217)								
Field Programmable Array Logic, CMOS, Reprogrammable 35 nsF TS 5								Field Programmable Array Logic, Quarter Power, Hex 16-Input Registered AND-OR array. 35 nsF TS 5						
				10P8	Panatech							PAL16R6B4C National		
				12P6	Panatech							PAL16R4B4M † National		
				14P4	Panatech									
				16P2	Panatech									
				16P8	Panatech									
				16RP6	Panatech									
				16RP8	Panatech									
Field Programmable Array Logic, Exclusive-OR 25 nsF TS 5								Field Programmable Array Logic, Quarter Power, Octal 16-Input AND-OR-INVERT array. 35 nsF TS 5						
				TIBPAL20R8-25 TI		(4320)						PAL16L8B4C National		
				TIBPAL20L10-30 TI		(4320)						PAL16R8B4C National		
Field Programmable Array Logic, Half Power, Quad 16-Input Registered AND-OR array. 30 nsF TS 5								Field Programmable Array Logic, Power, Octal 16-Input AND-OR-INVERT array. 45 nsF TS 5						
				PAL16R4B2M † National								PAL16L8B4M † National		
Field Programmable Array Logic, Half Power, Hex 16-Input Registered AND-OR array. 25 nsF TS 5								Field Programmable Array Logic, Quarter Power, Hex 16-Input Registered AND-OR array. 35 nsF TS 5						
				PAL16R6B2C National								PAL16R6B4C National		
				PAL16R6B2M † National										
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, Up to 20 Inputs (4 Dedicated and 16 I/O) or 16 Outputs 35 nsF TS 5						
				PAL16L8B2C National								5C060 Intel		
				PAL16R8B2C National										
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, Up to 36 Inputs (12 Dedicated and 24 I/O) or 24 Outputs 40 nsF TS 5						
				PAL16L8B2C National								5C090 Intel		
				PAL16R8B2C National										
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, 4 Latches (Common Clock) Plus 4 Combinatorial I/Os 5 nsF ECL 10KH -5.2 ECL 100KH -4.5						
				PAL16L8B2C National								PAL1016LC4 National		
				PAL16R8B2C National								PAL10016LC4 National		
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, 4 Latches (Dual Clocks) Plus 4 Combinatorial I/Os 5 nsF ECL 10KH -5.2 ECL 100KH -4.5						
				PAL16L8B2C National								PAL1016LD4 National		
				PAL16R8B2C National								PAL10016LD4 National		
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, 4 registers (Common Clock) Plus 4 Combinatorial I/Os 5 nsF ECL 10KH -5.2 ECL 100KH -4.5						
				PAL16L8B2C National								PAL1016RC4 National		
				PAL16R8B2C National								PAL10016RC4 National		
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, 4 Registers (Dual Clocks) Plus 4 Combinatorial I/Os 5 nsF ECL 10KH -5.2 ECL 100KH -4.5						
				PAL16L8B2C National								PAL1016RD4 National		
				PAL16R8B2C National								PAL10016RD4 National		
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, 8 Latched Outputs with Common ORed Clock 5 nsF ECL 10KH -5.2 ECL 100KH -4.5						
				PAL16L8B2C National								PAL1016LC8 National		
				PAL16R8B2C National								PAL10016LC8 National		
Field Programmable Array Logic, Half Power, Octal 16-Input AND-OR-INVERT array. 25 nsF TS 5								Field Programmable Array Logic, 8 Latches with Dual Clocks (4 Latches Each) 5 nsF ECL 10KH -5.2 ECL 100KH -4.5						
				PAL16L8B2C National								PAL1016LD8 National		
				PAL16R8B2C National								PAL10016LD8 National		
							(Continued)							



## ASIC/CUSTOM—Programmable Logic (Cont'd)

Organ- ization	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	Organ- ization	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line
Field Programmable Array Logic, 8 Registered Outputs with Common ORED Clock							Field Programmable Array Logic, 18 Inputs, 42 Product Terms, 10 Outputs						
	5 nsF	ECL 10KH	-5.2	PAL1016RC8	National			15 ns *	TS	5	PLUS153	◊ Signetics	
		ECL 100KH	-4.5	PAL10016RC8	National								
Field Programmable Array Logic, 8 Registers with Dual Clocks (4 Registers Each)							Field Programmable Gate Array, 16 Inputs, 9 AND/NAND Gates, 9 Outputs						
	5 nsF	ECL 10KH	-5.2	PAL1016RD8	National			20 ns*	TS	5	PLS103	Signetics (3155)	30
		ECL 100KH	-4.5	PAL10016RD8	National								
Field Programmable Array Logic, 10K ECL PAL with parity							Field Programmable Gate Array, 6 Inputs, 12 AND Gates, 12 I/O Lines						
	5 nsF	TS	5	TIEPAL10H16P8-6	TI (4320)	5		15 ns*	TS	5	PLS151	Signetics (3155, 3168)	
Field Programmable Array Logic, 22 Inputs, 10 Macro-Cell Outputs, Variable Product Terms, CMOS, Erasable.								20 ns*	OC	5	S82S150	† Signetics	
	25 nsF	TS	5	PALC22V10-25M	◊† Cypress (4217)		Field Programmable Identity Comparator, 12-Bit						
				PALC22V10-25WC	◊ Cypress (4217)			—	—	5	SN74ALS528	TI	
				PALC22V10-25WM	◊† Cypress (4217)		Field Programmable Identity Comparator, 16-Bit						
				PALC22V10L-25C	◊† Cypress (4217)			—	—	5	SN74ALS526	TI	
							Field Programmable Identity Comparator, 8-Bit and 4-Bit Comparator						
								—	—	5	SN74ALS527	TI	35
	30 nsF	TS	5	PALC22V10-30M	◊† Cypress (4217)	10	Field Programmable Logic Array, CMOS Erasable						
				PALC22V10-30WM	◊† Cypress (4217)			18 Inputs, 74 Product Terms, 8 Outputs					
								25 nsF	TS		EP320-1C	Altera	
								35 nsF	TS		EP320-2C	Altera	
								45 nsF	TS		EP320C	Altera	
											EP320M	Altera	
	35 nsF	TS	5	PALC22V10-35C	◊† Cypress (4217)		Field Programmable Logic Array, CMOS Erasable, 18 Inputs, 74 Product Terms, 8 Outputs						
				PALC22V10-35WC	◊ Cypress (4217)			25 nsF	TS	5	EP310-1C	Altera	40
				PALC22V10L-35C	◊† Cypress (4217)						EP310-1M	† Altera	
											EP600-1C	Altera	
											EP600-1M	† Altera	
	40 nsF	TS	5	PALC22V10-40M	◊† Cypress (4217)	15		30 nsF	TS	5	EP900-1C	Altera	45
				PALC22V10-40WM	◊† Cypress (4217)						EP900-1M	† Altera	
								35 nsF	TS	5	EP310-2C	Altera	
											EP310-2M	† Altera	
											EP600-2C	Altera	
											EP600-2M	† Altera	
	25 nsF	TS	5	PALC22V10-25C	◊† Cypress (4217)			40 nsF	TS	5	EP900-2C	Altera	50
Field Programmable Array Logic, 22 Inputs, 10 Outputs, Macrocell											EP900-2M	† Altera	
	25 nsF	TS	5	AT22V10-25	◊† Atmel			45 nsF	TS	5	EP600-3C	Altera	
	30 nsF	TS	5	AT22V10-30	◊† Atmel						EP600-3M	† Altera	
	35 nsF	TS	5	AT22V10-35	◊† Atmel	20		50 nsF	TS	5	EP1210-1C	Altera	55
	40 nsF	TS	5	AT22V10-40	◊† Atmel						EP1210-1M	† Altera	
Field Programmable Array Logic, 42 Inputs, 20 Flip-Flops, 10 Outputs											EP310C	Altera	
	30 nsF	TS	5	ATV750-30	◊† Atmel						EP310M	† Altera	
	35 nsF	TS	5	ATV750-35	◊† Atmel						EP900-3C	Altera	
	40 nsF	TS	5	ATV750-40	◊† Atmel						EP900-3M	† Altera	
Field Programmable Array Logic, 48 Flip-Flops, 26 Inputs, 24 Outputs								55 nsF	TS	5	EP600C	Altera	60
	35 nsF	TS	5	ATV2500-35	◊† Atmel						EP600M	† Altera	
	40 nsF	TS	5	ATV2500-40	◊† Atmel			60 nsF	TS	5	EP900C	Altera	
	45 nsF	TS	5	ATV2500-45	◊† Atmel						EP900M	† Altera	
Field Programmable Array Logic, 10K ECL								65 nsF	TS	5	EP1210-2C	Altera	65
	6 nsF	TS	-5.2	PAL10H20G8	MMI						EP1210-2M	† Altera	
								90 nsF	TS	5	EP1210C	Altera	
											EP1210M	† Altera	
Field Programmable Logic Array, 48 I/O							Field Programmable Logic Array, Erasable, 16 Inputs, 48 I/O						
	35 nsF	TS	5	ATV2500-35	◊† Atmel	25		50 nsF	—	5	5C180	Intel	
	40 nsF	TS	5	ATV2500-40	◊† Atmel								
	45 nsF	TS	5	ATV2500-45	◊† Atmel		Field Programmable Logic Array, E <sup>2</sup> , 10–22 Inputs, 66 product terms, 24 pins						
											XL78C800	EXEL (4228)	
Field Programmable Array Logic, 10K ECL							Field Programmable Logic Array, 18 Inputs (10 Dedicated and 8 I/O) and 8 Outputs						
	6 nsF	TS	-5.2	PAL10H20G8	MMI			50 nsF	TS	5	5C031	Intel	70
											5C032	Intel	

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

◊ Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Programmable Logic (Cont'd)

Organi- zation	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line	Organi- zation	Propa- gation Time	Output	Supply Voltage, V	Device	Source	Line
Field Programmable Logic Array, 36 Inputs or 24 Outputs, 28 Macrocells	50 nsF	TS	5	5C121	◊ Intel	5	Field Programmable Logic Element (PLE), 9 Inputs, 8 Registered Outputs, 512 Product Terms	15 nsF	Reg	5	PLE9R8C	◊ MMI	30
								20 nsF	Reg	5	PLE9R8M	◊ MMI	
Field Programmable Logic Array, 12 Inputs, 48 Product Terms, 8 Outputs	35 ns*	TS	5	PLS161	Signetics (3155)	5	Field Programmable Logic Element (PLE), 10 Inputs, 8 Registered Outputs, 1024 Product Terms	30 nsF	TS	5	PLE9P8C	◊ MMI	35
				PLS179	Signetics (3155, 3166)			35 nsF	TS	5	PLE9P4C	◊ MMI	
Field Programmable Logic Array, 14 Inputs, 32 Product Terms, Six Sum Terms	10 ns *	OC	5	TIFPLA840C	TI	5	Field Programmable Logic Element (PLE), 11 Inputs, 8 Registered Outputs with Asynchronous Enable, 2048 Product Terms	40 nsF	TS	5	PLE9P8M	◊ MMI	40
				TIFPLA840M †	TI			45 nsF	TS	5	PLE10P8M	◊ MMI	
Field Programmable Logic Array, 16 Inputs, 48 Product Terms, 8 Outputs		TS	5	TIFPLA839C	TI	5	Field Programmable Logic Element (PLE), 12 Inputs, 4 Outputs, 4096 Product Terms	50 nsF	TS	5	PLE10P4M	◊ MMI	40
				TIFPLA839M †	TI								
Field Programmable Logic Array, 18 Inputs, 42 Product Terms, 10 Outputs	35 ns*	TS	5	PLS100	Signetics (3155, 3167)	10	Field Programmable Logic Element (PLE), 5 Inputs, 16 Outputs, 3 Product Terms	15 nsF	TS	5	PLE11RA8C	◊ MMI	45
	50 nsF	TS	5	8700	Commodore			20 nsF	TS	5	PLE11RS8C	◊ MMI	
Field Programmable Logic Array, 18 Inputs, 72 Product Terms, 8 Outputs	45 ns *	TS	5	PLC153	Signetics	10	Field Programmable Logic Element (PLE), 6 Inputs, 16 Outputs, 6 Product Terms	35 nsF	TS	5	PLE11RA8M	◊ MMI	45
								50 nsF	TS	5	PLE11RS8M	◊ MMI	
Field Programmable Logic Array, 20 Inputs, 24 Product Terms, 11 Outputs	14 ns *	TS	5	PLHS18P8A	Signetics (3155, 3173)	15	Field Programmable Logic Element (PLE), 5 Inputs, 16 Outputs, 3 Product Terms				PLE11P4C	◊ MMI	50
											PLE11P8C	◊ MMI	
Field Programmable Logic Array, 20 Inputs, 24 Product Terms, 11 Outputs	15 ns*	TS	5	PLHS473	Signetics (3155, 3175)	15	Field Programmable Logic Element (PLE), 5 Inputs, 16 Outputs, 3 Product Terms	50 nsF	TS	5	PLE11P4M	◊ MMI	50
	20 ns*	TS	5	PLC473	Signetics						PLE11P8M	◊ MMI	
Field Programmable Logic Array, 22 Inputs, 42 Product Terms, 10 Outputs	15 ns *	TS	5	PLUS173	Signetics	15	Field Programmable Logic Element (PLE), 5 Inputs, 16 Outputs, 3 Product Terms						55
	20 ns*	TS	5	PLS173	Signetics (3155, 3172)								
Field Programmable Logic Array, 24 Inputs, 72 Product Terms, 16 Outputs						15	Field Programmable Logic Element (PLE), 6 Inputs, 16 Outputs, 6 Product Terms						55
Field Programmable Logic Array, 32 Inputs, 72 Product Terms, 24 Outputs	200 nsF	TS	5	μPB450	NEC	20	Field Programmable Logic Sequencer, 16 Inputs, 48 Terms, 8 Outputs	20 nsF	TS	5	PLE6P16C	◊ MMI	60
	20 ns *	TS	5	PLHS501	Signetics			60 nsF	TS	5	N82S105A	TI	
Field Programmable Logic Array, 48 Product Terms, 14 Inputs						20	Field Programmable Logic Sequencer, 14 Inputs, 48 AND Gates, 25 OR Gates, 6 I/O Lines						60
Field Programmable Logic Array, 8 Inputs, 32 AND Gates, 10 OR Gates, 10 I/O Lines	100 nsF	OC	5	IM5200	GE/Intersil	20	Field Programmable Logic Sequencer, 16 Inputs, 45 Transition Terms, 12 Outputs	—	TS	5	82S167A	TI	65
	15 ns*	TS	5	PLHS153	Signetics			-	TS	5	TIB82S167B	TI (4320)	
Field Programmable Logic Array, 8 Inputs, 32 AND Gates, 10 OR Gates, 10 I/O Lines						20	Field Programmable Logic Sequencer, 16 Inputs, 45 Transition Terms, 12 Outputs	45 ns*	TS	5	PLS168A	◊ Signetics (3155, 3164)	60
								45 nsF	TS	5	PLS167A	◊ Signetics (3155, 3162)	
Field Programmable Logic Element (PLE), 5 Inputs, 8 Outputs, 32 Product Terms	20 ns*	TS	5	PLS153A	Signetics (3155, 3169)	20	Field Programmable Logic Sequencer, 16 Inputs, 45 Transition Terms, 12 Outputs	60 ns*	TS	5	PLS168	Signetics (3155, 3164)	60
								60 nsF	TS	5	PLS167	Signetics (3155, 3162)	
Field Programmable Logic Element (PLE), 5 Inputs, 8 Outputs, 32 Product Terms	15 nsF	TS	5	PLE5P8AC	MMI	25	Field Programmable Logic Sequencer, 16 Inputs, 45 Transition Terms, 12 Outputs						65
	25 nsF	TS	5	PLE5P8C	◊ MMI								
Field Programmable Logic Element (PLE), 8 Inputs, 8 Outputs, 256 Product Terms	9974Z	OPC		PLE5P8M	◊ MMI	25	Field Programmable Logic Sequencer, 16 Inputs, 45 Transition Terms, 12 Outputs	55 ns *	TS	5	PLS155	Signetics (3155, 3158)	65
Field Programmable Logic Element (PLE), 8 Inputs, 8 Outputs, 256 Product Terms	28 nsF	TS	5	PLE8P8C	MMI	25	Field Programmable Logic Sequencer, 16 Inputs, 45 Transition Terms, 12 Outputs						65
	30 nsF	TS	5	PLE8P4C	◊ MMI			45 ns*	TS	5	PLS105A	◊ Signetics (3155, 3157)	
Field Programmable Logic Element (PLE), 8 Inputs, 8 Outputs, 256 Product Terms						25	Field Programmable Logic Sequencer, 16 Inputs, 45 Transition Terms, 12 Outputs	60 ns*	TS	5	PLS105	Signetics (3155)	65
								60 nsF	OC	5	TIB82S104A	TI	

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\* Typical Value

◊ Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Programmable Logic (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line	Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line
Field Programmable Logic Sequencer, 16 Inputs, 64 Transition Terms, 8 Outputs 30 ns* TS 5							Hard Array Logic 35 nsF TS 5						
PLUS405 ♦ Signetics (3174)							(Cont'd)						
Field Programmable Logic Sequencer, 4 Inputs, 32 AND Gates, 21 OR Gates, 6 I/O Lines 55 ns* TS 5							HAL16L2C ♦ MMI						
PLS157 Signetics (3155, 3159)							HAL16L8A-2C MMI						
PLS159 Signetics (3155, 3160)							HAL16L8B-4C MMI						
Field Programmable Logic (One device replaces several Field Programmable Array combinations)							HAL16R4A-2C MMI						
EPL VLSI Tech							HAL16R4B-4C MMI						
VP10P8 VLSI Tech							HAL16R6A-2C MMI						
VP12P6 VLSI Tech							HAL16R6B-4C MMI						
VP14P4 VLSI Tech							HAL16R8A-2C MMI						
VP16P2 VLSI Tech							HAL16R8B-4C MMI						
VP16P8 VLSI Tech							ZHAL10H8AC MMI						
VP16RP4 VLSI Tech							ZHAL10L8AC MMI						
VP16RP6 VLSI Tech							ZHAL12H6AC MMI						
VP16RP8 VLSI Tech							ZHAL12L6AC MMI						
VP20PX VLSI Tech							ZHAL14H4AC MMI						
Field Programmable Synchronous State Machine, 16-Cells 50 nsF TS 5							ZHAL14L4AC MMI						
PAL32R16M							ZHAL16C1AC MMI						
♦† MMI							ZHAL16H2AC MMI						
Field Programmable Synchronous State Machine, 32-Cells 55 nsF TS 5							ZHAL16L2AC MMI						
PAL64R32M † MMI							ZHAL16L8AC MMI						
Hard Array Logic 15 nsF TS 5							ZHAL16P8AC MMI						
HAL16L8BC MMI							ZHAL16RP4AC MMI						
HAL16R4BC MMI							ZHAL16RP6AC MMI						
HAL16R6BC MMI							ZHAL16RP8AC MMI						
HAL16R8BC MMI							ZHAL16R4AC MMI						
HAL20L8BC MMI							ZHAL16R6AC MMI						
HAL20R4BC MMI							ZHAL16R8AC MMI						
HAL20R6BC MMI							HAL12L10C ♦ MMI						
HAL20R8BC MMI							HAL14L8C ♦ MMI						
25 nsF TS 5							HAL16A4C MMI						
HAL16L8AC MMI							HAL16C1C ♦ MMI						
HAL16L8B-2C MMI							HAL16L6C ♦ MMI						
HAL16R4AC MMI							HAL16P8A MMI						
HAL16R4B-2C MMI							HAL16RA8C MMI						
HAL16R6AC MMI							HAL16RP4AC MMI						
HAL16R6B-2C MMI							HAL16RP6A MMI						
HAL16R8AC MMI							HAL16RP8A MMI						
HAL16R8B-2C MMI							HAL16X4C ♦ MMI						
HAL20L8AC MMI							HAL18L4C MMI						
HAL20R4AC MMI							HAL20C1C MMI						
HAL20R6AC MMI							HAL20L2C MMI						
HAL20R8AC MMI							HAL20RA10 MMI						
30 nsF TS 5							HAL20RS10 MMI						
HAL16L8AM † MMI							HAL20RS4 MMI						
HAL16R4AM † MMI							HAL20RS8 MMI						
HAL16R6AM † MMI							HAL20S10 MMI						
HAL16R8AM † MMI							HAL10H8M ♦† MMI						
HAL20L10AC MMI							HAL10L8M ♦† MMI						
HAL20L8AM † MMI							HAL12H6M ♦† MMI						
HAL20R4AM † MMI							HAL12L10M						
HAL20R6AM † MMI							♦† MMI						
HAL20R8AM † MMI							HAL12L6M ♦† MMI						
HAL20X10AC MMI							HAL14H4M ♦† MMI						
HAL20X4AC MMI							HAL14L4M ♦† MMI						
HAL20X8AC MMI							HAL14L8M ♦† MMI						
35 nsF TS 5							HAL16A4M ♦† MMI						
HAL10H8C ♦ MMI							HAL16C1M ♦† MMI						
HAL10L8C ♦ MMI							HAL16H2M ♦† MMI						
HAL12H6C ♦ MMI							HAL16L2M ♦† MMI						
HAL12L6C ♦ MMI							HAL16L6M ♦† MMI						
HAL14H4C ♦ MMI							HAL16L8M ♦† MMI						
HAL14L4C ♦ MMI							HAL16R4M ♦† MMI						
HAL16H2C ♦ MMI							HAL16R6M ♦† MMI						
(Continued)							(Continued)						

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

\*Macrocell

♦ Available in Surface Mount Package

Bold face indicates additional data is provided on the page noted.



ASIC/CUSTOM—Programmable Logic (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line	Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	Line			
Hard Array Logic							Programmable Memory-Based Sequencer									
	45 nsF	TS	5	HAL18L4M	◊† MMI	(Cont'd)		12 nsF	TS	5	PMS14R21	MMI	60			
				HAL20L2M	◊† MMI			20 nsF	TS	5	PMS14R21A	MMI				
	50 nsF	TS	5	HAL20L10C	MMI	5	Programmed at Factory, 14 Inputs, 96 Product Terms 150 nsF — 5					DM7575	† National	65		
				HAL20X10C	◊ MMI						DM7576	† National				
				HAL20X4C	◊ MMI	10					DM8575	National	65			
				HAL20X8C	◊ MMI						DM8576	National				
	60 nsF	TS	5	HAL10H8-2C	MMI	15	Programmed Synchronous State Machine, 16-Cells					40 — 5	HAL32R16C	MMI	65	
				HAL10L8-2C	MMI						50 — 5	HAL32R16M	† MMI			
				HAL12H6-2C	MMI	20	Programmed Synchronous State Machine, 32-Cells					50 — 5	ZHAL64R32C	MMI	65	
				HAL12L6-2C	◊ MMI						55 — 5	HAL64R32M	† MMI			
				HAL14H4-2C	MMI	25	Stand-Alone Microsequencer (SAM), 76 P-terms, 448x36 word microcode EPROM, 24-Pins.					35 nsF CMOS/TTL	5	EPS444	◊† Altera	65
				HAL14L4-2C	MMI								EPS448	◊† Altera		
				HAL16C1-2C	MMI	30	User configurable microprocessor peripheral device, 8-bit bus port extendable to 16 and 32-bits, supports 25 MHz processors.					40 nsF CMOS/TTL	5	EPB1400	◊† Altera	65
				HAL16H2-2C	MMI											
				HAL16L2-2C	MMI	35										65
				HAL20L10M	◊† MMI											
				HAL20X10M	◊† MMI	40										65
				HAL20X4M	◊† MMI											
				HAL20X8M	◊† MMI	45										65
	80 nsF	TS	5	HAL10H8-2M	† MMI											
				HAL10L8-2M	† MMI	50										65
				HAL12H6-2M	† MMI											
				HAL12L6-2M	◊† MMI	55										65
				HAL14H4-2M	† MMI											
				HAL14L4-2M	† MMI	60										65
				HAL16C1-2M	† MMI											
				HAL16H2-2M	† MMI	65										65
				HAL16L2-2M	† MMI											
Hard Array Logic, CMOS																
	25 nsF	TS	5	ZHAL12L10A	MMI	30										65
				ZHAL14L8A	MMI											
				ZHAL16L6A	MMI	35										65
				ZHAL18L4A	MMI											
				ZHAL20C1A	MMI	40										65
				ZHAL20L2A	MMI											
				ZHAL20L8A	MMI	45										65
				ZHAL20RS4A	MMI											
				ZHAL20RS8A	MMI	50										65
				ZHAL20R4A	MMI											
				ZHAL20R510A	MMI	55										65
				ZHAL20R6A	MMI											
				ZHAL20R8A	MMI	60										65
				ZHAL20S10A	MMI											
	35 nsF	TS	5	ZHAL20L10A	MMI	65										65
				ZHAL20X10A	MMI											
				ZHAL20X4A	MMI	70										65
				ZHAL20X8A	MMI											
Logic Device																
	25 nsF	TS	5	PLDC20RA10-25	Cypress (4218)	75										65
	30 nsF	TS	5	PLDC20RA10-30	Cypress (4218)											
	35 nsF	TS	5	PLDC20RA10-35	Cypress (4218)	80										65
Programmable Gate Arrays, CMOS																
	20 nsF	TS	5	XC3020	◊† Xilinx (4344)	85										65
				XC3030	† Xilinx (4344)											
				XC3042	† Xilinx (4344)	90										65
				XC3064	† Xilinx (4344)											
				XC3090	◊† Xilinx (4344)	95										65
	25 nsF	TS	5	XC2018-70	◊† Xilinx (4346)	100										65
				XC2064-70	◊† Xilinx (4346)											

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

•Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Standard Cells

Manufacturer Device Process	Geometry (μm)	Interconnections		Delay 2-Input NAND Gate <sup>1</sup> (ns)	A/D	D/A	Cell Library Includes					Supply Voltage, V	Comments	Library or Process Name	Source	Line
		Metal	Poly				Op Amp	Core μP	RAM	ROM	PLA					
Texas Instruments CMOS	1.0	2	1	0.5					x	x		5		TSC500 Series ◊† TI SystemCell ◊† TI	(4317)	
	2	2	1	1.2	x	x	x		x	x	x	5				
Advanced Linear Devices SiGateCMOS	5	x	x		x	x	x					± 1 to ± 6 V	STD Cell Analog, other members of cell library available	SiGateCMOS ◊† AdvLinear		
Si-Gate CMOS	5	1	1		x	x	x					± 1 to 6	Standard Cell Analog, other members of cell library available.	CMOS ◊† AdvLinear		
Alphatron CMOS, Si-Gate	3	1	1	2		x	x		x	x	x	4–6	Emulates 74LS SSI/MSI	ALPHAMAP	Alphatron	5
Barvon Bi-CMOS	2	2		1.5	x	x	x		x	x	x	3 to 40		BB200	Barvon	10
CMOS, Si-Gate	1.5	2		0.9	x	x	x		x	x	x	3 to 10		BC6000	Barvon	
	2	2		1.5	x	x	x		x	x	x	3 to 10		BC2000	Barvon	
	2	2		1.3	x	x	x		x	x	x	3 to 10		BC4000	◊ Barvon	
	3	2		1.8	x	x	x	x	x	x	x	3 to 10	Core μP	BHC Library	Barvon	
HAMOS	3	2												BHN Library	Barvon	
California Micro Devices BiCMOS	2	2		1.1			x		x	x	x	3 to 7	Up to 15,000 gates	CSC700	CMD ASIC (4216)	15
CMOS, Si-Gate	1.2	2		0.47			x	x	x	x	x	3 to 7	Up to 50,000 gates	CSC500	CMD ASIC (4216)	
	1.5	2		0.6			x	x	x	x	x	3 to 7	Up to 40,000 gates	CSC400	CMD ASIC (4216)	
	2	2		1.1			x	x	x	x	x	3 to 7	To 18,000 gates	CSC300	CMD ASIC (4216)	
	2	2	2	1.1			x		x	x	x	3 to 7	Up to 16,000 gates	CSC600	CMD ASIC (4216)	
	2.5	1		2.2			x		x	x	x	3 to 7	To 7500 gates	CSC200	CMD ASIC (4216)	
Calmos CMOS	1.2	2	1	0.5				x	x	x	x	5	Rad Hard, VHSIC Compatible	Standard Cell CMOS	Calmos Calmos	20
	2	1	1	1.5				x	x	x	x	5		CMOS Library	Calmos	
	3	1	1	2				x	x	x	x	5		CMOS Library	Calmos	
CMOS P-Well	1.6	4	3.2	0.8			x	x	x	x		1	MetalUPD1	DMC1.6	Calmos	25
	2	5	4	1				x	x	x	x	5	Dual Metal	DMC2	Calmos	
	2.4	6.4	4.8	1.2			x	x	x					SMC2.4	Calmos	
	3	8	6	1.5				x	x	x		5	Single Metal	SMC3	Calmos	
Barvon CMOS, Si-Gate	3	2	1.8	x	x	x	x	x	x	x	3 to 10	Core μP		BHC Library	Barvon	
Custom Integrated Circuits CMOS, Si-Gate	3	2	1	2 nS		x	x		x	x	x	2.2–9.0		LPHDI	CIC	
EXAR CMOS	2	2	2	1	x	x	x					3 to 15	Includes Oscillators, Switched Capacitor Filters and Phase Locked Loops	N2000 P3000	Exar ◊ Exar	
	3	2		1			x					5	49 Digital Cells, 6 Analog Cells			
Fairchild CMOS, Si-Gate	2	2	1	1	x	x	x	x	x			5.0		FACT	Fairchild	30

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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## ASIC/CUSTOM—Standard Cells (Cont'd)

Manufacturer Device Process	Geometry (μm)	Interconnections Metal	Poly	Delay 2-Input NAND Gate <sup>1</sup> (ns)	A/D	D/A	Op Amp	Cell Library Includes Core μP	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source	Line
Fujitsu Microelectronics CMOS, Si-Gate	1.5	3	1	0.85					x	x	x	x	5	UH Library	Fujitsu	5
	2.2	2	1	2.2					x	x	x	3 to 6	Digital cells match gate array macro library.	VH Library	Fujitsu	
	2.8	2	0	3.5					x	x		5		CMOS Library	Fujitsu	
	1.3	2/3	1	0.7				x	x	x	x	5	Cell logic is compatible with the UHB library	AU Library	Fujitsu	
	1.8	2	1	1.6					x	x	x	3 to 6	Digital cells match gate array macro library.	AV Library	Fujitsu	
GE Semiconductor CMOS, Si-Gate	2	2		1.7 *			x		x	x		2 to 5.5		ISC20000	GE/Intersil	10
	3	2	1	<2								2 to 10		CMOS Library	GE/Intersil	
Gigabit Logic GaAs MESFET	1	2		0.07								-5.2, -3.4	Custom Foundry Services Available	SC1	† GigaBit	15
Goldstar HCMOS	1.5	2		0.7					x	x		5		GSC6000	GoldStar (4243)	
	2	2		1.2					x	x		5		GSC2000	GoldStar (4243)	
		2		1					x	x		5		GSC4000	GoldStar (4243)	
Gould CMOS	2	2	2		x	x	x		x	x	x	5		SoftCells	Gould	20
	3	1	2		x	x	x		x	x	x	± 5		LB	Gould	
		1	2		x	x	x		x	x	x	± 5		LF	Gould	
		1	2		x	x	x		x	x	x	± 5		LK	Gould	
		1	2		x	x	x		x	x	x	± 5		LL	Gould	25
		1	2		x	x	x		x	x	x	± 5		LO	Gould	
CMOS, Si-Gate	2μm	2M	1P	1.2*					x	x	x	2.5-5.5	PLA available	CBD	Gould	
	3	1	1	2.6								2.5 to 5.5	Speed is measured at 25°C, 5 V, 1 pF load	CCB	Gould	
		1	1	5			x		x			2.5 to 10		SLM CMOS	† Gould	30
		1	2	2.6	x	x	x					2.5 to 10.0	Speed is measured at 25°C, 5 V, 1 pF load	CCF	Gould	
		2	1	2.4					x	x	x	2.5 to 5.5	Speed is measured at 25°C, 5 V, 1 pF load	CCD	Gould	
		2	1	4.8			x		x			2.5 to 6.5		DLM CMOS	† Gould	
	3μm	1M	1P	2.6*					x	x	x	2.5 to 5.5				30
		1M	2P	2.6*	x	x	x					2.5-5.5		CCB	Gould	
												2.5-10	5 V digital logic can interface with 10 V analog functions	CCF	Gould	
	2	2	1	1.2					x	x	x	2.5 to 5.5				
													Speed is measured at 25°C, 5 V, 1 pF load	CCB	Gould	30
CMOS	3	2	2		x	x	x	x	x	x		10 to 30	Mixed Mode (analog and digital process)	CCI	Gould	
GTE Microcircuits CMOS, Si-Gate	2	2	1	1.5	x	x	x	x	x	x	x			ADV-CMOS	CMD Micro	30
Harris CMOS	1.5	2	1	1.5				x	x	x		-0.5 to 7.0		HSC250	† Harris (4248)	
	2	2	1	1								5	Radiation Hardened	HSCDLMRH	± Harris	30

(Continued)

<sup>1</sup> Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

## ASIC/CUSTOM—Standard Cells (Cont'd)

Manufacturer Device Process	Geometry ( $\mu\text{m}$ )	Interconnections Metal	Poly	Delay 2-Input NAND Gate <sup>1</sup> (ns)	A/D	D/A	Op Amp	Cell Library Includes Core $\mu\text{P}$	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source	Line
Harris CMOS, Si-Gate	2.5			3									Radiation Hardened, Up to 5000 gatesu	HSDXXXRH ‡ Harris	(2721)	5
	3	1	1	2								4.5 TO 5.5	Radiation Hardened	HSCXXXRH ‡ Harris	(2721)	
1.0	2	1	0.9					x	x	x		-0.5 to 7.0		HSC200 † Harris		
Harris Microwave Semiconductor GaAs	1.0	2		0.18								-2, +2.5	GaAs Std. Cell, 1-Volt pinch-off	HMS	Harris	
Hughes Aircraft CMOS, Si-Gate	2.5											4 to 10		HCMOS Library † Hughes		
IC Options, Inc. CMOS	1.5	2	1	1.2			x		x	x		3 to 7	95 SSI/MSI Cell Functions	ICO-Cell	IC Options	10
Integrated Circuit Design Centre CMOS, Si-Gate	6	1	1	7			x					3-11	ISO Cell Generic Library	CMOS	ICDC	
Integrated Circuit Systems CMOS, Metal Gate	7.5	1		30			x		x	x		5 to 18		CMOS Library IntCirSys	(4256)	
CMOS, Si-Gate	2	2	1	10-20			x		x	x		2 to 5		CMOS LIBRARY IntCirSys		
	2 $\mu\text{m}$	2	1	1.5-4	x	x	x	x	x	x	x	4.5-5.5	ICS Custom Library	CMOS Library IntCirSys	(4256)	
	3	2	1	4	x	x	x	x	x	x	x	5	ICS Custom Library	CMOS Library IntCirSys	(4256)	
	5	1	1	10	x	x	x		x			5 to 10	ICS Custom Library	CMOS Library IntCirSys	(4256)	
NMOS, Metal-Gate	4.5	1		20	x	x	x	x	x	x	x	5 to 10		CMOS Library IntCirSys	(4256)	
		1		20				x	x	x	x	5 to 10		NMOS Library † IntCirSys	(4256)	
	5	1	1	20	x	x	x	x	x	x	x	5 to 10		CMOS Library IntCirSys	(4256)	
		1	1	20					x	x	x	5 to 10		NMOS Library † IntCirSys	(4256)	
NMOS, Si-Gate	3	1	1	4	x	x	x	x	x	x	x	5	ICS Custom Library	CMOS Library IntCirSys	(4256)	20
Intel CMOS, Si-Gate	2	1	1	1.0				x	x	x	x	5	Currently in Beta sites	CHMOS-1 Library Intel		
Int'l Microcircuits CMOS, Si-Gate	3	2	1	2	x	x	x		x	x	x	3.5 to 8		CMOS Library IMI		
Int'l Microelectronic Prod CMOS	2	2		1.0					x	x	x	5		Impel Library IMP		
CMOS, Si-Gate	3	1	2.5						x	x	x	5 to 10		Impel Library † IMP		
		2	2	2.5	x	x	x		x	x	x	5 to 10	Analog and Digital	Impel Library † IMP		
LSI Logic HCMOS	1.5	2M	1P	0.7				x	x	x		3 to 6	High Density, High Performance ASIC; RAM and ROM capabilities; up to 100,000 usable gates.	LSC15	LSI Logic (4271)	25
Marconi Electronic Devices CMOS, Si-Gate	3	1	1	3			x		x	x		3 to 8	200°C operation	CELLMOS † Marconi		
	5	1	1	8			x		x	x		3 to 10	200°C operation	CELLMOS † Marconi		
CMOS, SOS	3	1	1	2			x		x	x		3 to 8		CELLSOS ‡ Marconi		
	5	1	1	5			x		x	x		3 to 11		CELLSOS ‡ Marconi		
Master Logic CMOS, Metal-Gate	4	1		15	x	x	x					2 to 7		MALV Series † MasterLogic		
CMOS, Si-Gate	4	1		3	x	x						2 to 7		MASG Series † MasterLogic		

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## ASIC/CUSTOM—Standard Cells (Cont'd)

Manufacturer Device Process	Geometry ( $\mu\text{m}$ )	Interconnections Metal	Poly	Delay 2-Input NAND Gate <sup>1</sup> (ns)	A/D	D/A	Op Amp	Cell Library Includes Core $\mu\text{P}$	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source	Line	
MCE Semiconductor Bipolar, J. I.	5	1	1	12.5	x	x	x					to 75	Library includes some 75V devices	UniCELL	† MCE		
CMOS, Metal-Gate	5	1		10			x					1 to 18		UniCELL MGA	† MCE		
Micro-Rel Inc. BIP, J.I., D.I.	8	1										100		High Voltage	‡ Micro-Rel		
BIP, J.I, D.I	8	1										40	MOS capacitor available, dielectric isolation, 1.3 Kohms/square CrSi resistors	High Voltage	Micro-Rel		
BIP, J.I, D.I.	8	1										20	100Kohms/square CrSi resistors available	Low Voltage	‡ Micro-Rel	5	
CMOS	3	2	1	2.5	x	x	x					2-10	MOS capacitor available, 1.3 Kohms/square CrSi resistors 200ppm/C° for linear applications.				
	5	1	1	5	x	x	x					2-18	Same as 3 $\mu$ CMOS	D3 Library D5 Library	† Micro-Rel † Micro-Rel		
Mitsubishi Electronics America CMOS	1.3	2	1	0.9	x	x	x	x	x	x	x	5		CMOS	◊ Mitsubishi		
	2	2	1	1.4	x	x	x	x	x	x	x	5		CMOS	◊ Mitsubishi		
NCM Corp CMOS, Metal-Gate	7.5	1	0	20			x		x	x	x	1.5 to 15		2000 Series	† NCM	10	
CMOS, Si-Gate	3	1	1	3			x		x	x	x	3.5 to 12		4000 Series	NCM		
NCR Corp. CMOS Si-gate	2	1 or 2	1	1.5 to 4	x	x	x	x	x	x	x	4.5 to 5.5		NCRVS2000	† NCR		
	3	1 or 2	1	3 to 5	x	x	x	x	x	x	x	4.5 to 5.5	Some analog is $\pm 5.0\text{V}$ dual supply	NCRVS3000	† NCR		
OKI CMOS	2	2						x	x	x				MSM91000	OKI	15	
	3	2						x	x	x				MSM90000	OKI		
	1.5	2	1	1.2					x	x	x	5		91V000	◊ OKI		
	2	2	1	1.7					x	x	x	5		91H000	◊ OKI		
Plessey Semiconductor CMOS	2	2	1	1.7	x	x			x	x	x	5	RAM, ROM, PLA are software generated	Megacell	Plessey	20	
CMOS, Si-Gate	2.5	2		1.4	x	x	x	x	x	x	x	3 to 7		CMOS	Plessey		
	5	1	1	6	x	x	x					3 to 7		CMOS	Plessey		
NMOS	5	1		20								5		NMOS	Plessey		
RCA CMOS	2	2	1	1				x	x	x	x	6		PACMOS III D	GE/RCA		
	3	1	1	2.5								7		PaCMOS II	GE/RCA		
		2	1	2.5					x	x		7	Double-level metal	PaCMOS IID	GE/RCA		
CMOS, Si-Gate	3	1	1	5			x					3 to 7		PaCMOS-2	GE/RCA	25	
	7	1	1	20			x					3 to 12		PaCMOS-C2L	GE/RCA		
CMOS, SOS	3	1	1	4			x					3 to 12		SOS-2 Library	‡ GE/RCA		
	4	1	1	1								7	Rad Hard	PaCMOS SOS	‡ GE/RCA		
	5	1	1	8			x					3 to 12		SOS-1 Library	‡ GE/RCA		
Ricoh CMOS, Si-Gate																	
	2	2		2					x	x	x	-0.3 to 7	Full CAD Support System	RSC20	Ricoh	30	
SGS-ATES Bipolar MTL <sup>3</sup> V	6	2		25		x	x		x	x		2 to 10		Zodiac	SGS		

<sup>1</sup> Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

## ASIC/CUSTOM—Standard Cells (Cont'd)

Manufacturer	Device Process	Geometry (μm)	Interconnections Metal	Poly	Delay 2-Input NAND Gate <sup>1</sup> (ns)	A/D	D/A	Op Amp	Cell Library Includes Core μP	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source	Line
Sierra Semiconductor	CMOS	2	2	2	1.2	x	x	x	x	x	x	x	5	(2 poly layers with EEPROM)	CMOS Library	Sierra	5
			2	2	1.2	x	x	x	x	x	x	x	5	Includes EEPROM and SCF	SC70000	Sierra	
		3	2	2	2	x	x	x					10	EEPROM available	CMOS Library	Sierra	
			2	2	2	x	x	x					10	Includes EEPROM and SCF.	CMOS 3 Micron	Sierra	
	CMOS, Si-Gate	1.5	2	2		x	x	x	x	x	x	x	4.5–5.5	EEPROM Included in process.	SC8000	° Sierra	
Signetics	Bipolar	5	2		3.5								5	Medium power	EPL1	† Signetics	10
			2		5								5	Low power	EPL2	† Signetics	
			2		6								5		ISL	† Signetics	
	CMOS, Si-Gate	3	2	1	8								2 to 6	High Speed	INTER	Signetics	
		4	1	1	8								3 to 15	Medium Speed	INTER	Signetics	
Silicon Systems	CMOS, Si-Gate	3	2	1	3	x	x	x	x	x	x	x	5		CMOS Library	SiliconSys	
Siliconix	CMOS, Si-Gate	3	2	2	3		x	x		x	x		3 to 6		ISO-3 Library	Siliconix	
		5	2	2	5.5		x	x		x	x		3 to 14		ISO-5 Library	Siliconix	
Standard Microsystems	CMOS Si-Gate	2	2	1	1.5				x	x	x	x	4 to 6		Customation III	SMC	15
		3	1	1	2	x	x	x	x	x	x	x	3.5 to 10		Customation II	° SMC	
Texas Instruments	CMOS, Si-Gate	2	2	1	1.2	x	x	x		x	x	x	5		SYSTEMCELL	TI	
Thomson Components-Mostek	CMOS, Si-Gate	2	2	0	1 *				x	x	x	x	3–6	Military 883C processing available.	TSSB Series	Thomson	
		3	2	0	1.5				x	x	x	x	3–6	Military 883C processing available.	TSSC Series	Thomson (4326)	
Thomson-Mostek	CMOS, Si-Gate	2	2	1	7.4	x	x	x					5,10	Analog and Digital	TSGSM Series	Thomson	
TLSI	CMOS	3	1	1	2.5			x		x	x		2.5 to 5.0		CMOSII Library	TLSI	20
			2	1	2.5			x		x	x		2.5 to 5	Double-Metal, High Density	CMOS II-DM	TLSI	
		5	1	2	7	x	x	x		x	x		5 to 12	Switched Capacitor, Analog Functions	CMOS-DP	TLSI	
	CMOS Si-Gate	3	1	1	2.5			x		x	x		2.5 to 5		CMOS II	TLSI	
		5	1	1	7	x	x	x		x	x		5 to 12		CMOS	TLSI	
	NMOS	4	1	1	5			x		x	x		5		NMOS Library	TLSI	25
		4	1	1	5			x		x	x		5		NMOS	TLSI	
Toshiba	CMOS	1.5	2		1.0								5		TC23SC	Toshiba (4327)	
		2	2		1.5								5		TC21SC	Toshiba (4327)	
		2	2		1.5				x	x	x	x	5		TC22SC	Toshiba (4327)	
TriQuint	GaAs	1	2		0.15									± 4	Q-LOGIC	TriQuint	30
Unicorn Microelectronics	CMOS, Si-Gate	1.5	2	1	1.0				x	x	x	x	5	Core μPs, Supercells	COMPILE	Unicorn	
		2	2	1	1.4				x	x	x	x	5	RAM, ROM	COMPILE	Unicorn	
		3	2	1	2.2				x	x	x	x	5	FIFO, Datapath Modules	COMPILE	Unicorn	

(Continued)

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

Bold face indicates additional data is provided on the page noted.



## ASIC/CUSTOM—Standard Cells (Cont'd)

Manufacturer Device Process	Geometry ( $\mu\text{m}$ )	Interconnections Metal	Poly	Delay 2-Input NAND Gate <sup>1</sup> (ns)	A/D	D/A	Op Amp	Core $\mu\text{P}$	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source	Line
Unicorn Microelectronics Si-GATE CMOS 1.5 $\mu$ –3 $\mu$		2	1	2.2				x	x	x	x		Silicon Compiler, 5 Foundry Sources.	COMPILE ° Unicorn		(Cont'd)
VLSI Design Associates CMOS, Si-gate	2 3 5	2 1 1	1 1 2	2 3 7					x x x	x x x	x x x	3 to 5 5 3 to 12	Multiple Sourcing	MULTI-CELL2 VDA MULTI-CELL3 VDA MULTI-CELL5 VDA		
VLSI Microsystems, Inc. CMOS	2	2 2	1 2	1.1 0.9 *		x x		x x	x x	x x		3 to 7 4.5 to 5.5		CMOS VMI CMOS VMI		5
VLSI Technology CMOS CMOS, Si-Gate HCMOS HMOS	2 3 1.5 1.5 3	2 2 2 1 1		2 5 4				x x x x	x x x x	x x x x		5 5 5 5	Configurable cells Configurable cells	VSC Series VLSI Tech CMOS Library VLSI Tech CMOS Library VLSI Tech HMOS Library VLSI Tech HMOS Library VLSI Tech		10
VTC Bipolar	2			0.4		x x			x x	x x		–5 to 12 –5.2 to 5	106 Digital cells, 73 analog cells 78 Cells	VL1000 VTC VL2000 VTC	(4340) (4338)	
CMOS	1.25	2	1	0.5				x x	x x	x x		5	Over-the-cell routing, radiation-hardened process available.	VL5000 VTC	(4334)	
Waferscale CMOS	1.2	1 2	2 2	0.60 0.85				x x	x x	x x	x x	3 to 6 3 to 6	Library includes SSI/MSI elements plus CMOS EPROM macro cells. Specializes in large block cells. Also contains EPROM cells.	Modular-Cell Waferscale Modular-Cell Waferscale		15
	1.6	1 1	2 2	0.85 0.85				x x	x x	x x	x x	3 to 6 3 to 6	Process includes EPROM Library includes SSI/MSI elements plus CMOS EPROM macro cells.	Modular-Cell Waferscale Modular-Cell Waferscale		
Western Design Center CMOS	1.5	2 2 2 2	1 1 1 1	1 1 1 1				x x x	x x x			1.8 to 6 1.8 to 6 1.8 to 6 1.8 to 6	64, 128, 192, 256 x 8 static 1K, 2K, 3K, 4K, 6K, 8K x 8 static W65C02 8-bit static and pseudostatic W65C816 16-bit static and pseudostatic	W65CRAM WDC W65CROM WDC W65C02 WDC W65C816 WDC		20
	2.4	2 2 2 2	1 1 1 1	3 3 3 3				x x x	x x x			1.8 to 6 1.8 to 6 1.8 to 6 1.8 to 6	64, 128, 192, 256 x 8 static 1K, 2K, 3K, 4K, 6K, 8K x 8 static W65C02 8-bit static and pseudostatic W65C816 16-bit static and pseudostatic	W65CRAMx2 WDC W65CROMx2 WDC W65C02x2 WDC W65C816x2 WDC		25
	3	2 2 2 2	1 1 1 1	4 4 4 4				x x x	x x x			1.8 to 6 1.8 to 6 1.8 to 6 1.8 to 6	64, 128, 192, 256 x 8 static 1K, 2K, 3K, 4K, 6K, 8K x 8 static W65C02 8-bit static and pseudostatic W65C816 16-bit static and pseudostatic	W65CRAMx3 WDC W65CROMx3 WDC W65C02x3 WDC W65C816x3 WDC		30
ZyMOS CMOS, Metal-Gate	6	1	1	12.2								1.1 to 6		Zy20000 † ZyMOS		
CMOS, Si-Gate	3 5	1 1 1	1 1 1	1.6 5.8	x x	x x		x x	x x	x x	x x	1.1 to 5.5 1.1 to 5.5	80C49 80C49	Zy50000 † ZyMOS Zy40000 † ZyMOS		

<sup>1</sup> Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

ASIC/CUSTOM—Gate Array Design Automation Tools

Array Source									Array Source										
Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Resimulation	Design Tool	Source	Line		Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Resimulation	Design Tool	Source	Line			
AMCC									Fujitsu Microelectronics (Cont'd)										
All AMCC products	x	x		x	LOGICIAN	Daisy	5		B240-B2000 Bipolar	x	x			GATE MASTER	Daisy	45			
	x	x		x	IDEASTATION	Mentor				x	x			GATE STATION	Mentor				
	x	x		x	SCALDSYSTEM	Valid				x	x			SCALD	Valid				
	x	x		x	CAE2000	Tek/CAE				x	x			DASH	FutureNet				
	x	x		x	TEGAS	Calma				x	x	x	x	LCAD	Fujitsu				
		x			GAWS	Tektronix													
	x	x	x	x	Merlyn-G	Tek/ICO													
Array Technology																			
DHS	x	x	x	x	GATE STATION	Mentor	10		AV, AVB, AVM, UH, UM, UHB, ECL, BiCMOS, LSTTL	x	x				Mentor	50			
HCD	x	x	x	x	GATE STATION	Mentor				x	x				Daisy				
California Devices																			
CHA	x	x			Daisy, Mentor, FutureNet, Vax	CalDevices	15		AV, AVB, UHB	x	x	x	x		HP	60			
DLM	x	x			Daisy, Mentor, FutureNet, Vax	CalDevices				x	x				Tektronix				
DLM XXXXX	x	x			LOGICIAN	Daisy				x	x				Intergraph				
	x	x			PERSONAL														
	x	x			GATEMASTER	Daisy													
	x	x			IDEA STATION	Mentor													
CHA XXXXX	x	x			LOGICIAN	Daisy	20		All CMOS, ECL, LSTTL, and BiCMOS Devices					LCAD	Fujitsu	55			
	x	x			PERSONAL					x	x	x							
	x	x			LOGICIAN	Daisy													
	x	x			GATEMASTER	Daisy													
	x	x			IDEA STATION	Mentor													
CSBXXXX	x				FutureNet	CalDevices	25		General Electric							65			
	x				FutureNet	Datal/O				IGC 10000	x	x			GATE MASTER		Daisy		
	x	x			Gatemaster	CalDevices						x	x	x	CADEXEC		GE Semi		
	x	x			Gatemaster	Daisy				IGC 20000 2μ, 2LM, CMOS	x	x			LOGICIAN		Daisy		
	x	x			Logician	Daisy					x	x			PERSONAL		Daisy		
	x	x			Personal		30			x	x			CAE-1, CAE-2	PCAD	70			
	x	x			Logician	Daisy					x	x			DASH		FutureNet		
	x	x			Idea Station	Mentor					x	x			TEGASTATION		Calma		
											x	x	x	x	GATE STATION		Mentor		
												x	x	x	TEGAS		Calma		
CMD ASIC Division																			
G50000B	x	x	x	x	ALIS	CMD Micro	35		Gould							75			
EXAR Corp.																			
XR-30000 Series	x	x	x	x	GATE MASTER	Daisy				GA-XXXXD, GB-XXXXD	x	x	x	x	CAD		Gould		
XR-CM Series	x	x	x	x	GATE MASTER	Daisy					x	x	x	x	GATEMASTER		Daisy		
											x	x							
Fairchild																			
FGCXXXX, FGEXXXX	x	x	x	x	FAIRCAD	Fairchild	40									80			
	x	x		x	GATE MASTER	Daisy													
	x	x		x	GATE STATION	Mentor				GTE Microcircuits									
	x	x		x	GATE DESIGNER	Valid				G50000B	x	x			GATEMASTER		Daisy		
	x	x		x	CAE-2000	Tek/CAE				Harris Semiconductors									
	x	x		x	DASH II	FutureNet			HGA-XXXX	x				GATEMASTER	Daisy				
Fujitsu Microelectronics																			
All CMOS	x	x	x	x	GATE MASTER	Daisy	40		Hitachi							85			
	x	x	x	x	GATE STATION	Mentor				HD 61	x	x	x	x	HITACHI DA SYSTEM		Hitachi		
	x	x			SCALD	Valid				HD61	x	x			LOGICIAN		Daisy		
	x	x			DASH	FutureNet				HD 27	x	x	x	x	HITACHI DA SYSTEM		Hitachi		
	x	x	x	x	LCAD	Fujitsu					x	x			LOGICIAN		Daisy		
(Continued)									(Continued)										

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FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION

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ASIC/CUSTOM—Gate Array Design Automation Tools (Cont'd)

Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Resimulation	Design Tool	Source	Line	Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Resimulation	Design Tool	Source	Line
Hitachi	HG 61H	x	x	x	x	HITACHI DA SYSTEM	Hitachi	(Cont'd)	LSI Logic	LL5000, LL7000, LL9000, LCA10000, LSC15, LRH9000	x	x	x	x	MDE	LSI Logic	(Cont'd)
		x	x			LOGICIAN	Daisy			LL5000, LL7000, LL9000	x	x			Design Verifier	LSI Logic	
		x	x			IDEA STATION	Mentor				x	x					
Honeywell	HM1000R	x	x			GATE STATION	Mentor	5	Marconi	MA8304	x	x	x	x	Ideastation	Mentor	
	HE2000	x	x	x	x	GATE STATION	Mentor				x	x			Logician	Daisy	
	HM3000/RAM	x	x	x	x	GATE STATION	Mentor				x		x		CASS	SilvarLisco	
	HM3500(R)	x	x	x	x	GATE STATION	Mentor			MA2000, MA2000A	x	x	x	x	Hilo	GenRad	50
	HT5000	x	x	x	x	GATE STATION	Mentor				x	x			Array 1	Marconi	
	HE8000	x	x	x	x	GATE STATION	Mentor						x		Array 2	Marconi	55
	HC3500(R)	x	x	x	x	GATE MASTER	Mentor	10		MS200A	x	x			SCALD	Valid	
Hughes	HHGA XXXX	x	x			IDEA 1000	Mentor			MA4000	x	x	x	x	Ideastation	Mentor	
	HVGA XXXX	x	x			LOGICIAN	Daisy				x	x			Logician	Daisy	
	HSGA XXXX	x	x			TEXSIM	Calma								CASS	SilvarLisco	
	HHGA XXXX			x		GALA	Hughes	15				x			Hilo	GenRad	60
	HVGA XXXX			x		GALA	Hughes			MA9000	x	x	x	x	Ideastation	Mentor	
	HSGA XXXX			x		GALA	Hughes			x	x				Logician	Daisy	
	HHGA XXXX		x			DANA	Hughes								CASS	SilvarLisco	
	HVGA XXXX		x		x	DANA	Hughes				x		x		Hilo	GenRad	65
	HSGA XXXX		x		x	DANA	Hughes					x		2	Array	Marconi	
iLSi	CB-3XXX	x	x			GATE MASTER	Daisy	20	Matra Design Systems	MA-0250 to MA-5000	x	x	x	x	MDS	Matra	
		x	x			IDEA STATION	Mentor										
		x				DASH	FutureNet		Micro-Rel	5µm CMOS 3 +	x	x				Calma	
	CA-2XXX	x	x			GATE MASTER	Daisy						x			Daisy	
		x	x			IDEA STATION	Mentor										
		x				DASH	FutureNet	25	Mitsubishi Electronics America	All gate arrays	x	x			LOGICIAN	Daisy	70
International Microcircuits, Inc.	IMI6000	x	x	x	x		IMI				x	x			IDEASTATION	Mentor	
	G90000	x	x	x	x		IMI				x	x			SCALDSYSTEM		
	G70000	x	x	x	x		IMI				x	x			DASH	FutureNet	
	G4000	x	x	x	x		IMI				x	x	x	x	PROPRIETARY		
Laserpath Corp.	LP7000	x	x		x		Mentor	30			x	x			Series 9000	Mitsubishi	75
	LP5000	x	x		x		Mentor		Monolithic Memories Inc.	CMOS 2µM	x	x	x	x	MMI Gate		
	LP7000	x	x				Daisy								Array Design	MMI	
	LP5000	x	x				Daisy			M2064	x	x	x		System		
	LP7000	x	x				PCAD								XACT		
	LP5000	x	x				PCAD	35		M2018	x	x	x		Development	MMI	
LSI Logic	LL3000, LL5000, LL8000, LL7000, LL9000	x	x	x	x	LDS	LSI Logic								System		
		x	x			IDEA STATION	Mentor								XACT		
		x	x			SCALD									Development	MMI	
		x	x			SYSTEM	Valid								System		
		x	x			LOGICIAN	Daisy										
		x	x			IDEAL	Tek/CAE	40	Motorola	MCA2900ETL	x	x	x	x	WACC	Motorola	80
											x	x			GATEMASTER	Daisy	
	LL3000, LL5000, LL7000	x				CAE-1 (-2)	PCAD			MCA2800ALS	x	x	x	x	WACC	Motorola	
	LL8000, LL9000, LRH9000	x				DASH	FutureNet				x	x			GATE STATION	Mentor	
															GATEMASTER	Daisy	
										MCA1300ALS	x	x	x	x	WACC	Motorola	85
											x	x			GATEMASTER	Daisy	
											x				CAE-1, -2	PCAD	

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FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION

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## ASIC/CUSTOM—Gate Array Design Automation Tools (Cont'd)

Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Resimulation	Design Tool	Source	Line	Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Resimulation	Design Tool	Source	Line
Motorola	MCA500ALS	x	x	x	x	WACC	Motorola	(Cont'd)	OKI Semiconductor	70H000	x	x			Personal Logician	Daisy	50
		x	x			GATEMASTER	Daisy				x	x			Mega Logician	Daisy	
		x				CAE-1, -2	PCAD				x	x			DN3000, DN660	Mentor Valid	
	MCA2500ECL	x	x	x	x	WACC	Motorola	5			x	x			IBM PC	FutureNet	
		x	x			GATEMASTER	Daisy				x	x					
		x	x			GATE STATION	Mentor				x	x					
	MCA1200ECL	x	x	x	x	WACC	Motorola	10		70V000	x	x			Personal Logician	Daisy	55
		x	x	x	x	GATEMASTER	Daisy				x	x			Mega Logician	Daisy	
		x	x			CAE-1, -2	PCAD				x	x			DN3000, DN660	Mentor Valid	
		x				GATE DESIGNER	Valid				x	x			IBM PC	FutureNet	
	MCA600ECL	x	x	x	x	WACC	Motorola	15		70HB000	x	x			Personal Logician	Daisy	60
		x	x	x	x	GATEMASTER	Daisy				x	x			Mega Logician	Daisy	
		x	x			CAE-1, -2	PCAD				x	x			DN3000, DN660	Mentor Valid	
		x				GATE DESIGNER	Valid				x	x			IBM PC	FutureNet	
	MCA800ECL	x	x	x	x	WACC	Motorola	20		Performance Semiconductor	CMOS	x	x	x	Daisy CAD Systems	Daisy	
		x	x			GATEMASTER	Daisy										
	HCA63XX	x	x	x	x	DASH	FutureNet			Plessey	CLA5000, CLA3000	x	x	x	CLASSIC	Plessey	
		x	x	x	x	WACC	Motorola										
		x	x	x	x	GATEMASTER	Daisy										
		x	x	x	x	GATE STATION	Mentor										
		x				CAE-1, -2	PCAD										
		x				DASH	FutureNet										
	HCA62XX	x	x	x	x	WACC	Motorola	25		RCA	PA40000		x	x	RCA DESIGN SYSTEM	GE/RCA	
		x	x	x	x	GATEMASTER	Daisy								LOGICIAN	Daisy	
		x	x	x	x	GATE STATION	Mentor										
		x				CAE-1, -2	PCAD										
		x				DASH	FutureNet										
	HD6000	x	x	x	x	MIDAS	ControlData										
National Semiconductor	SCX2-WS-D-X	x	x	x	x	GATEMASTER	Daisy	30									
	SCX2-WS-M-X	x	x	x	x	GATESTATION	Mentor										
	SCX2-WS-V-X	x	x	x	x	GATE DESIGNER	Valid										
	SCX2-WS-F-X	x	x			DASH	FutureNet										
	SCX2-WS-H-X	x	x		x	HILO	GenRad										
	SCX2-WS-S-X			x		VR SYSTEM	Tek/CAE										
NCM Corp.	NCM 300XZ, NCM 7001XZ	x	x	x	x	ARIES	Applicon										
NCR Microelectronics	3μ-2 metal, 2μ-2 metal, Macrocell Arrays	x	x	x	x	GATESTATION	Mentor	35		S-MOS Systems	SLA XXXX	x	x	x	DASH LOGICIAN	FutureNet Daisy	75
		x	x			GATE MASTER	Daisy								GATESTATION	Mentor	
															GDS-II	Calma	
															BRAVO	Applicon	
	HCA63XX, HCA62XX, Gate Arrays	x	x	x	x	WACC	Motorola	40		Thomson-Mostek	GA-XXXX, GB-XXXX	x	x	x	HIGHLAND 2	Thomson	80
		x	x	x	x	GATEMASTER	Daisy					x	x	x	GATE STATION	Mentor	
		x	x	x	x	GATE STATION	Mentor					x	x	x	LOGICIAN	Daisy	
		x				CAE-1, -2	PCAD					x	x		CT1000/SILO	CaseTech	
		x				DASH	FutureNet					x	x		GATE DESIGNER	Valid	
NEC	CMOS 65XXX, ECL 63XX, TTL 61XX	x	x			LOGICIAN	Daisy	45		TriQuint	GaAs	x	x	x	TEKSTATION 2000	Tek/CAE	85
		x	x			IDEA STATION	Mentor					x	x		TEGASTATION	Calma	
		x	x			SCALD	Valid										
		x	x			CAE2000	Tek/CAE										

FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION  
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ASIC/CUSTOM—Gate Array Design Automation Tools (Cont'd)

Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Re-simulation	Design Tool	Source	Line
UMC-Unicorn		x	x	x	x	UMC-Unicorn Macrocell Library (Daisy) Unicorn		
United Technologies Microcircuits Center UTD, UTB		x x x	x	x	x	Highland Scaldsystem Ideastation Logician	UTMC Valid Mentor Daisy	5
Vatic Systems MA1, MB1, MC1, MC2, BA2 MA1, MB1, MC2, BA2, MC1 MA1, MB1, MC1, BA2, MC2 MA1, MB2, BA2		x x x x	x x	x	x	CAL-MP  GATEMASTER GATESTATION GATE DESIGNER	SilvarLisco  Daisy Mentor Valid	
VLSI Technology Inc. VGC Series		x x x x	x x x	x	x x x	VTI Tools Idea Logician Tek/CAE	Mentor VLSI Tech Mentor Daisy Tektronix	10
Xilinx XC20XX  XC30XX		x  x	x	x	x x	PGA Development System PGA Development System	  Xilinx  Xilinx	15

FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION

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## ASIC/CUSTOM—Linear & Linear/Digital Design Automation Tools

ASIC/CUSTOM																			
Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Re-simulation	Design Tool	Source	Line		Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Re-simulation	Design Tool	Source	Line	
ECI Semiconductor	Bipolar CMOS	x				Future Net	Datal/O			Semicustom Arrays Modula—LA250 Series, LA200 Series								45	(Cont'd)
	Bipolar CMOS		x			SPICE 3A.7	Datal/O				x	x	x	x		CV	CompVision		
	Bipolar CMOS		x			Crystal	Datal/O				x	x	x	x		APLE860	Applicon		
	Bipolar COS			x		Magic	Datal/O												
European Silicon Structures		x	x	x	x	Solo 1200	European	5		Sierra Semiconductor									
												x			x	Mixsim	Sierra		
												x			x	Mixsim	Sierra		
EXAR	Linear Bipolar Master Chips-Series XR-100	x	x	x	x	GATE MASTER	Daisy			Tektronix			x	x	x	QUIKIE	Tek/ICO	45	
		x	x	x	x	PROPRIETARY	Exar				QuickChip		x	x	x				
											Thomson-Mostek	MOS	x	x		CT2000	CaseTech		
												x	x			CT2000	CaseTech		
Linear I <sup>2</sup> L Master Chips-Series XR-400		x	x	x	x	GATE MASTER	Daisy			United Silicon Structures		x	x	x	x	Solo 1200	United		
		x	x	x	x	PROPRIETARY	Exar				VLSI Technology Inc.	All CMOS	x	x	x	VTI Tools	VLSI Tech		
Linear CMOS Custom		x	x	x	x	CHIP MASTER	Daisy	10		VTC Incorporated								50	
		x	x	x	x	PROPRIETARY	Exar				VJ800 Analog Master Chip Family	x	x			PERSONAL ENGINEER	CompVision		
												x	x			IDEA STATION	Mentor		
Linear Bipolar Custom		x	x	x	x	CHIP MASTER	Daisy			ZyMOS									
		x	x	x	x	PROPRIETARY	Exar				Standard Cell Analog ZyCOMII Library	x	x			ZyPSIM/ZySPICE	ZyMOS		
											MOS	x	x			CT2000	CaseTech		
Gennum Corp.	LA200	x	x			Workview/SPICE	Gennum	15											
		x	x			CADD5-2	Gennum												
						Workview/SPICE	Gennum												
						CADD5-2	Gennum												
LA200, LA250		x	x	x	x	GDS II	Calma	20											
		x	x	x	x	Chip Master	Daisy												
		x	x	x	x	SCALD	Valid												
		x	x	x	x	CV	CompVision												
Linear Technology Inc	LA200, LA250	x	x	x	x	APLE860	Applicon												
LSI Logic	CMOS, MOS	x	x			CT2000	CaseTech												
		x	x			CT2000	CaseTech												
Micro Linear	FB300, FB3600	x	x			Linear CAD II	MicroLinear	25											
	FB900	x	x			Linear CAD II	MicroLinear												
	FB300, FB3600	x	x			Logician	Daisy												
		x	x			Personal													
		x	x	x		Logician	Daisy												
		x	x	x		ChipMaster	Daisy												
		x	x			Analog													
		x	x			Workbench	AnalDesTools												
		x	x			PC Workbench	AnalDesTools	30											
				x		Applicon	Applicon												
				x		GDS-II	Calma												
BIP, Analog Bipolar/Analog		x	x			CT2000	CaseTech												
		x	x			CT2000	CaseTech												
Micronos	MOS	x	x			CT2000	CaseTech	35											
		x	x			CT2000	CaseTech												
Polycore	Linear Maxichips	x	x	x	x	ANALOG WORKBENCH	AnalDesTools												
Semicustom Arrays	Modula—LA250 Series, LA200 Series	x	x	x	x	GDSII	Calma	40											
		x	x	x	x	CHIP MASTER	Daisy												
		x	x			SCALD	Valid												

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FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION

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## ASICs/CUSTOM

## ASICs/CUSTOM

## ASICs/CUSTOM

## ASIC/CUSTOM—Standard Cell Design Automation Tools

ASIC/CUSTOM									
Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Re-simulation	Design Tool	Source	Line	
Array Technology	3μ CMOS	x	x		x	CELL STATION	Mentor		
BICMOS Technology	BC2000 2μ 2 metal	x				SDS	Barvon		
			x			SILOS	Barvon		
				x		CAL-MP +	Barvon		
		x	x		x		Barvon	5	
		x	x	x	x		Barvon		
BC4000 Enhanced	2μ 2 metal	x				SDS	Barvon		
			x			SILOS	Barvon		
				x		CAL-MP +	Barvon	10	
		x	x		x		Barvon		
		x	x	x	x		Barvon		
BC6000 1.5μ 2 metal		x				SDS	Barvon		
			x			SILOS	Barvon		
				x		CAL-MP +	Barvon	15	
		x	x		x		Barvon		
		x	x	x	x		Barvon		
EXAR Corp.	A3000 Series	x				SDS	SilvarLisco		
			x			HILO	GenRad	20	
				x		CAL-MP	SilvarLisco		
					x	DRACULA	ECAD		
Fairchild	FSC10000	x	x	x	x	FAIRCAD	Fairchild		
		x	x			MEGA	Daisy	25	
		x	x			LOGICIAN	Daisy		
						GATE STATION	Mentor		
Fujitsu Microelectronics	VH Series CMOS	x	x			LOGICIAN	Daisy		
		x	x			SCALD	Valid		
		x	x	x	x	CELL STATION	Mentor	30	
All CMOS		x	x	x	x	LCAD	Fujitsu		
General Electric	ISC 20000 2μ, 2LM CMOS					CADEXEC	GE Semi		
		x	x	x	x	CELL MASTER	Daisy		
		x	x			PERSONAL	Daisy		
						LOGICIAN	Daisy		
		x	x	x	x	CELL STATION	Mentor	35	
		x	x			TEGASTATION	Calma		
			x			TEGAS	Calma		
		x				CAE-1,	PCAD		
		x				CAE-2	FutureNet		
Gould	3μ 1 metal, 3μ 2 metal, 2μ 2 metal	x	x	x	x	CIPAR	Gould		
								40	
		x	x		x	LOGICIAN	Daisy		
		x	x		x	MEGALOGICIAN	Daisy		
		x	x		x	CELL STATION	Mentor		
		x	x	x	x	IEDS/TANCELL	Intergraph		
(Continued)									
Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Re-simulation	Design Tool	Source	Line	
Gould Inc.	3μ 1 metal, 3μ 2 metal, 2μ 2 metal								(Cont'd)
		x	x		x	IDEA STATION	Mentor	45	
		x				PERSONAL LOGICIAN	Daisy		
Harris	HSC-CMOS	x	x	x	x	Harris/SDA	Harris		
	HSC, 2μ 1 metal	x	x		x	CELL MASTER	Daisy		
		x	x			SCALD	Valid		
		x	x			CELL STATION	Mentor		
	HSCD, 1.5μ 2 metal (Q2 1986)	x	x		x	CELL MASTER	Daisy	50	
		x	x			SCALD	Valid		
		x	x			CELL STATION	Mentor		
Hughes	3μ 1 Metal	x				LOGICIAN	Daisy	55	
		x				IDEA 1000	Mentor		
			x			DANA	Hughes		
				x		ALPS	Hughes		
IC Options, Inc.	ICO-Cell	x	x			Idea Station	Mentor		
		x				ICO-ECS (PC-AT)	IC Options		
			x			Salt (on PC-AT)	CAD Group		
				x	x	ICO-ATA (PC-AT)	IC Options	60	
International Microcircuits, Inc.	2μ, 2metal	x	x	x	x		IMI		
	2.5μ, 2metal	x	x	x	x		IMI		
	3.5μ, 1metal	x	x	x	x		IMI		
	5μ, 1metal	x	x	x	x		IMI		
LSI Logic	STANDARD CELL	x	x			SCALDSYSTEM		65	
		x	x			Valid	Tek/CAE		
		x				IDEAL	PCAD		
		x				CAE-1 (-2)	FutureNet		
		x	x	x	x	DASH	MDE	70	
		x	x			IDEASTATION	Mentor		
		x	x			LOGICIAN	Daisy		
		x	x			DASH	FutureNet		
Marconi	3μCellMOS	x		x	x	CASS/CAL-MP	SilvarLisco	75	
		x	x			Hilo	GenRad		
		x	x			Ideastation	Mentor		
	5μCellMOS	x		x	x	CASS/CAL-MP	SilvarLisco		
		x	x			Hilo	GenRad		
		x	x			Ideastation	Mentor		
	3μCellSOS	x		x	x	CASS/CAL-MP	SilvarLisco	80	
		x	x			Hilo	GenRad		
		x	x			Ideastation	Mentor		
	5μCellSOS	x		x	x	CASS/CAL-MP	SilvarLisco		
		x	x			Hilo	GenRad		
		x	x			Ideastation	Mentor		
	3μCellSOS	x	x			Logician	Daisy	85	
		x	x			Logician	Daisy		

FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION  
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## ASICs/CUSTOM

## ASICs/CUSTOM

## ASICs/CUSTOM

## ASICs/CUSTOM

## ASIC/CUSTOM—Standard Cell Design Automation Tools (Cont'd)

Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Re-simulation	Design Tool	Source	Line	Array Source	Device Family	Schematic Entry	Simulation & Timing	Place & Route	Layout Extraction & Re-simulation	Design Tool	Source	Line
Standard Microsystems Customization				x		(Cont'd)			Waferscale Integratiion Modular Cell Library				x		(Cont'd)		
		x	x		x	Tancell	Tangent							x	Tancell	Tangent	
		x	x		x	Tansure	Tangent							x	Dracula	ECAD	
		x	x		x	Workview	ViewLogic										
						Logician/Megalogician	Daisy										
		x	x		x	Ideastationn	Mentor	5		Waferscale Integration Modular-Cell Library	x	x			CAE-1	PCAD	
		x	x		x	SCALD System	Valid				x	x	x	x	CASS/CAL-MP	SilvarLisco	45
				x		CAL-MP	SilvarLisco								CELL		
						Cadat	HHB-Sys				x	x			STATION	Mentor	
					x	GDS-II	Calma								SCALD		
															STATION/REDL	Valid	
															CHIP		
CMOS Si-Gate	x	x			x	Workview	ViewLogic	10		Waferscale Integration, Inc. Modular-Cell Library	x	x			LOGICIAN	Daisy	
		x			x	Logician/Megalogician	Daisy				x	x			MEGALOGICIAN	Daisy	
	x	x			x	Ideastation	Mentor										
	x	x			x	SCALDsystem	Valid										
	x	C	A			L-MP	SilvarLisco										
	x	x			x	CADAT	HHB-Sys	15		Zymos							
						GDS II	Calma			ZyCOM II 5μ 2 metal, ZyDP II 3μ 2 metal, ZyDP-3 2μ 2 metal	x	x			LOGICIAN	Daisy	50
Texas Instruments 2μ, 2 Metal 3μ, 1 Metal	x	x			x	Megalogician	Daisy										
	x	x			x	Logician	Daisy										
	x					Dash-1	FutureNet										
	x	x			x	Ideastation	Mentor	20									
	x	x			x	CAE-2	PCAD										
	x	x			x	DCS											
						Hilo-Genrad	HP										
Thomson-Mostek SA Series, 3μ 2 metal, SB Series, 2μ 2 metal	x	x	x		x	HIGHLAND 2	Thomson										
	x	x				GATE											
	x	x				STATION	Mentor										
	x	x				LOGICIAN	Daisy	25									
	x	x				CT1000/SILOS	CaseTech										
	x	x				GATE											
	x	x				DESIGNER	Valid										
	x	x				TEGASTATION	Calma										
Unicorn Microelectronics COMPILE	x	x	x		x	COMPILE	Unicorn										
	x	x	x		x	COMPILE	Unicorn	30									
Vatic Systems HC1P-H, HC1P-A, HC2	x	x	x		x	CAL-MP	SilvarLisco										
VLSI Design Associates VD3000	x	x				CELL											
	x	x				STATION	Mentor										
						LOGICIAN	Daisy										
ZY	x	x	x		x	ZYP	ZyMOS										
VLSI Technology Inc. CMOS 2μM	x	x	x		x	VTI Tools	VLSI Tech	35									
VTC Incorporated VL1000 Bipolar Linear/Digital Cell Library	x	x				PERSONAL	CompVision										
	x	x				ENGINEER	Mentor										
VL2000 Digital Cell Library	x	x				PERSONAL	CompVision										
	x	x				ENGINEER	Mentor										
	x	x				IDEA STATION											
Waferscale Integratiion Modular Cell Library	x					Logician	Daisy	40									
	x					Mentor	Mentor										

FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION

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ASIC/CUSTOM—VLSI/LSI Macrocell Libraries

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
AMCC	Q1500, Q3500	x		Up Counter—4-Bit cascadable				AMCC	5
		x		Up Counter—8 bit ripple				AMCC	
		x		Adder—8-bit carry lookahead				AMCC	
		x		Register-octal D flip/flop w/reset				AMCC	
		x		Register-octal D latch w/reset				AMCC	
		x		Shift register—8-bit				AMCC	
		x		Clock driver				AMCC	
		x		Clock pulse generator				AMCC	
		x		ALU—4-bit				AMCC	
		x		MUX—8:1 w/enable				AMCC	
	QM1600S	x		RAM—1280 bits, programmable w/(2) 640-bit blocks			Macro Matrix	AMCC	10
Array Technology	3 $\mu$ CMOS		x	Core microprocessor	65C02		3 $\mu$ CMOS	NCR	15
			x	ROM		Configurable size		NCR	
			x	RAM		Configurable size		NCR	
		x	x	Counter/Timer		16 bit latched disk/tape interface	DHS/HCD	NCR	
			x	Data Separator			DHS/HCD	ArrayTech	
Calmos Systems Inc.	CA8XXXX		x	Octal I/O Port	CA8212		3–2 $\mu$ m CMOS	Calmos	
Fairchild	Supermacros	x	x	32x32 Cross point switch	—		Supermacros	Fairchild	20
		x	x	Bit slice	2901			Fairchild	
			x	Parallel I/O	82C55A			Fairchild	
			x	Multifunction UART	82C56A			Fairchild	
			x	Priority Interrupt Controller	82C59A			Fairchild	25
			x	Octal latch	82C82			Fairchild	
			x	Octal latch (inv)	82C83			Fairchild	
		x	x	Clock generator	82C84A			Fairchild	
			x	Octal bus transceiver	82C86			Fairchild	30
			x	Octal bus transceiver (inv)	82C87			Fairchild	
			x	Bus arbiter	82C89			Fairchild	
			x	Baud rate generator	4702			Fairchild	
		x	x	Manchester encoder/decoder	6409			Fairchild	30
			x	Reconfigurable static RAM 1K	—			Fairchild	
			x	CRT Controller	—			Fairchild	
Fujitsu Microelectronics	B240-B2000 Bipolar	x		ALU/Function generator	74LS181		Bipolar	Fujitsu	35
		x		ALU/Function generator	74LS381		Bipolar	Fujitsu	
		x		ALU/Function generator	74LS382		Bipolar	Fujitsu	
	CMOS	x		RAM-(1k to 12K) (x4 to x64)		Multiport or split memories	AVM, UM	Fujitsu	40
	Supermacros	x	x	USART			AV, UH	Fujitsu	
General Electric	ISC20000		x	Core Microprocessor	29C01	Cascadable from 8 bits to 8, 12 or 16 bits	ISC20000	GE Semi	40
			x	Microprogram Sequencer	29C10, 29C10A	Cascadable from 4 bits to 8, 12 or 16 bits		GE Semi	
			x	Configurable static RAM, 4K				GE Semi	
			x	Configurable static ROM, 128K				GE Semi	
			x	4-Bit Magnitude Comparator	F7485			GE Semi	45
			x	1-of-8 Decoder	F74138			GE Semi	
			x	Dual 4-to-1 Multiplexer	F74153			GE Semi	
			x	4-Bit Modulo 10 Counter	F74160			GE Semi	
			x	4-Bit Modulo 16 Counter	F74161			GE Semi	50
			x	4-Bit Modulo 10 Counter	F74162			GE Semi	
			x	4-Bit Modulo 16 Counter	F74163			GE Semi	
			x	8-Bit Shift Register	F74165			GE Semi	
			x	4-Bit Modulo 10 Up/Down Counter	F74168			GE Semi	55
			x	4-Bit Modulo 16 Up/Down Counter	F74169			GE Semi	
			x	4-Bit ALU	F74181			GE Semi	
			x	4-Bit Modulo 10 Up/Down Counter	F74190			GE Semi	
			x	4-Bit Modulo 16 Up/Down Counter	F74191			GE Semi	55
			x	4-Bit Modulo 16 Up/Down Counter	F74193			GE Semi	
			x	Quad Bidirectional Buffer	F74243			GE Semi	
			x	8-Bit Tristate Buffer	F74244			GE Semi	

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
General Electric	ISC20000							(Cont'd)	
		x	8-Bit D Flip-Flop	F74273		GE Semi			
		x	4-Bit Full Adder	F74283		GE Semi			
		x	8-Bit Tristate D Latch	F74373		GE Semi			
		x	8-Bit Tristate D Flip-Flop	F74374		GE Semi			
		x	1-Bit Full Adder/Subtractor	FAS1		GE Semi		5	
		x	D Flip-Flop With Scan	FDFRBT		GE Semi			
		x	2-to-4-Line Decoder	F74139		GE Semi			
		x	8-Line to 3-Line Priority Encoder	F74148		GE Semi			
		x	1 of 8 data selector	F74151		GE Semi			
		x	Quadruple 2-Line to 1-Line Mux	F74157		GE Semi		10	
		x	8 Bit Parallel Out Serial Shift Register	F74164		GE Semi			
		x	8 Bit Odd/Even Parity Generator/Checker	F74180		GE Semi			
		x	Look Ahead Carry Generator	F74182		GE Semi			
		x	Synch. 4 Bit Up/Down Cntr	F74192		GE Semi			
		x	4 Bit Bidirectional Universal Shift Reg	F74194		GE Semi		15	
		x	4 Bit Parallel Access Shift Register	F74195		GE Semi			
		x	Octal Buffer w/Line Driver	F74240		GE Semi			
		x	Octal Buffer w/Line Driver	F74241		GE Semi			
		x	Quad Bus Transceiver	F74242		GE Semi			
		x	Octal Bus Transceiver	F74245		GE Semi		20	
		x	Data Selector	F74251		GE Semi			
		x	Dual 4 to 1 Line Data Selector/Mux Tristate	F74253		GE Semi			
		x	9 Bit Parity Generator w/Checker	F74280		GE Semi			
		x	8-Input NAND Gate	F7430		GE Semi			
		x	4 to 10 Decoder/BCD to Decimal	F7442		GE Semi		25	
		x	8-Bit Equality Comparator	F74688		GE Semi			
		x	Decade Counter	F7490		GE Semi			
		x	Divide by Twelve Counter	F7492		GE Semi			
		x	4-Bit Binary Ripple Counter	F7493		GE Semi			
		x	4-Bit Parallel Access Shift Register	F7495		GE Semi		30	
		x	1-Bit BILBO	FBILBO1		GE Semi			
		x	8-Bit BILBO	FBILBO8		GE Semi			
		x	4-Bit Equality Comparator	FECMP4		GE Semi			
		x	4-Bit Incrementer	FINC4		GE Semi			
		x	6-Input NAND gate	FND6		GE Semi		35	
		x	6-Input NOR gate	FNR6		GE Semi			
		x	8-Input NOR gate	FNR8		GE Semi			
		x	4-Bit Rotater	FROT4		GE Semi			
		Gould	Soft Cells		x	Dual 2-Line to 4-Line Decoder	74139		
CCD		x	256x4 ROM				CCD	Gould	40
		x	256x16 ROM				Gould		
		x	256x32 ROM				Gould		
		x	512x8 ROM				Gould		
		x	512x16 ROM				Gould		45
		x	512x32 ROM				Gould		
Soft Cells		x	32x8 SRAM				Gould		
		x	Dual 2-Line to 4-Line or 3-Line to 8-Line Decoder	74155		Gould			
		x	4-Bit D-Type Register, Three-State	74173		Gould			
		x	Hex D-Type Flip-Flop with Clear	74174		Gould		50	
		x	Quad D-Type Flip-Flop with Clear	74175		Gould			
		x	Octal D-Type Flip-Flop with Clear	74273		Gould			
		x	Octal D-Type Flip-Flop, Three-State	74374		Gould			
		x	Octal Latch, Three-State	74373		Gould			
		x	4-Bit Bistable Latch	74375		Gould		55	
		x	Dual 4-Line to 1-Line Data Selector/Multiplexer	74153		Gould			
x	Quad 2-Line to 1-Line Data Selector/Multiplexer	74157		Gould					
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## ASICs/CUSTOM

## ASICs/CUSTOM

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
Gould	HCMOS		x	16-Bit Barrel Shifter	BR16			Gould	(Cont'd)
				32-Bit Barrel Shifter	BR32			Gould	
				8-Bit Pipeline Register	PR08			Gould	
				16-Bit Pipeline Register	PR16			Gould	
				24-Bit Pipeline Register	PR24			Gould	
				Dual-Port RAM Controller	SP03			Gould	
				Serial Port	SE01			Gould	
				4-Bit Adder/Subtractor	AU04			Gould	
				8-Bit A/D Converter	LA08			Gould	
				8-Bit D/A Converter	LD08			Gould	
				6-Bit Logarithmic	LM06			Gould	
				Multiplying D/A Converter				Gould	
				Bandgap Reference	LB04			Gould	
				Low Pass Filter	LF10			Gould	
				High Pass Filter	LF11			Gould	
				Band Pass Filter	LF12			Gould	
	Soft Cells							Soft Cells	Gould
	CCD		x	256x8 ROM				Gould	
				512x4 ROM				Gould	
	Soft Cells		x	8-Bit Bistable Latch	74100			Gould	20
				16-Line to 1-Line Data Selector/Multiplexer	74150			Gould	
				8-Line to 1-Line Data Selector/Multiplexer	74151			Gould	
				8-Line to 1-Line Data Selector/Multiplexer	74152			Gould	
				16-Line to 1-Line Multiplexer, Three-State	74250			Gould	
				8-Line to 1-Line Multiplexer, Three-State	74251			Gould	
				8-Bit Parallel Output Shift Register	74164			Gould	
				8-Bit Parallel Load Shift Register	74165			Gould	
				8-Bit Parallel Load Shift Register	74166			Gould	
				8-Bit Shift Register with Three-State Parallel Output Register	74595			Gould	
				8-Line to 3-Line Priority Encoder	74148			Gould	
				9-Bit Parity Generator	74280			Gould	
				8-Bit Magnitude Comparator	74686			Gould	
				8-Bit Identity Comparator	74688			Gould	
Harris Semiconductor	HSC-CMOS		x	DMA Controller	82C37A			HSC250	Harris Harris
				Asynchronous Communication Element	82C50A				
				Asynchronous Communication Element	82C50B				
				UART/BRG	82C52				
				Programmable Interval Timer	82C54				
				Parallel I/O	82C55A				
				Priority Interrupt Controller	82C59A				
				Clock Generator	82C84A				
				Bus Controller	82C88				
				Baud Rate Generator	HD4702				
				UART	HD6402				
				UART/BRG/Modem Control	HD6406				
				ASMA	HD6408				
				Manchester Encoder/Decoder	HD6409				
				Manchester Encoder/Decoder	HD15530				
				Programmable Manchester Encoder/Decoder	HD15531				
				Reconfigurable Static RAM	1K RAM				
				Reconfigurable ROM	1K ROM				
ILSI	CB-3XXX, CA-2XXX	x		RAM		Configurable	STD. CELL	iLSi iLSi	

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ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
ILSI	CB-3XXX, CA-2XXX	x		ROM		Words 16, 32, 64, 128, 256 Bits x1, x4, x8, x9, x16, x18			(Cont'd)
		x		PLA		True PLA implementation Configurable	iLSi		
International Microcircuits, Inc.	IMI6000	x	x	BCD-to-Decimal Decoder	SN74HC42		IMI6000	IMI	5
		x	x	4-Bit Magnitude Comparator	SN74HC85			IMI	
		x	x	3-Line to 8-Line Decoder/Demultiplexers	SN74HCT138			IMI	
		x	x	2-Line to 4-Line Decoder/Demultiplexers	SN74HC139			IMI	
		x	x	4-Line to 1-Line Data Selectors/Multiplexers	SN74HC153			IMI	
		x	x	Quadruple 2-Line to 1-Line Data Selectors/Multiplexers	SN74HC157			IMI	10
		x	x	Octal 2-Line to 1-Line Data Selectors/Multiplexers	SN74HC604			IMI	
		x	x	Synchronous 4-Bit Binary Counters	SN74HC161			IMI	
		x	x	Synchronous 2-Bit Binary Counters	—			IMI	
		x	x	Fully Synchronous 4-Bit Binary Counters	—			IMI	
		x	x	8-Bit Parallel-Out Serial Shift Register	SN74HC164			IMI	15
		x	x	8-Bit Shift Register	SN74HC166			IMI	
		x	x	4-Bit Shift Register	—			IMI	
		x	x	Quadruple D Flip-Flops	SN74HC175			IMI	
		x	x	Octal D Flip-Flops	—			IMI	
		x	x	Presetable 4-Bit Binary Counters/Latches	SN74HC177			IMI	20
		x	x	Presetable 2-Bit Binary Counters/Latches	—			IMI	
		x	x	Carry Save Full Adder	SN74HC183			IMI	
		x	x	Synchronous 4-Bit Up/Down Counters	SN74HC4024			IMI	
		x	x	Synchronous 2-Bit Up/Down Counters	—			IMI	
		x	x	Synchronous 4-Bit Dual Clock Binary Up/Down Counters	—			IMI	25
		x	x	Synchronous 2-Bit Dual Clock Binary Up/Down Counters	—			IMI	
		x	x	Octal D-Type Transparent Latch	SN74HCT373			IMI	
		x	x	Decade Counters	SN74HC390			IMI	
		x	x	4-Bit Binary Counters	SN74HC393			IMI	
		x	x	8-Bit Magnitude Comparator	SN74HC688			IMI	30
		x	x	PLL Synthesizer	MC145152			IMI	
		x	x	PLL Synthesizer	MC145155			IMI	
		x	x	PLL Synthesizer	MC145156			IMI	
		x	x	PLL Synthesizer	MC145157			IMI	
		x	x	PLL Synthesizer	MC145158			IMI	35
		x	x	Multiplier, 8x8	ADSP1080			IMI	
		x	x	Multiplier, 12x12	ADSP1012			IMI	
		x	x	Multiplier, 16x16	ADSP1016			IMI	
		x	x	Microprocessor, Integrated with 4x2901, 2902, and 2910.				IMI	
LSI Logic	LLXXXX	x	x	Bit Slice ALU	2901		LLXXXX	LSI Logic	40
		x	x	Carry Look Ahead	2902			LSI Logic	
		x	x	Bit Slice ALU	2903			LSI Logic	
		x	x	Bit Slice ALU	29203			LSI Logic	
		x	x	Status & Shift Control Unit	2904			LSI Logic	
		x	x	Microprogram Sequencer	2909			LSI Logic	45
		x	x	Microprogram Controller	2910			LSI Logic	
		x	x	Microprogram Sequencer	2911			LSI Logic	
		x	x	Priority Interrupt Expander	2913			LSI Logic	

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gates Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
LSI Logic	LLXXXX							(Cont'd)	
		x	x	Vectored Priority Interrupt Controller	2914		LSI Logic		
		x	x	Program Control Unit	2930		LSI Logic		
		x	x	Program Control Unit	2932		LSI Logic		
		x	x	DMA Address Generator	2940		LSI Logic		
		x	x	Prog. Timer/Counter DMA Address Generator	2942		LSI Logic		5
		x	x	16-Bit EDC Unit	2960		LSI Logic		
		x	x	DMA Controller	8237		LSI Logic		
		x	x	UART	8251		LSI Logic		
		x	x	Programmable Interval Timer	8253		LSI Logic		
		x	x	Programmable Interval Timer	8254		LSI Logic		10
		x	x	Programmable Peripheral Interface	8255		LSI Logic		
		x	x	Programmable DMA Controller	8257		LSI Logic		
		x	x	Programmable Interrupt Controller	8295		LSI Logic		
		x	x	Clock Generator	8284		LSI Logic		
		x	x	Bus Controller	8288		LSI Logic		15
		x	x	Clock Generator	82284		LSI Logic		
		x	x	Bus Controller	82288		LSI Logic		
		x	x	UART	6850		LSI Logic		
		x	x	CRT Controller	6845		LSI Logic		
		x	x	8x8 Multiplier			LSI Logic		20
		x	x	12x12 Multiplier			LSI Logic		
		x	x	16x16 Multiplier			LSI Logic		
		x	x	16-Bit Barrel Shifter			LSI Logic		
		x	x	32-Bit Barrel Shifter			LSI Logic		
		x	x	Content Addressable Memory			LSI Logic		25
		x	x	Floating Point Arithmetic Blocks			LSI Logic		
		x	x	12-Bit Microprogram Controller	2910A		LSI Logic		
		x	x	16-Bit Microprogram Controller	2916-16		LSI Logic		
		x	x	32-Bit EDC Unit	2960-32		LSI Logic		
		x	x	64-Bit EDC Unit	2960-64		LSI Logic		30
		x	x	Dynamic Memory Controller	2964		LSI Logic		
		x	x	8-Bit Slice Microprogram Sequencer	29112		LSI Logic		
		x	x	Multiport Pipeline Processor	29501		LSI Logic		
		x	x	Multilevel Pipeline Registers	29520		LSI Logic		
		x	x	Programmable Interrupt Controller	8259A		LSI Logic		35
		x	x	16 or 32-Bit Carry Select Adder			LSI Logic		
		x	x	16 or 32-Bit 3-Port Adder			LSI Logic		
		x	x	16 or 32-Bit 74181 Type ALU			LSI Logic		
		x	x	16 or 32-Bit Magnitude Comparator			LSI Logic		
		x	x	16x4 FIFO			LSI Logic		40
		x	x	16x4 Content Addressable Memory			LSI Logic		
		x	x	32x4 Content Addressable Memory			LSI Logic		
Matra Design Systems		x		ALU (16 Arith., 16 Logic)		21 gates/bit	SAJ I V	Matra	
		x		STATIC SHIFT REGISTER		6 gates/stage		Matra	45
		x		Asynchronous Counter		6 gates/stage		Matra	
		x		Synchronous Counter		11 gates/stage		Matra	
		x		Up/Down Counter		12 gates/stage		Matra	
		x		UART		360 to 644 gates		Matra	
		x		Presetable Counter		14 gates/stage		Matra	50
		x		Divide by N Counter		12 gates/stage		Matra	
		x		N by M Multiplier		11 gates/basic unit		Matra	
		x		Dynamic PLA		1 gate/PLA output		Matra	
		x		STATIC RAM		up to 2K bits		Matra	
		x		ROM		up to 4K bits		Matra	55
Micro Linear	FB300, FB3600						FB300	MicroLinear	
		x		2.5 V Bandgap Voltage Reference				MicroLinear	
		x		5 V Bandgap Voltage Reference				MicroLinear	60
		x		50 MHz VCO				MicroLinear	
		x		PNP Input-Ground Sensing Op Amp	LM324			MicroLinear	
								MicroLinear	

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ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
Micro Linear	FB300, FB3600							(Cont'd)	
		x		NPN Input Op Amp	μA741			MicroLinear	
		x		Transconductance (GM) Op Amp	LM13600			MicroLinear	
		x		External Compensation Op Amp				MicroLinear	5
		x		High Slew-Rate Op Amp				MicroLinear	
		x		Wideband Unity Gain Buffer				MicroLinear	
		x		Ground Sensing Comparator	LM339			MicroLinear	10
		x		High-Speed Latching Comparator	LM360			MicroLinear	
		x		Wideband Video Amplifier	NE592			MicroLinear	
		x		Low Power Video Amplifier				MicroLinear	15
		x		Double Balanced Modulator/Demodulator	MC1496			MicroLinear	
		x		AGC Amplifier	MC1350			MicroLinear	
		x		Timer	NE555			MicroLinear	20
		x		Sample and Hold Buffer				MicroLinear	
		x		6-Bit D/A Converter Core with Switches				MicroLinear	
		x		2-Input Exclusive-OR				MicroLinear	
		x		D-Type Flip-Flop with SET/RESET				MicroLinear	25
Micro Power Systems	Special Function	x		Instrument Amp	INA101			Analog	
		x		Voltage to Freq. Converter	VFC32			MicroPwr	
		x		Dig. Multiplier/Accumulator	1010			MicroPwr	30
		x		Dynameter	5007			MicroPwr	
		x		Dynameter	7104			MicroPwr	
		x		CB PLL Syn.	5041			MicroPwr	
		x		CB PLL Syn.	7189			MicroPwr	
		x		Low Pwr Narrow Band FM IF	5071			MicroPwr	35
		x		Switching Regulator	5078			MicroPwr	
		x		D/A Support Function	5528/5529			MicroPwr	
	OP AMPS	x		OP AMP	OP01			MicroPwr	
		x		OP AMP	OP02			MicroPwr	
		x		OP AMP	OP03			MicroPwr	40
		x		OP AMP	OP04			MicroPwr	
		x		OP AMP	OP05			MicroPwr	
		x		OP AMP	OP06			MicroPwr	
		x		OP AMP	OP07			MicroPwr	
		x		OP AMP	OP08			MicroPwr	45
		x		OP AMP, Quad Matched	OP09			MicroPwr	
		x		OP AMP, Dual	OP10			MicroPwr	
		x		OP AMP, Quad Matched	OP11			MicroPwr	
		x		OP AMP	OP12			MicroPwr	
		x		OP AMP, Dual Matched	OP14			MicroPwr	50
		x		OP AMP	OP27			MicroPwr	
		x		OP AMP	OP37			MicroPwr	
		x		OP AMP	108A/208A/308A			MicroPwr	
		x		OP AMP	155A/156A/157A			MicroPwr	
		x		OP AMP, Dual	OP207			MicroPwr	55
		x		OP AMP, Dual	OP227			MicroPwr	
		x		OP AMP	OP2108A/2208A			MicroPwr	
		x		OP AMP, Quad	4136			MicroPwr	
Voltage References		x		Voltage Ref.	REF01			MicroPwr	
		x		Voltage Ref.	REF02			MicroPwr	
		x		Voltage Ref.	REF05			MicroPwr	60
		x		Voltage Ref.	REF10			MicroPwr	
		x		Voltage Ref.	5010			MicroPwr	

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
(Cont'd)									
Micro Power Systems	Analog Switches		x	SPST, Dual	200DI			MicroPwr	5
			x	SPST, Quad	201DI			MicroPwr	
			x	DPST, Dual	302DI			MicroPwr	
			x	SPDT, Dual	302DI			MicroPwr	
			x	SPST, Quad	7610DI			MicroPwr	
			x	SPST, Quad	7511DI			MicroPwr	
			x	SPDT, Dual	7512DI			MicroPwr	
	Multiplexers		x	4 Ch Diff Mux	7502			MicroPwr	10
			x	4 Ch Diff Mux	7509DI			MicroPwr	
			x	8 Ch Mux	7501			MicroPwr	
			x	8 Ch Mux	7503			MicroPwr	
			x	8 Ch Diff Mux	7507			MicroPwr	
			x	8 Ch Mux	7508DI			MicroPwr	
			x	16 Ch Mux	7506			MicroPwr	
	D/A		x	16 Bit DAC	7616			MicroPwr	15
			x	16 Bit DAC, Dual Buffered	7636			MicroPwr	
			x	16 Bit DAC	9331			MicroPwr	
			x	16 Bit DAC	9377-16			MicroPwr	
			x	18 Bit DAC	370			MicroPwr	
			x	18 Bit DAC	377-18			MicroPwr	
	A/D		x	3 1/2 DPM A/D	7138			MicroPwr	25
			x	6 Bit A/D CMOS Flash	7682			MicroPwr	
			x	8 Bit A/D	7574			MicroPwr	
			x	8 Bit A/D, 8 Chn	7581			MicroPwr	
			x	8 Bit A/D, CMOS Flash	7683			MicroPwr	
			x	8 Bit A/D, CMOS Flash	7684			MicroPwr	
			x	10 Bit A/D	7570			MicroPwr	
			x	12 Bit A/D, w/uP	574			MicroPwr	
			x	13 Bit A/D	7550			MicroPwr	
	D/A		x	6 Bit DAC	5520			MicroPwr	30
			x	8 Bit DAC	7523			MicroPwr	
			x	8 Bit DAC	7524			MicroPwr	
			x	8 Bit DAC, Dual Buffered	7528			MicroPwr	
			x	8 Bit DAC, Quad Buffered	7628			MicroPwr	
			x	10 Bit DAC	7520			MicroPwr	
			x	10 Bit DAC, Buffered	7522			MicroPwr	
			x	10 Bit DAC	7530			MicroPwr	
			x	10 Bit DAC	7533			MicroPwr	
			x	10 Bit DAC	7633			MicroPwr	
			x	12 Bit DAC, Dual Buffered	1208			MicroPwr	
			x	12 Bit DAC, Dual Buffered	1230			MicroPwr	
			x	12 Bit DAC	562			MicroPwr	
			x	12 Bit DAC	7521			MicroPwr	
			x	12 Bit DAC	7531			MicroPwr	
			x	12 Bit DAC	7541			MicroPwr	
			x	12 Bit DAC, Dual Buffered	7542			MicroPwr	
			x	12 Bit DAC, Serial Input	7543			MicroPwr	
			x	12 Bit DAC	7621			MicroPwr	
			x	12 Bit DAC, Dual Buffered	7622			MicroPwr	
			x	12 Bit DAC	7623			MicroPwr	
			x	12 Bit DAC, Buffered	7645			MicroPwr	50
			x	13 Bit DAC, Complete	8526			MicroPwr	
			x	14 Bit DAC	3140			MicroPwr	
			x	14 Bit DAC	7614			MicroPwr	
Motorola	Supercell 3 $\mu$ -1 Metal		x	Core microprocessor	6502	8-bit with added instructions and expanded op codes	Supercell	Motorola	55
			x	Modular ROM	6502	Can be organized in 512 x n-bit blocks		Motorola	
			x	Modular RAM	6502	Can be organized in 16 x n-bit blocks		Motorola	
			x	Timer	6502	16-bit counter, compatible with 65CX02		Motorola	
	Supercell 2 $\mu$ -2 Metal		x	Modular ROM	6502	Can be organized in 512 x n-bit blocks		Motorola	60
			x	Modular RAM	6502	Can be organized in 16 x n-bit blocks		Motorola	

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
Motorola	Supercell 3 $\mu$ -1 Metal		x	Linear D/A	6502	8-bit linearity switch capacitor architecture		Motorola	(Cont'd)
			x	Linear A/D	6502	8-bit linearity, 30 microsecond conversion, successive approximation architecture		Motorola	
National Semiconductor	SCX-WS, SCX2-WS	x	x	Octal latch	82C82		SCX-WS, SCX2-WS	National	5
		x	x	Octal latch (inv)	82C83			National	
		x	x	Clock generator	82C84A			National	
		x	x	Octal bus transceiver	82C86			National	
		x	x	Octal bus transceiver (inv)	82C87			National	
		x	x	Bus controller	82C88			National	10
		x	x	Configurable static RAM 1K				National	
		x	x	Configurable ROM 1K				National	
		x	x	RAM up to 2K				National	
		x	x	ROM up to 32K				National	
		x	x	Linear components				National	
		x	x	Microprocessor cores				National	15
		x	x	UART/controllers				National	
NCR Microelectronics	CMOS II, 3 $\mu$ Supercells		x	Core $\mu$ P	6502	8-bit, 14 added instructions, expander op codes, 2 new address modes	Supercells	NCR	
			x	Modular ROM		Can be organized into 512 x n-bit blocks		NCR	
			x	Modular RAM		Can be organized into 16 x n-bit blocks		NCR	20
			x	Timer		16-bit counter timing compatible with 65CX02, 1 shot or continuous operation.		NCR	
	CMOS III, 2 $\mu$ Supercells		x	Modular ROM		Can be organized into 512 x n-bit blocks		NCR	
			x	Modular RAM		Can be organized into 16 x n-bit blocks		NCR	
	CMOS II, 3 $\mu$ Supercells		x	8-bit D/A		8-bit linearity, switch capacitor architecture		NCR	
			x	8-bit A/D		8-bit linearity, 8 $\mu$ s conversion, successive approximation architecture		NCR	25
RCA	3 $\mu$ DLM PaCMOS		x	1K bit ROM		Configurable Word Size	PaCMOS	GE/RCA	
			x	2K bit RAM		Configurable Word Size	PaCMOS	GE/RCA	
Silicon Systems Inc.	SmartCell		x	8-Bit Magnatude Comparator		5-V/12-V CMOS	CC/CD	SiliconSys	
Sierra Semiconductor	SC70000		x	8-bit Flash DAC		Current Output	2 $\mu$ CMOS	Sierra	30
			x	1-bit EEPROM, Flip-Flop				Sierra	
			x	1-bit EEPROM, Latch				Sierra	
			x	4-bit EEPROM, D-Register				Sierra	
			x	4-bit EEPROM, D-Register				Sierra	
			x	4-bit EEPROM, L-Register				Sierra	
			x	4-bit EEPROM Counter				Sierra	35
			x	64 to 1024 EEPROM Array				Sierra	
			x	32x8 EEPROM Memory				Sierra	
			x	64x8 EEPROM Memory				Sierra	
			x	28x8 EEPROM Memory				Sierra	
			x	256x8 EEPROM Memory				Sierra	40
			x	512x8 EEPROM Memory				Sierra	
			x	1024x8 EEPROM Memory				Sierra	
			x	High Voltage Interface				Sierra	
			x	High Voltage Supply				Sierra	
			x	Compiler RAM				Sierra	45
			x	Compiler ROM				Sierra	
			x	Compiler PLA				Sierra	
			x	Compiler 2901		Bit Slice Processor		Sierra	
			x	Compiler State Machine				Sierra	
			x	Compiler Data Path				Sierra	50
			x	Compiler Multiplier		NxN		Sierra	
			x	COP800 Microcontroller		Add up to 8K Byte ROM, 192-byte RAM		Sierra	
			x	LCD Controller		32-Segment Triplex		Sierra	
			x	12-bit ADC		Dual Slope		Sierra	
			x	8-bit Input Port				Sierra	55
			x	8-bit Output Port				Sierra	

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
Sierra Semiconductor	SC70000				NSC 58174			(Cont'd)	
			x	8-bit Input/Output Port				Sierra	
			x	Real Time Clock				Sierra	
			x	Key-Board Encoder				Sierra	
			x	Watchdog Timer				Sierra	
			x	External ROM Interface				Sierra	5
			x	UART		8250 Subset		Sierra	
			x	4-bit Flash ADC				Sierra	
			x	8-bit ADC		Successive Approximation		Sierra	
			x	10-bit ADC		Successive Approximation		Sierra	
			x	12-bit ADC		Dual Slope		Sierra	10
			x	8-bit ADC		High Speed		Sierra	
			x	4-bit Flash DAC		Current Output		Sierra	
			x	8-bit DAC		Voltage Output		Sierra	
			x	10-bit DAC		Charge Integration		Sierra	
			x	8-bit Flash DAC		Current Output		Sierra	15
			x	Internal Op-Amp		Gain $\pm 89$ dB, Bandwidth $\pm 2.8$ MHz		Sierra	
			x	Internal Op-Amp		Gain $\pm 90$ dB, BW $\pm 3.5$ MHz		Sierra	
			x	Internal Op-Amp		Gain $\pm 90$ dB, BW $\pm 2.9$ MHz		Sierra	
			x	External Op-Amp		Gain $\pm 89$ dB, BW $\pm 2.8$ MHz		Sierra	
			x	External Op-Amp		Gain $\pm 90$ dB, BW $\pm 3.5$ MHz		Sierra	20
			x	External Op-Amp		Gain $\pm 90$ dB, BW $\pm 2.9$ MHz		Sierra	
			x	Internal Op-Amp		Gain $\pm 66$ dB, BW $\pm 2.5$ MHz		Sierra	
			x	Internal Op-Amp		Gain $\pm 69$ dB, BW $\pm 3.0$ MHz		Sierra	
			x	External Op-Amp		Gain $\pm 66$ dB, BW $\pm 2.5$ MHz		Sierra	
			x	External Op-Amp		Gain $\pm 69$ dB, BW $\pm 3.0$ MHz		Sierra	25
			x	2:1 Analog MUX				Sierra	
			x	2:1 Analog MUX				Sierra	
			x	2:1 Analog MUX				Sierra	
			x	4:1 Analog MUX				Sierra	
			x	4:1 Analog MUX				Sierra	30
			x	4:1 Analog MUX				Sierra	
			x	Analog Switch				Sierra	
			x	Analog Switch				Sierra	
			x	Analog Switch				Sierra	
			x	Power-On-Reset		Threshold Reference		Sierra	35
			x	Power-On-Reset		Band Gap Reference		Sierra	
			x	RC Oscillator		500 kHz MAX		Sierra	
			x	RC Oscillator		50 kHz MAX		Sierra	
			x	Oscillator		Voltage Controlled, 30 MHz		Sierra	
			x	Crystal Oscillator		32 to 100 MHz		Sierra	40
			x	Crystal Oscillator		2 to 6 MHz		Sierra	
			x	Crystal Oscillator		6 to 12 MHz		Sierra	
			x	Voltage Comparator		80 ns Response Time		Sierra	
			x	Voltage Comparator		350 ns Response Time		Sierra	
			x	Voltage Comparator		15 ns Response Time		Sierra	45
			x	Voltage Comparator		500 ns Response Time		Sierra	
			x	Voltage Comparator		5 $\mu$ s Response Time		Sierra	
			x	Differential Receiver		Type 422		Sierra	
			x	Differential Driver		Type 422		Sierra	
			x	Analog Reference Amplifier				Sierra	50
			x	Voltage to Current Converter				Sierra	
	SC80000		x	8-bit ADC		Successive approximationA	1.5 $\mu$ CMOS, Si-Gate	Sierra	
			x	8-bit DAC		Resistor String, Voltage Output		Sierra	
			x	Comparator		High Speed		Sierra	
			x	2:1 Analog MUX				Sierra	55
			x	2:1 Analog MUX				Sierra	
			x	2:1 Analog MUX				Sierra	
			x	4:1 Analog MUX				Sierra	
			x	4:1 Analog MUX				Sierra	
			x	4:1 Analog MUX				Sierra	
			x	Oscillator		Voltage Controlled, 50 MHz		Sierra	60
			x	Crystal Oscillator		32–100 kHz		Sierra	
			x	Crystal Oscillator		2–6 MHz		Sierra	
			x	Crystal Oscillator		6–12 MHz		Sierra	

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FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
Sierra Semiconductor	SC80000		x	Crystal Oscillator		12–20 MHz		Sierra	(Cont'd)
			x	Crystal Oscillator		20–30 MHz		Sierra	
			x	Crystal Oscillator		30–50 MHz		Sierra	
			x	Compiler-RAM				Sierra	
	SC8000 SC80000		x	Compiler-ROM				Sierra	5
			x	Compiler-PLA				Sierra	
			x	Compiler–2901		Bit Slice Processor		Sierra	10
			x	Compiler-State Machine				Sierra	
			x	Compiler Multiplier		NxN		Sierra	
			x	OP-AMP, Internal		Gain ± 89 dB, BW ± 2.8 MHz		Sierra	
			x	OP-AMP, External		Gain ± 89 dB, BW ± 2.8 MHz		Sierra	
			x	OP-AMP, External		Gain ± 90 dB, BW ± 3.5 MHz		Sierra	
			x	OP-AMP, External		Gain ± 90 dB, BW ± 2.9 MHz		Sierra	15
			x	OP-AMP, Internal		Gain ± 90 dB, BW ± 2.9 MHz		Sierra	
	SC70000		x	Core Microcontroller	COPS800		SC70000	Sierra	15
			x				88164	Sierra	
Silicon Systems Inc.	SmartCell		x	8-Bit DAC		12-Volt CMOS	CD	SiliconSys	20
			x	8-Bit ADC			CD	SiliconSys	
			x	ROM (Variable Size)			CC/CD	SiliconSys	
			x	Switched Capacitor Filter			CD	SiliconSys	
Standard Microsystems	Customation		x	UART Transmitter				SMC	25
			x	Comparator				SMC	
			x	Oscillator				SMC	
			x	Analog Switch				SMC	
			x	UART Receiver			Customation 2,3	SMC	30
			x	Baud Rate Generator				SMC	
			x	VCO				SMC	
			x	DTMF Encoder				SMC	
			x	RC Timer	555			SMC	35
			x	Asynchronous Communications Element	8250			SMC	
			x	Interrupt Controller	8259			SMC	
			x	Op Amp				SMC	
			x	RAM				SMC	40
			x	ROM				SMC	
			x	8-Bit A/D Converter				SMC	
			x	8-Bit D/A Converter				SMC	
			x	Core Microprocessor	65C02			SMC	50
			x	SCSI Interface				SMC	
			x	TWINAX	52C50			SMC	
			x	Real-Time Clock	146818			SMC	
Texas Instruments	Standard Cells		x	256x2 SRAM, TS	RA802LH			TI	45
			x	16x8 SRAM, TS	RA408LH			TI	
			x	64x8 SRAM, TS	RA608LH			TI	
			x	128x8 SRAM, TS	RA708LH			TI	
			x	8x14 Three-Port Register File, TS	RF314LH			TI	50
			x	16x8 Three-Port Register File	RF408LH			TI	
			x	64x9 Three-Port Register File, TS	RF692LJ			TI	
			x	2903 Status/Shift Controller				TI	
			x	SRAM				TI	55
			x	ROM				TI	
			x	16x8 Edge-Triggered 3-Port Register File, TS	RF400LJ			TI	
			x	16x8 Edge-Triggered 4-Port Register File, TS	RF401LJ			TI	
			x	16x9 Edge-Triggered 3-Port Register File, TS	RF402LJ			TI	

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

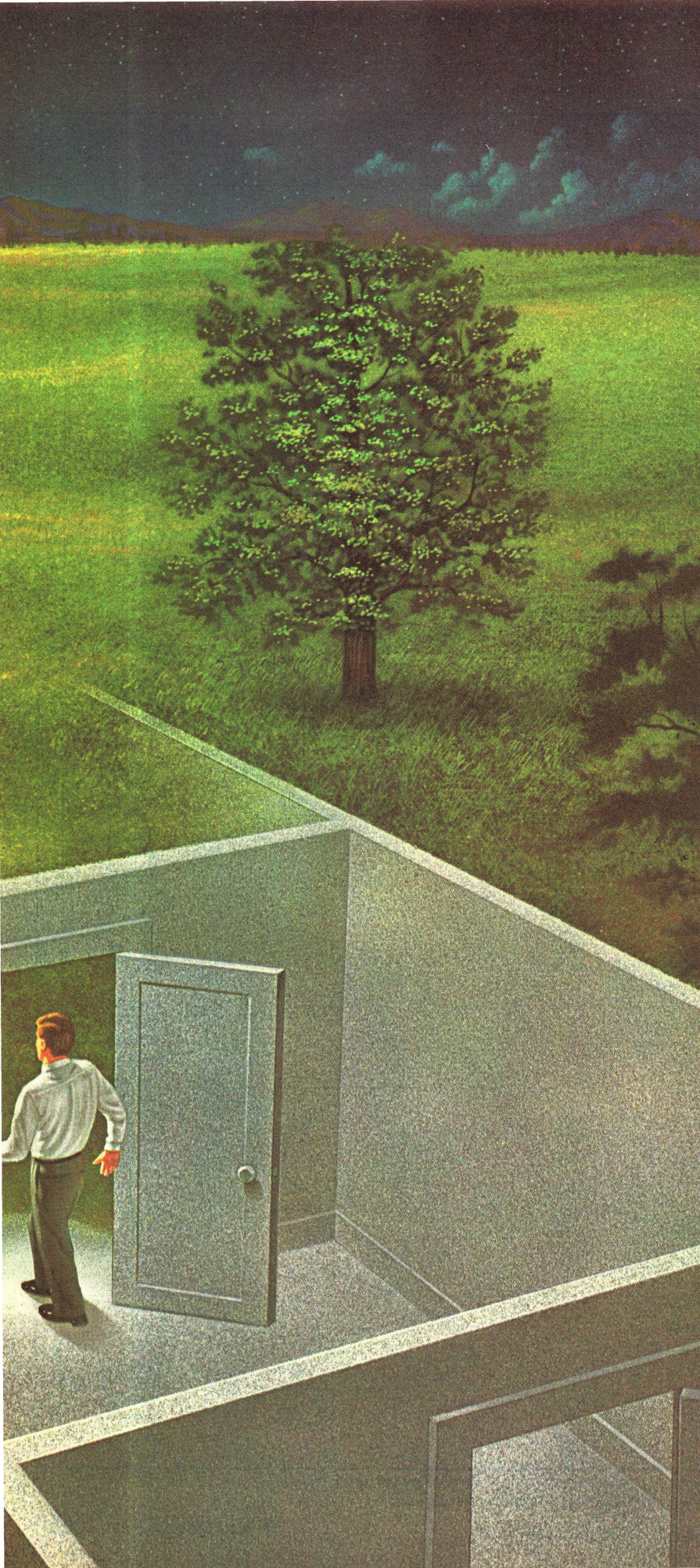
Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
Texas Instruments	Standard Cells		x	64x8 Edge-Triggered 3-Port Register File, TS	RF600LJ			(Cont'd)	
			x	64x9 Edge-Triggered 4-Port Register File, TS	RF601LJ			TI	
			x	64x9 Edge-Triggered 3-Port Register File, TS	RF602LJ			TI	
			x	32x8 FIFO	F1500LJ			TI	
			x	32x9 FIFO	F1501LJ			TI	5
			x	32x9 FIFO, TS	F1503LJ	Expanded Status Indicators		TI	
			x	64x8 FIFO, TS	F1600LJ			TI	
			x	64x9 FIFO	F1601LJ			TI	
			x	64x8 FIFO	F1602LJ	Expanded Status Indicators		TI	
			x	64x9 FIFO	F1603LJ	Expanded Status Indicators		TI	10
			x	128x8 FIFO, TS	F1700LJ			TI	
			x	128x9 FIFO, TS	F1701LJ			TI	
			x	128x8 FIFO, TS	F1702LJ	Expanded Status Indicators		TI	
			x	128x9 FIFO, TS	F1703LJ	Expanded Status Indicators		TI	
			x	4-Bit Microprocessor Slice	2901			TI	15
			x	Look-Ahead Carry Generator	2902			TI	
			x	Status And Shift Controller	2904			TI	
			x	Microprogram Controller	2910			TI	
			x	DMA Controller	8237A			TI	
			x	Internal Timer	8254			TI	20
			x	Interrupt Controller	8259			TI	
			x	Clock Generator Controller	82284			TI	
			x	Bus Controller	82288			TI	
							Standard Cells	TI	
Thomson-Mostek	SA, SB, Standard Cells		x	Compilable SRAM		Compilable cells allow customer to configure ckt. in any organization	SAXX, SBXX, STANDARD CELLS	Thomson	25
			x	Compilable multiport RAM				Thomson	
			x	Compilable ROM				Thomson	
			x	Compilable PLA				Thomson	
			x	Compilable Counters				Thomson	30
			x	Compilable Registers				Thomson	
			x	Compilable Shift Registers				Thomson	
			x	Compilable Multipliers				Thomson	
			x	Programmable ALU	74181/74381			Thomson	
			x	bit sliced $\mu$ P	2901			Thomson	35
			x	$\mu$ sequencer	2910			Thomson	
Unicorn Microelectronics	COMPILE		x	UART	82C50	Expandable in 1-bit increments	CMOS	Unicorn	
			x	Micro controller	80C31		CMOS	Unicorn	
			x	4-bit slice	2901			Unicorn	40
			x	First-in First-out Memory		Width and depth configurable		Unicorn	
			x	Dual Port RAM				Unicorn	
			x	Static RAM				Unicorn	
			x	ROM				Unicorn	
			x	PLA				Unicorn	45
			x	512x9 FIFO	4501			Unicorn	
			x	1024x9 FIFO	4502			Unicorn	
			x	Programmable Interval Timer	82C54			Unicorn	
			x	Parallel I/O Port	88C55A			Unicorn	
			x	Priority Interrupt Controller	82C59A			Unicorn	50
			x	Clock Generator	82C84A			Unicorn	
			x	Bus Controller	82C88			Unicorn	
			x	Clock Generator	82C284			Unicorn	
			x	Bus Controller	82C288			Unicorn	
			x	DMA Controller	82C37A			Unicorn	55
			x	Real Time Clock	146818			Unicorn	
			x	Memory Mapper	74HCT612			Unicorn	

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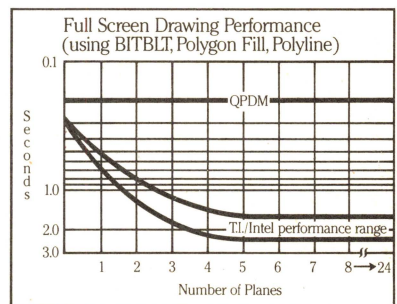
## Don't let reality stop you.

Grab a pad and get to work on tomorrow.

That's how we designed the Am95C60 Quad Pixel Dataflow Manager, a CMOS graphics coprocessor that proves "high performance graphics" is no longer a contradiction in terms.

With a polyline draw speed of 110,000 vectors per second, a BITBLT transfer of 55ns per pixel, and a polygon fill of 20ns per pixel, QPDM can change a screen faster than the speed of thought. (It can redraw a 1K X 1K screen in 0.2 seconds.)

Besides being powerful, this animal is highly trained. The instruction set for full graphics and text primitives is already on the chip. There aren't any extra programming hurdles to slow it down.



Each QPDM addresses four planes. It's cascadable, too. With no degradation in performance. And it can deliver all the color you need.

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## Advanced Micro Devices

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## ASIC/CUSTOM—VLSI/LSI Macrocell Libraries (Cont'd)

Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
VTC Incorporated	VL2000								(Cont'd)
		x		Signal Buffer				VTC	
		x		Shifter, Positive to Negative				VTC	
		x		Shifter, Negative to Positive				VTC	
		x		10KH Input Buffer				VTC	
		x		Differential Input Receiver				VTC	5
		x		Inverting 10KH Output Buffer				VTC	
		x		Non-Inverting 10KH Output Buffer				VTC	
		x		Differential Output Driver				VTC	
		x		Inverting and Non-Inverting TTL Input Buffer				VTC	
		x		Inverting Bistate TTL Output Buffer				VTC	10
		x		Non-Inverting Bistate TTL Output Buffer				VTC	
		x		Inverting Tristate TTL Output Buffer				VTC	
		x		Non-Inverting Tristate TTL Output Buffer				VTC	
		x		Tristate Output Buffer Enable Gate				VTC	
		x		Inverting Open Collector TTL Output Buffer				VTC	15
		x		Non-Inverting Open Collector TTL Output Buffer				VTC	
Waferscale Integration, Inc.	Modular-Cell, CMOS	x		4 Bit Microprocessor Slice	2901		Modular-Cell	Waferscale	
		x		Look Ahead Carry Generator	2902			Waferscale	
		x		4 Bit Microprocessor Slice	2903			Waferscale	20
		x		Status And Shift Control	2904			Waferscale	
		x		Microprogram Sequencer	2909			Waferscale	
		x		Memory Sequencer	2910			Waferscale	
		x		Memory Sequencer	2911			Waferscale	
		x		Priority Interrupt Expander	59013			Waferscale	25
		x		Vectored Priority Interrupt Expander	59014			Waferscale	
		x		16 Bit Microprocessor Slice	59016			Waferscale	
		x		32 Bit Microprocessor Slice	59032			Waferscale	
		x		64K (8Kx8) EPROM	59064			Waferscale	
		x		16K (1Kx16) EPROM	1Kx16			Waferscale	30
		x		1K (128x8) Static RAM	128x8			Waferscale	
		x		16x16 Parallel Multiplier	59316			Waferscale	
		x		Multiplier Accumulator	59510			Waferscale	
		x		Multiplier	59517			Waferscale	
		x		Multilevel Pipeline Registers	59520/21			Waferscale	35
		x		Bidirectional Variable Pipeline Register	59522			Waferscale	
		x		Triple Port RAM	59735			Waferscale	
		x		Funnel Shifter	TBA			Waferscale	
		x		FIFO	TBA			Waferscale	
		x		Barrel Shifter	TBA			Waferscale	40
ZyMOS	Super Cells	x		DMA Controller	8237A		ZyDP-3	ZyMOS	
		x		UART	8250			ZyMOS	
		x		Programmable Interval Timer	8254			ZyMOS	
		x		Parallel I/O	8255			ZyMOS	45
		x		Clock Generator	82284			ZyMOS	
		x		Bus Controller	82288			ZyMOS	
		x		Interrupt Controller	8259			ZyMOS	
		x		Clock Generator	8284			ZyMOS	
		x		Clock	6818			ZyMOS	50
		x		Baud Rate Generator				ZyMOS	
	Block Structured Silicon	x		Interrupt Priority Encoder				ZyMOS	
	Super Cells	x		Configurable RAM				ZyMOS	
		x		Configurable ROM				ZyMOS	
		x		Configurable PLA				ZyMOS	55
		x		Memory Mapper	612			ZyMOS	
		x		Floppy Disk Controller	765			ZyMOS	
		x		Bus Controller	8288			ZyMOS	

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ASIC/CUSTOM-VLSI/LSI Macrocell Libraries (Cont'd)

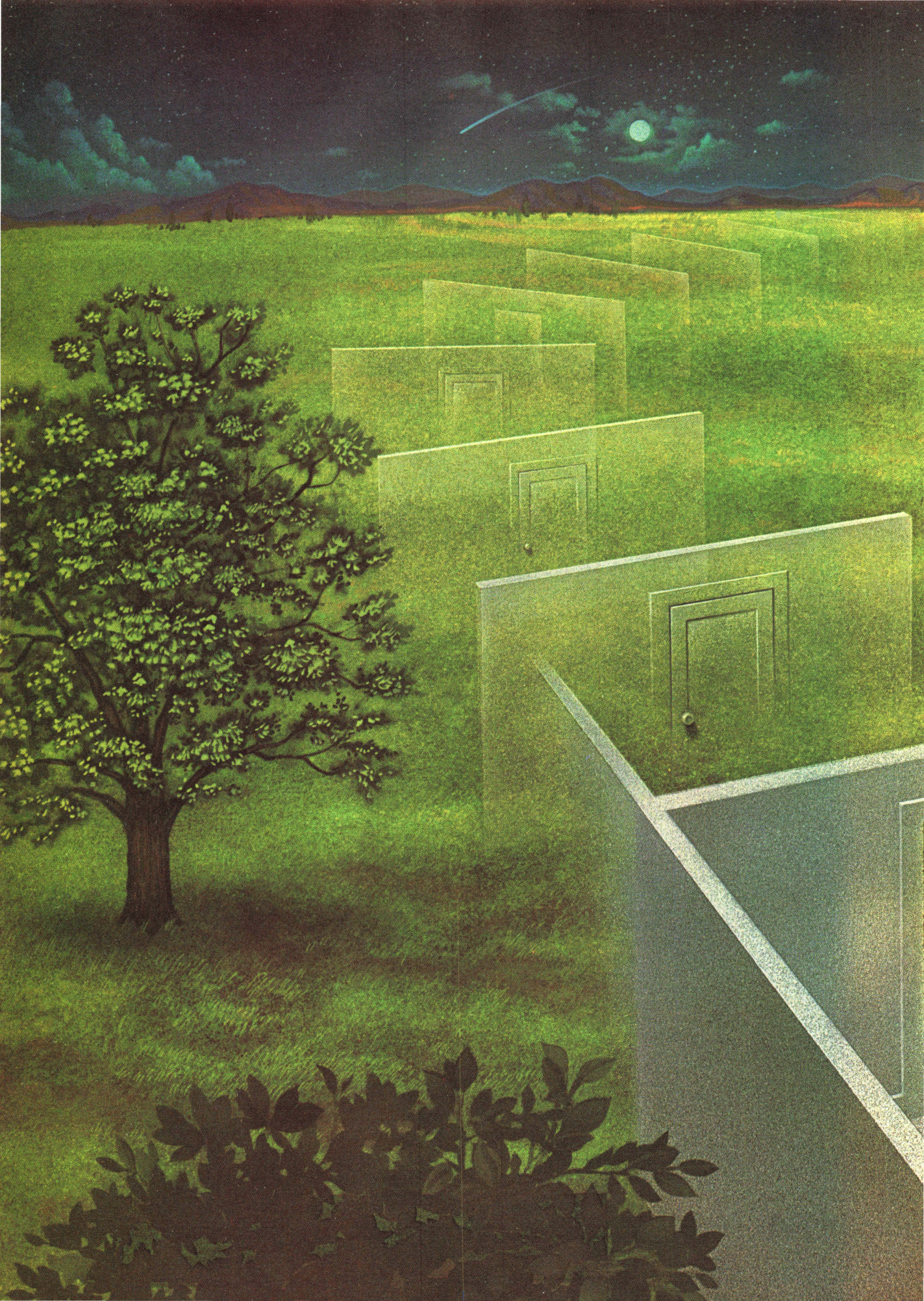
Manufacturer	Device Family	Gate Arrays	Standard Cells	VLSI/LSI Macrocell Function (SSI & MSI Omitted)	Equivalent Discrete Part Number	Comments	Library or Process Name	Source	Line
Unicorn Microelectronics	COMPILE		x	Clock Generator	82384	16, 20 MHz for 80386		Unicorn	(Cont'd)
			x	Integrated Peripherals Controller	82C206	Contains 2x82C37A, 2x82C59A, 82C54, 146818, 74HCT612		Unicorn	
Unicorn Microelectronics	COMPILE		x	First-in First-out Memory 512x9	MK4501	CMOS	Compile	Unicorn	
VLSI Design Assoc.	VD3000, 3μ CMOS		x	16x8 SRAM			Multicell	VDA	5
			x	128x8 SRAM				VDA	
			x	1024x8 SRAM				VDA	
			x	128x8 ROM				VDA	
			x	1024x8 ROM				VDA	
			x	2048x8 ROM				VDA	
VTC Incorporated	VL1000		x	Five Bit DAC			VL1000	VTC	10
			x	Six Bit DAC				VTC	
			x	Seven Bit DAC				VTC	
			x	Eight Bit DAC				VTC	
			x	Five Bit ADC				VTC	15
			x	Six Bit ADC				VTC	
			x	Seven Bit ADC				VTC	
			x	Eight Bit ADC				VTC	
			x	OP AMP-A, 741 Type				VTC	20
			x	OP AMP-B, 741 Type				VTC	
			x	OP AMP-C, 741 Type				VTC	
			x	OP AMP-D, 741 Type				VTC	
			x	Widlar Bandgap				VTC	
			x	PTAT Bandgap				VTC	
			x	Widlar 2-Bandgap				VTC	25
			x	Zener Current Reference				VTC	
			x	External Zener Reference				VTC	
			x	PTAT Current Reference				VTC	
			x	Bandgap Current Source				VTC	
			x	PNP Current Mirror				VTC	30
			x	NPN Current Mirror				VTC	
			x	DAC Bias Generator				VTC	
			x	Comparator	339			VTC	
			x	CML Compatible Comparator				VTC	
			x	Video Amplifier	733			VTC	35
			x	10 mA Voltage Regulator				VTC	
			x	60 mA Voltage Regulator				VTC	
			x	200 mA Voltage Regulator				VTC	
			x	4 MHz Crystal Oscillator				VTC	
			x	TTL Input Buffer				VTC	40
			x	TTL Output Buffer				VTC	
			x	TTL Output Buffer, 3-State				VTC	
			x	TTL Output Buffer, Open Collector				VTC	
			x	Schmitt Input Buffer				VTC	
			x	10K Input Buffer				VTC	45
			x	10K Output Buffer				VTC	
			x	Clock Buffer				VTC	
			x	Signal Buffer				VTC	
			x	Differential ECL 10K Input Buffer				VTC	
			x	Differential CML Comparator with 10 V Input Range				VTC	50
	VL2000		x	Shift Register, 4 Bit			VL2000	VTC	
			x	Counter, 4 Bit				VTC	
			x	Comparator, 5 Bit				VTC	
			x	Carry Look Ahead, 4 Bit				VTC	
			x	Parity Generator Checker, 9 Bit				VTC	55
			x	Full Adder, 2 Bit				VTC	
			x	Priority Interrupt Encoder				VTC	
			x	2901, 4 Bit Microprocessor Slice				VTC	
			x	RAM, 16x4 Dual Port				VTC	
			x	Clock Driver				VTC	60

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FOR ADDITIONAL INFORMATION ON DESIGN TOOLS SEE DESIGN AUTOMATION SECTION

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Analog Devices offers a full spectrum of capabilities in application-specific integrated circuits (ASICs). These chip-level systems can implement designs with 12-bit accuracy and 16-bit resolution that formerly required board-level solutions.

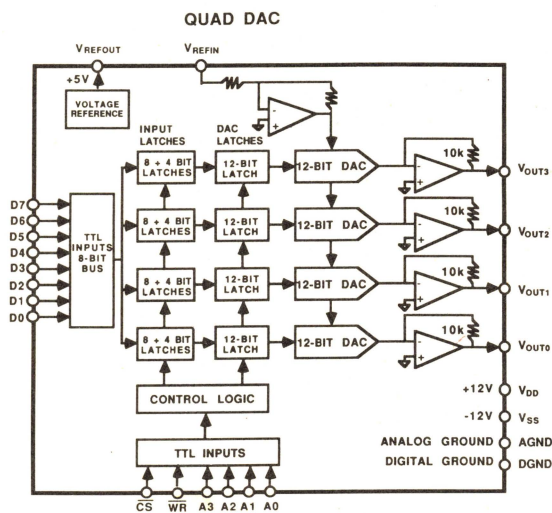
Analog Devices can incorporate most of the functions of its standard monolithic parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a generic predefined system-on-a-chip to your application.

Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, California, and England.

Multiple locations for fabrication, assembly, and testing ensure a ready supply of production parts. Products can be processed in full MIL-38510 certified facilities.

## DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASIC parts. Described here are two examples, a custom chip set and a semicustom chip.



### Quad DAC

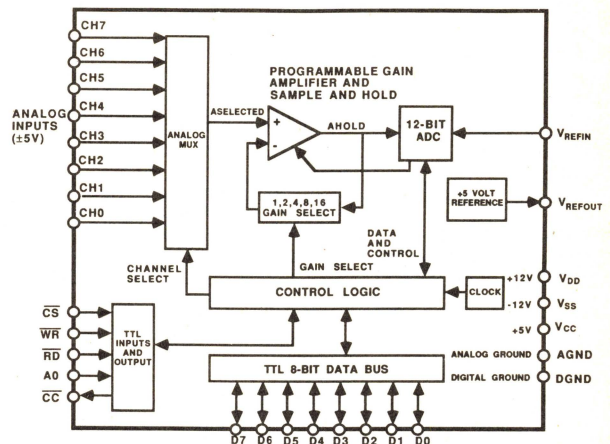
This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously.

### Data Acquisition System

This DAS converts analog signals on 8 input channels to 12-bit values and interfaces via an 8-bit parallel bus. The chip integrates

an 8-channel multiplexer, programmable-gain amplifier, sample-and-hold, and 12-bit A/D converter with internal voltage reference.

DATA ACQUISITION SYSTEM



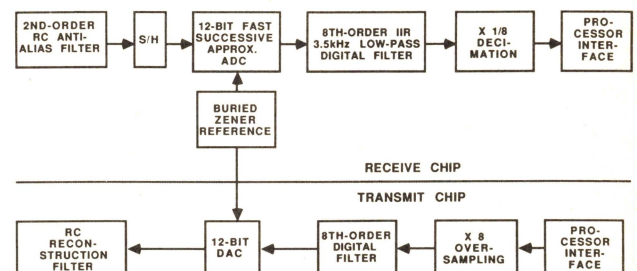
### Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. One such device is a serial-interface DAS. This design was altered to have programmable gains of 1 to 20 instead of 1 to 16, and a serial UART instead of an 8-bit parallel interface. In addition, this part contains a precision instrumentation amplifier, a programmable line-frequency notch filter, a 7-bit trim DAC, and a temperature sensor.

### Modem Chip Set

Library cells can be combined to form macro building blocks for high-speed modems. This two-chip design concept filters and converts data to interface a digital signal processor with the analog circuitry of a 9600-baud modem. On one chip, the received signal passes through an anti-aliasing filter, sample-and-hold, 12-bit A/D converter, 8th-order digital filter, and decimation. On the other chip, transmit data is 8x oversampled, then goes to an 8th-order filter, a 12-bit DAC, and an active reconstruction filter.

HIGH-SPEED MODEM CHIP SET

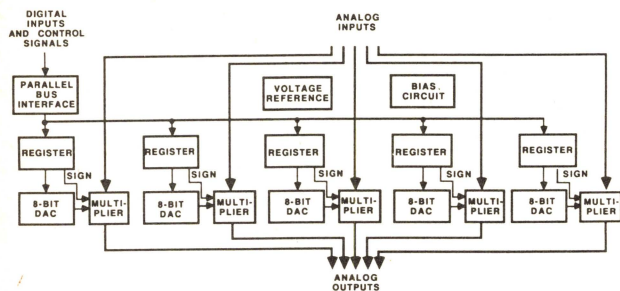




### Transversal Filter Element

This design implements 5 taps of a finite-impulse response filter. Each tap comprises an 8-bit DAC and a multiplier, which handle signals up to 40MHz. A parallel interface sets the tap weights.

TRANSVERSAL FILTER ELEMENT



### HIGH-PERFORMANCE PROCESSES

Analog Devices' semicustom and custom circuits are fabricated using the same high-performance processes as our standard ICs. These technologies include two mixed bipolar-CMOS processes, a high-voltage CMOS process, and high-speed and low-power bipolar processes. These processes can include thin-film resistors, which may be laser trimmed for precise matching and stable performance over a wide temperature range.

The BiMOS II and Linear-Compatible CMOS (LC<sup>2</sup>MOS) processes combine bipolar and CMOS devices on one chip. Functional density is an order of magnitude greater than previous mixed-signal processes; over 20,000 devices can be placed on a single chip. Bipolar transistors provide low-noise, low-offset input stages and high-power output stages. The CMOS devices offer high input impedance, and make dense logic and good switches for data converters and switched-capacitor filters. LC<sup>2</sup>MOS also provides a JFET for very low input noise.

The bipolar-CMOS processes operate on supply voltages ranging from single +5 volts to split  $\pm 15V$ , with signal levels ranging from single-ended +3V to  $\pm 10V$ . These processes are ideally suited for applications in data acquisition, instrumentation, industrial automation, and telecommunications.

The High-Voltage Switch (HVS) process provides quality analog switches that can operate with supply voltages up to  $\pm 22$  volts. It can combine switches and multiplexers with CMOS logic.

The Flash bipolar process makes high-speed linear signal processing, data conversion, and ECL logic functions on one chip. Signal levels are  $\pm 4$  volts with  $\pm 5V$  supplies or +10V with a +12V supply. Applications include disk-drive read/write circuitry and high-speed telecommunications equipment.

The Complementary Bipolar (CB) process features high-speed PNP and NPN devices for precision, low-power linear applications. It also offers low-noise buried-Zener references and dual-gate JFETs. CB runs on +5V to  $\pm 15V$  supplies.

The table below summarizes the processes available for designing ASICs. Other processes in development will offer even higher speed, denser logic, and higher integration of analog and digital functions.

ANALOG DEVICES HIGH-PERFORMANCE PROCESSES FOR ASICs

Process	Power	Signal	Features
BiMOS II	$\pm 12V$	$\pm 5V$	Wide Variety of Precision Linear and Digital Functions
LC <sup>2</sup> MOS	+5 to $\pm 15$	$\pm 3$ to $\pm 10$	Wide Variety of Precision Linear and Digital Functions
HVS	+5 to $\pm 22$	+2 to $\pm 18$	High-Voltage Switches, Muxes and Logic Functions
Flash	$\pm 5$ or +12	$\pm 4$ or +10	High-Speed Linear and Digital Functions
CB	+5 to $\pm 15$	+2 to $\pm 10$	High-Speed, Low-Power Linear Functions



## CELL LIBRARIES

Cell libraries for the bipolar-CMOS processes are described below. These libraries are growing with the development of new processes, macrocells, and cells. Many new catalog parts will also be available as cells. Your local sales office can give you current information on the cell libraries and available generic circuits.

Operational amplifiers are available in bipolar and CMOS configurations. Representative bipolar opamp cells have performance characteristics similar to an AD OP-27 and a slew-enhanced AD741. The LC<sup>2</sup>MOS process offers JFET op amps, including an AD544 equivalent.

Instrumentation amplifiers with performance comparable to the AD521 and AD524 are available. Comparators suitable for 12-bit-accurate applications are available. Linear comparators have response times down to 100 nanoseconds and strobed comparators have setup/access times down to 50 nanoseconds.

Digital-to-analog converters range in resolution from 8 to 14 bits, and include a cell similar to the AD667. Analog-to-digital converters vary from 8 to 12 bits in resolution, and include cells equivalent to the AD7572 and AD574. One half-flash ADC cell converts to 8-bit accuracy in 500 nanoseconds, and one successive approximation-cell converts to 12 bits in 5 microseconds.

Support cells include sample-and-hold amplifiers with performance comparable to the AD585, low-voltage bandgap references comparable to the AD584, and low-noise buried-Zener references.

RC active filters and programmable switched-capacitor filters are available with specifications in these ranges:

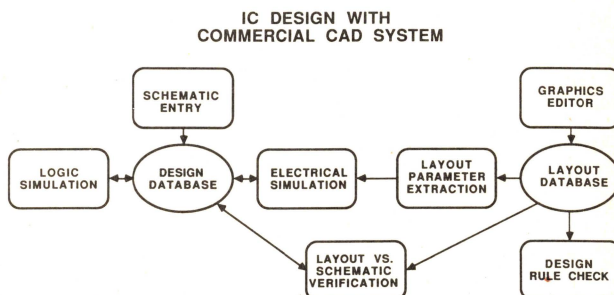
Topology: all classical filter types  
 Frequency Range: 200Hz to 20kHz (switched-cap)  
 Number of Sections: up to 10th-order (switched-cap) or 4th-order (RC)  
 Signal/Noise and THD: >72dB, compatible with 12-bit data acquisition.

Logic cells include gates, counters, registers, PLA, RAM, and ROM. Interface cells include 8- and 16-bit parallel I/O ports and UARTs.

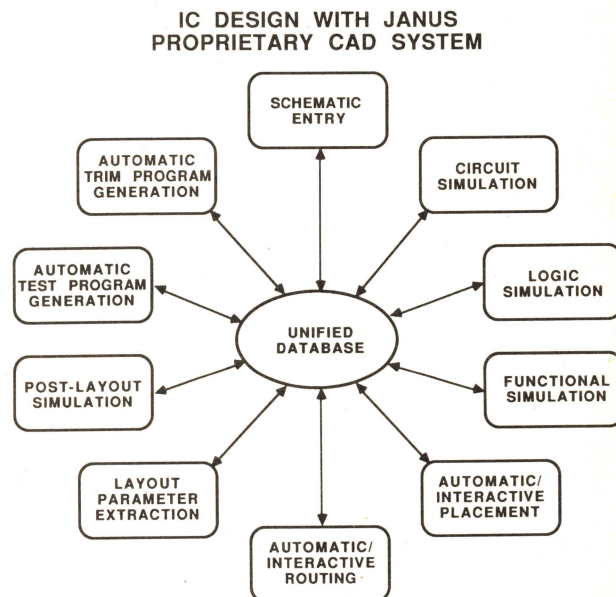
## DESIGN AND LAYOUT

Analog Devices engineers are available to design your integrated circuit, drawing on their years of experience and using powerful computer-aided design (CAD) tools. These comprehensive CAD tools help design, simulate, and lay out the circuit, and aid in generating test programs.

The following figure shows the standard design cycle, which begins with schematic entry. After logic and initial electrical simulation, the designer uses the graphics editor to lay out the circuit. Parasitics and other data are extracted from the layout and circuit operation is simulated again. Finally, the system checks that the layout follows process design rules and matches the schematic.



In addition to using these commercial CAD tools, Analog Devices has developed a proprietary compiler for mixed-signal IC design, called JANUS. By integrating all design functions into one environment with a common database, JANUS reduces design time by an order of magnitude.



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To speed schematic entry, the designer selects devices, cells, and macrocells from comprehensive menus. Device generators allow the designer to specify devices for maximum performance and minimum size. Analog, logic, and functional simulators verify the performance of individual cells and the overall chip design. Placement and routing algorithms complete circuit layouts automatically, yet allow interaction with the designer to handle special cases. When placing devices, JANUS considers thermal and electrical matching as well as die area. An expert system optimizes routing to minimize interconnect length and number of vias. Post-layout simulation comprehends the parasitics of the final routing and is more accurate than the initial simulation.

Future goals for JANUS include automatically generating programs for production trim and test of analog/digital ICs.

### TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, Teradyne, and LTX test equipment. The design, wafer probe, and test areas share data on the network for statistical analysis and device modelling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser-drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

### PACKAGING

Analog Devices ICs are available in most modern package types, including high-pin-count and surface-mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high-performance applications.

#### Available Packages

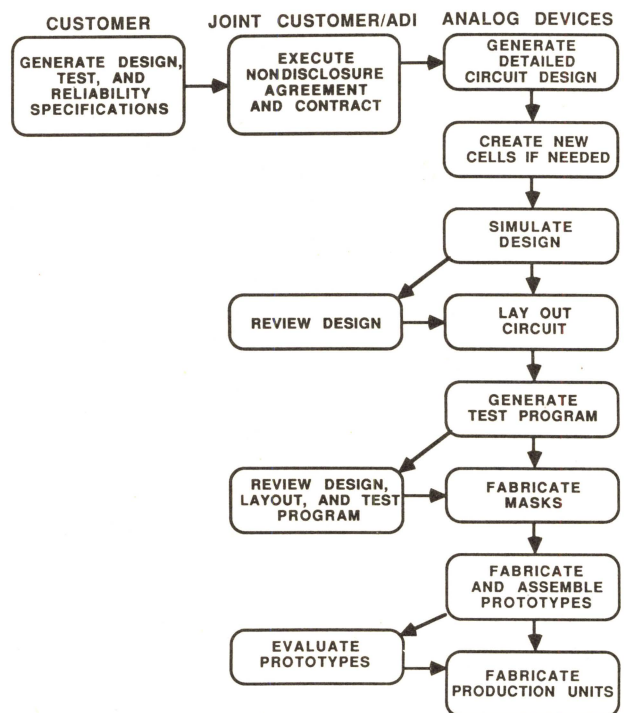
Pin-grid array (PGA): 68 to 144 pins  
Leadless ceramic chip carrier (LCC): 20 to 68 pins  
Plastic leaded chip carrier (PLCC): 20 to 44 pins  
Plastic dual in-line package (DIP): 14 to 64 pins  
Side-brazed DIP: 14 to 64 pins  
Frit-seal DIP (Cerdip): 14 to 28 pins  
Small outline (SO): 14 and 16 pins

### PROGRAM RESPONSIBILITIES AND INTERFACES

The following chart shows the major phases in developing an ASIC, and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices Sales Engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.

### PROGRAM RESPONSIBILITIES AND INTERFACES







# CUSTOM/SEMICUSTOM

## AT&T's ASIC CMOS Standard Cell Product Offering

AT&T's ASIC CMOS Standard Cell product offering is quite flexible and includes the capability for chip design, prototype development and high-volume device production. AT&T can accommodate a customer's ASIC circuit design in a "netlist" format from one of several sources; 1) the "netlist" as developed by the customer at his facility using our library on a Valid, Mentor or Daisy workstation, 2) as developed at the customer's facility using the ported AT&T chip design CAD system, 3) as developed by the customer either independently or jointly with AT&T at one of our worldwide AT&T ASIC Design Centers. Each Design Center is equipped with AT&T's CAD on mainframe computers as well as Valid, Mentor and Daisy workstations.

Of course, AT&T can accept a customer's logic diagram and electrical specifications and our designers will perform the complete design cycle, thus requiring minimal customer interaction at appropriate review intervals prior to prototype mask commitment.

The process outlined above is capable of producing highly complex standard cell designs with a first-time silicon success rate approaching 100%. Our ASIC offering is differentiated by the following features:

- Extensive and Specialized Standard Cell Libraries
- A Versatile Functional Design System
- Parameterized Macroblock Compilers
- Total Commitment to Technology Advancement
- Superior CMOS Performance
- Powerful CAD Tools Designed to Eliminate Risk
- Full Testing Capability and Quality Assurance
- Complete IC Design Support and CAD Tool Training

### Cell Libraries

AT&T's standard cells are predesigned and precharacterized logic elements providing an extensive choice of logic functions as well as speed/size tradeoffs to accommodate a wide range of requirements. The library includes: combinatorial cells, sequential elements, linear functions, input/output buffers and level shifters. In each technology, we supply two versions of our cell library. In one version, cells are area-optimized to minimize chip size. In the other version, cells are larger to maximize performance. The two libraries can be combined on the same chip if necessary.

### Design System

The capability to easily create complex functions is essential to the fast development of any design. That is why AT&T's comprehensive Functional Design System (FDS) meets this need. Complex circuits, however, are made up of more than just simple logic elements. Following simple interactive procedures, a customer can quickly synthesize or compile complex sequential logic functions from simple functional specifications. The functionally synthesized elements available include:

- Adders
- Counters
- Comparators
- Decoders
- Multipliers
- Parity generators
- Universal registers
- Combinatorial cells
- Finite state machines

### Macroblock Compilers

AT&T's Parameterized Macroblock Compilers can solve customer requirements for memory and other special blocks by automatically synthesizing these blocks from a library of primitives, including PLAs, Dynamic Shift Registers, FIFOs, Multipliers and Cross Points. This way the customer gets exactly the capability and configuration needed. And, the customer also gets full CAD support, including automatic multiple block simulation modeling and layout generation. This gives you the advantage of fast development with accuracy and performance on minimum silicon area.

### Technology Advancements

At AT&T, we're constantly shrinking design rules to bring ever greater complexity and performance within the reach of our customers. Our current mainstream VLSI technology is 1.25  $\mu$ m CMOS. And you can bet we're not stopping there! But aggressive technology development means nothing if the finished part won't work. So, to ensure the manufacturability of all of our customers' designs, we process initial prototypes on the same fabrication line that will supply production requirements.

For additional information, contact your AT&T Account Manager, or call:

□ AT&T Technologies, Dept. 51AL230240, 555 Union Boulevard, Allentown, PA 18103 **1-800-372-2447**





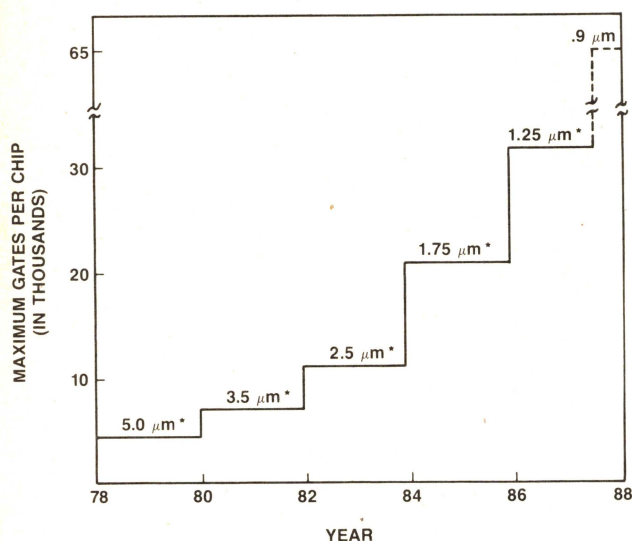
AT&amp;T

# CUSTOM/SEMICUSTOM

## AT&T's ASIC CMOS Standard Cell Product Offering

ASICs/CUSTOM

AT&amp;T



\* CURRENTLY IN PRODUCTION

### Performance

Our high-volume CMOS processes utilize twin-tub epitaxial structures. This enables us to optimize both NMOS and PMOS transistor characteristics for superior circuit performance.

#### CMOS Speed Performance

Gate	Average Gate Delay (ns)	
	1.75 μm (1.3 μL')	1.25 μm (1.0 μL')
Inverter	1.0	0.8
2-Input NAND	1.4	1.0
f-f Setup	2.5	0.7
f-f clk to out	4.5	1.6
Input Buffer	1.5	1.0
Output Buffer (50 pF Load)	5.9	3.5

(Nominal process, 5 V power supply, 25°C, fanout = 3, 2.5 mm wire)

And, when performance requirements are tight, we can make use of our new three-level interconnect system consisting of one level of polysilicide and two levels of aluminum.

The use of the epitaxial layer together with refined layout techniques, eliminates latchup problems. We also incorporate advanced electrostatic discharge (ESD) protection circuitry that exceeds industry standards for Class II ESD protection.

### CAD Tools

Our CAD tools, developed and supported by AT&T Bell Laboratories engineers, will give you high confidence of design success by eliminating manual intervention. Comprehensive audits, full-chip timing simulation, and 100% automatic placement and routing provide that assurance.

The schematic capture tool is flexible, easy-to-use, and offers the powerful features needed for complex VLSI circuits. Auditing features provide early detection of circuit problems, thereby shortening the design cycle. The simulator provides the ability to quickly and accurately verify both the logic and timing requirements. The layout tool handles both standard cells and higher level blocks. Automatic placement and routing assure that even the most complex circuits are properly interconnected.

In addition, using parasitics extracted from the final layout, you can resimulate and verify your circuit over the full range of process, temperature and power supply variations.

### Testing and Quality

Our CAD Test Program Generation (TPG) automatically creates a test program for your design. So the same tests used to verify the design in simulation are used to guarantee the performance of every manufactured part.

State-of-the-art test systems at each of our six manufacturing facilities ensure the operation and performance each customer specifies.

Every device shipped receives not only full operational tests, but is subjected to rigid quality assurance and final inspection procedures. At your option, burn-in can also be provided. Our commitment to quality also includes on-going process evaluations to ensure the integrity of our design and manufacturing techniques.

### Design Support and Training

To familiarize a customer with the use and capabilities of our Design Automation System, we offer design support training courses in our local design centers or at any customer facility. This support can be tailored to suit your particular needs and schedules. Individualized training can also be provided by our experienced design engineers.

We invite you to investigate our capabilities and realize how a partnership in this new generation of technology can work to make your products more competitive in today's world markets.

For additional information, contact your AT&T Account Manager, or call:

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# CUSTOM/SEMICUSTOM

## Semicustom Linear Arrays

### ALA200 UHF Linear Array

#### Complementary NPN and PNP Transistors

##### Description

The ALA200 UHF Linear Array is a semi-custom integrated circuit consisting of very high-frequency uncommitted vertical NPN and PNP transistors, capacitors, and ion-implanted resistors. Designed on a regular grid system, the array provides easy interconnections for the integrated circuit designer.

The ALA200 UHF Linear Array is fabricated with a complementary bipolar process (CBIC) that offers the advantages of similar NPN and PNP transistor characteristics at very high speed. Typical  $f_T$  of 2.5 GHz for PNP and 4.0 GHz for NPN transistors with high current drive capability are unique to this linear array.

Dual-layer metal and thick metal are typically used for most applications; however, single-layer metal may be used upon special request. The bottom and top metal layers have a low sheet resistance of  $<0.03 \Omega/\text{sq.}$  and a current capacity of 2 mA/micron of metal width. The standard  $6 \mu\text{m}$  bottom and  $10 \mu\text{m}$  top metal linewidths are capable of carrying a maximum of 12 mA and 20 mA dc current, respectively. For cases where high-current dc must be

carried, a thicker gold layer called thick metal is available with a sheet resistance of  $<0.01 \Omega/\text{sq.}$  and a current capacity of 14 mA/micron of metal width.

The device is divided into twelve modules, consisting of eight standard, two power, one input, and one trim module. All twelve modules are symmetrically located within the array for ease of layout. Because the modules are on a regular grid system, the user interconnects components by drawing lines on a clearly defined grid marked on a layout sheet.

##### Features

- Quick design turnaround
- Custom circuitry at low cost
- High performance
- Design proprietorship
- High probability of success
- High reliability

##### Component Totals

Component Type	Total**	Number Per Module			
		Standard	Input	Trim	Power
NPN	133	12	12	9	8
PNP	85	7	7	6	8
Implanted Resistors	984	84	84	94	60
Capacitors	62	6	6	6	—
Bonding Pads	44	—	—	—	—

\* L denotes a  $50 \Omega/\text{sq.}$  implanted boron resistor.

H denotes a  $1000 \Omega/\text{sq.}$  implanted boron resistor.

\*\* The UHF Linear Array consists of 8 standard modules, 2 power modules, 1 input module, and 1 trim module.

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# CUSTOM/SEMICUSTOM

## Semicustom Linear Arrays

### ALA300, ALA301 90 Volt Linear Array

#### Description

The ALA300 and ALA301 Linear Arrays provide design engineers the means to obtain 90 volt semi-custom integrated circuits. The single-module array (ALA300) consists of 13 vertical NPN and 15 vertical PNP transistors, three 6 pF capacitors, and 1k diffused and 10k non-implanted resistor banks. The quad-module array (ALA301) is identical to the single-module array (ALA300), but has four times the number of components.

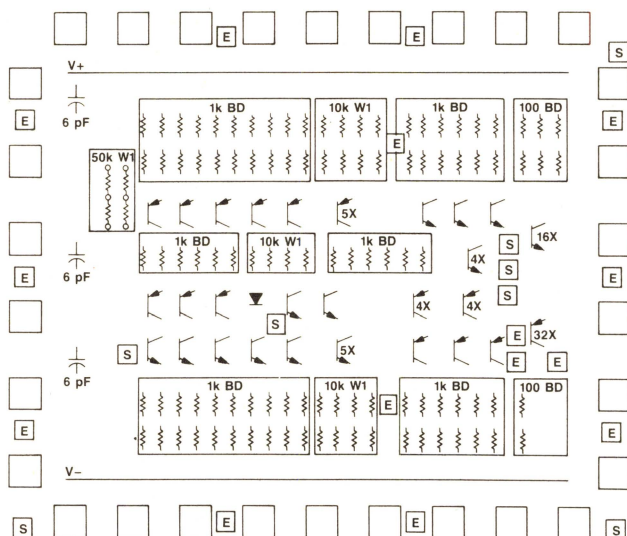
These linear arrays are fabricated using the complementary bipolar integrated circuit (CBIC) process that offers the advantages of vertical NPN and PNP transistors. CBIC technology offers the advantage of designing high-performance circuits with less design complexity. A minimum collector-to-emitter reverse breakdown voltage of 90 volts is guaranteed for both transistors. Typical peak ft of 350 MHz for NPN and 300 MHz for PNP transistors and 5 mA current drive capability for the minimum area transistors are unique for these linear arrays.

Two-level metal is used for interconnections. Upon request a thick-metal interconnect is also available to provide higher current capacity. The top and bottom metal layers have a low sheet resistance of <0.03 ohms/sq and <1.0 ohms/sq with a current capacity of 2.0 mA/micron and 60  $\mu$ A/micron of metal width, respectively. The thicker metal interconnect has a sheer resistance of <0.003 ohms/sq and a current capacity of 20 mA/micron of metal width.

#### Features

- High-frequency performance, typical ft of 350 MHz for NPN and 300 MHz for PNP transistors
- 90 volt capability
- Low development costs
- Quick design turnaround, typically four weeks from design approval
- Complementary vertical NPN and PNP transistors
- Two-level metal interconnect
- 1k and 10k resistor banks
- All I/O ESD protected
- Available in chip form and a variety of standard packages

Schematic of ALA300 Components



#### Component Totals

Component Type	ALA300	ALA301
NPN	13	52
PNP	15	60
Resistors	108	432
Capacitors	3	12
Diodes	1	4
Bonding Pads	30	32

For additional information, contact your AT&T Account Manager, or call:

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### ALA400/401 Linear Array Family

#### Description

The ALA400/401 Linear Array Family is fabricated using the complementary bipolar integrated circuit (CBIC) process that offers the advantages of vertical NPN and vertical PNP transistors. CBIC technology offers the advantage of designing high-performance circuits with less design complexity. A minimum collector-to-emitter reverse breakdown voltage of 33 volts is guaranteed for both transistors.

Typical peak  $f_T$  of 350 MHz for NPN and 300 MHz for PNP transistors and 2 mA current drive capability for the 1 X transistors are unique for these linear arrays. Current drive capability for the other on-chip transistors is linear, e.g., 2 X = 4 mA, 3 X = 6 mA, etc. Pinch-off voltage for JFETs is 1 to 2 volts.  $I_{DSS}$  is about 1.0 mA.

The ALA400 Linear Array is divided into 16 modules, consisting of 12 standard, 2 power and 2 JFET modules. The ALA401 Linear Array is divided into 9 modules, consisting of 7 standard and 2 power modules. All modules are symmetrically located within the array for ease of design layout. Because the modules are on a regular grid system, the user interconnects components by drawing lines on a clearly defined grid, marked on a layout sheet.

Two-level metal is used for interconnections. Upon request, a thick-metal interconnect is also available to provide higher current capacity. The top metal layer has a low sheet resistance of  $<0.03 \Omega/\text{sq.}$  and a current capacity of 2.0 mA/micron metal width. The bottom metal layer has a sheet resistance of  $<1.0 \Omega/\text{sq.}$  and a current capacity of 200  $\mu\text{A}/\text{micron}$  of metal width. The thicker metal interconnect has a sheet resistance of  $<0.003 \Omega/\text{sq.}$  and a current capacity of 20 mA/micron of metal width.

#### Features

- High-frequency performance, typical  $f_T$  of 350 MHz for NPN and 300 MHz for PNP transistors
- 33 volt capability
- Low development costs
- Quick design turnaround, typically six to eight weeks from design approval
- Complementary vertical NPN and PNP transistors
- Two-level metal interconnect
- All I/O ESD protected

#### Electrical Characteristics $T_A = 25^\circ\text{C}$

##### NPN1X Transistor

Symbol	Measurement Condition	Min	Typ	Max	Unit
$h_{FE}^*$	$I_C = 1 \text{ mA}, V_{CE} = 2.5 \text{ V}$	40	85	250	—
$I_C$	80% of peak $h_{FE}$	—	2	—	mA
$BV_{CEO}$	$I_C = 1 \text{ mA}$	33	38	—	V
$BV_{CBO}$	$I_C = 10 \mu\text{A}$	33	50	—	V
$BV_{EBO}$	$I_C = 10 \mu\text{A}$	7.7	8.2	8.7	V
$V_{BE}^{**}$	$I_E = 100 \mu\text{A}$	—	743	—	mV
$R_{sat}$	$h_{FE} = 2$	—	37	—	$\Omega$
$V_{CE}(\text{sat})$	$I_C = 1 \text{ mA}, h_{FE} = 2$	—	70	150	mV
$V_A$ (early voltage)	$I_C = 500 \mu\text{A}$	65	225	—	V
$f_T$	$V_{CE} = 10 \text{ V}$	—	350	—	MHz

\*  $h_{FE}$  match of same type adjacent transistors is within 5%.

\*\*  $V_{BE}$  match of same type adjacent transistors is within 1.5 mV.

For additional information, contact your AT&T Account Manager, or call:

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# CUSTOM/SEMICUSTOM

## Semicustom Linear Arrays

### PNP1X Transistor

Symbol	Measurement Condition	Min	Typ	Max	Unit
$h_{FE}^*$	$I_C = 1 \text{ mA}$ , $V_{CE} = 2.5 \text{ V}$	40	110	250	—
$I_C$	80% of peak $h_{FE}$	—	800	—	mA
$BV_{CEO}$	$I_C = 1 \text{ mA}$	33	47	—	V
$BV_{CBO}$	$I_C = 10 \mu\text{A}$	33	48	—	V
$BV_{EBO}$	$I_C = 10 \mu\text{A}$	7.7	8.2	8.7	V
$V_{BE}^{**}$	$I_E = 100 \mu\text{A}$	—	748	—	mV
$R_{sat}$	$h_{FE} = 2$	—	127	—	$\Omega$
$V_{CE} \text{ (sat)}$	$I_C = 1 \text{ mA}$ , $h_{FE} = 2$	—	140	250	mV
$V_A$ (early voltage)	$I_C = 500 \mu\text{A}$	45	60	—	V
$f_T$	$V_{CE} = 10 \text{ V}$	—	300	—	MHz

\*  $h_{FE}$  match of same type adjacent transistors is within 5%.

\*\*  $V_{BE}$  match of same type adjacent transistors is within 1.5 mV.

### Component Totals (ALA400)

Component	Type	Total	Standard	JFET	Power
NPN	1 X	70	5	5	—
NPN	2 X	12	1	—	—
NPN	3 X	14	1	—	2
NPN	38 X	4	—	—	2
PNP	1 X	70	5	5	—
PNP	2 X	12	1	—	—
PNP	3 X	14	1	—	2
PNP	63 X	4	—	—	2
Resistors*	500 $\Omega$	104	8	4	—
	1 k $\Omega$	168	12	12	—
Resistors**	5 k $\Omega$	216	16	8	4
	10 k $\Omega$	168	12	12	—
Capacitors	—	14	1	1	—
JFETs	—	4	—	2	—
Bonding Pads	—	44	—	—	—

### Component Totals (ALA401)

Component	Type	Total	Standard	Power
NPN	1 X	50	5	4
NPN	3 X	16	2	1
NPN	38 X	2	—	1
PNP	1 X	50	5	4
PNP	3 X	16	2	1
PNP	63 X	2	—	1
Resistors*	100 $\Omega$	42	6	—
	500 $\Omega$	72	8	8
	1 k $\Omega$	64	8	4
Resistors**	5 k $\Omega$	132	16	10
	10 k $\Omega$	100	12	8
Capacitors	—	7	1	—
Bonding Pads	—	38	—	—

\* Denotes a 200 ohm/sq. implanted boron resistor.

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### TE1000, TE2000, TE3000

#### Description

The customized high-speed TTL-ECL gate array family is designed using advanced oxide-isolated (OXIL) bipolar technology. The internal logic gates are built of stacked ECL/EFL gates, and the buffers are a mixture of ECL and TTL for optimum speed/power combinations. The ECL outputs are capable of driving 50-ohm loads. The array is ECL 10K, ECL 10KH, and Schottky TTL compatible.

#### Product Features

- Internal clock frequency of 200 MHz
- Internal gate delay of 0.9 ns, typical
- All ECL outputs drive 50-ohm loads
- Fast turnaround time: 8 weeks from T = 0
- Available mixture of ECL and TTL I/O
- Highly integrated SSI/MSI macro library

#### CAD Features

- Schematic capture
- Multiple delay logic simulation
- Automatic placement and routing
- Design verification
- Test program generation

#### Product Matrix

Series	Maximum No. of Equivalent Gates	Total No. Inputs, Outputs, Input/Outputs	Package Type
TE1000	1000	96 (48 outputs)	68-pin chip carrier; 68-pin plastic multilayer chip carrier
TE2000	2000	84 (84 outputs)	100-pin surface-mount leaded ceramic chip carrier; 104-pin PGA
TE3000	3000	168 (84 outputs)	149-pin PGA
LS2000	2000	84 (84 outputs)	68-pin surface-mount chip carrier; 70-pin PGA; 104-pin PGA

### LS2000

#### Description

The LS2000 high-speed gate array is designed using advanced oxide-isolated (OXIL) bipolar technology. It is compatible with the TTL-ECL series of customized gate arrays. The internal logic gates are built of stacked ECL/EFL gates, and the buffers are LS240 compatible.

#### Product Features

- Internal clock frequency of 200 MHz
- Internal gate delay of 0.9 ns, typical
- Fast turnaround time: 8 weeks from T = 0
- Schottky-compatible I/O
- Highly integrated SSI/MSI macro library

#### CAD Features

- Schematic capture
- Multiple delay logic simulation
- Automatic placement and routing
- Design verification
- Test program generation



# California Micro Devices Corporation

## CORPORATE OVERVIEW

California Micro Devices is a leading producer of high performance, application specific, integrated circuitry (ASIC's) with technologies in CMOS, BICMOS, Bipolar, and Gallium Arsenide. California Micro Devices offers ASIC products across the complete spectrum of design methodologies, from gate arrays, to standard cells, to cell

based custom, to full custom. In addition to ASIC's California Micro Devices is the leading manufacturer of microelectronic based thin film products and offers a broad range of microprocessor, microprocessor peripheral and communication circuits.

## GATE ARRAYS

California Micro Devices offers multiple gate array families so you can choose the one that best suits your application.

We offer arrays from 3 microns down to 1.2 microns with complexities ranging from 200 to 25,000 gates.

## C3000 SERIES

### Features

- Available in seven array sizes from 200 to 3,100 gates
- Up to 216 pins
- Schottky TTL speeds
- Fully characterized over the military temperature range
- Low leakage and standby currents
- Full range of plastic and ceramic packages

### Description

The C3000 Series of gate arrays is manufactured using proven silicon gate 3.0 micron (drawn) CMOS technology. The I/O can be configured as inputs, outputs, bidirectional, CMOS or TTL levels and, with active pull-ups or pull-downs.

Device Number	Gate Complexity	Maximum Pads	Gate Speed	
			Typ.	Max.
C3002	200	28	2.3 ns	3.1 ns
C3004	400	40	2.3 ns	3.1 ns
C3008	800	60	2.3 ns	3.1 ns
C3015	1,500	80	2.3 ns	3.1 ns
C3018	1,800	126	2.3 ns	3.1 ns
C3026	2,600	149	2.3 ns	3.1 ns
C3031	3,100	216	2.3 ns	3.1 ns

## C2000 SERIES

### Features

- Available in seven array sizes from 1,500 to 10,500 gates
- Up to 232 pins
- Silicon gate 2-micron drawn, dual layer metal technology
- Full military capability
- Speeds exceeding TTL logic
- Extensive macro library

### Description

The C2000 Series of gate arrays is manufactured using silicon gate 2-micron drawn gate length, dual layer metal CMOS technology. The speed and range of gate counts make the C2000 series ideal for high performance LSI and VLSI implementation of processors and peripheral controllers.

Device Number	Gate Complexity	Maximum Pads	Gate Speed	
			Typ.	Max.
C2015	1,500	72	1.2 ns	2.2 ns
C2022	2,200	88	1.2 ns	2.2 ns
C2028	2,800	98	1.2 ns	2.2 ns
C2045	4,500	156	1.2 ns	2.2 ns
C2061	6,100	188	1.2 ns	2.2 ns
C2084	8,400	224	1.2 ns	2.2 ns
C2105	10,500	232	1.2 ns	2.2 ns

CALIFORNIA MICRO DEVICES CORPORATION, ASIC DIVISION  
215 TOPAZ STREET, MILPITAS, CA 95035 (408) 263-3214



**Features**

- Available in eight array sizes from 2,600 to 18,500 gates
- Up to 276 pins
- Advanced silicon gate 1.5 micron drawn dual layer metal technology
- Very high performance with .68 ns typical delay for 2-input NAND with fanout of 2
- Full military capability
- Extensive macro cell library
- Large selection of high lead count plastic and ceramic packages
- Workstation support of schematic capture and simulation

**Description**

The C1000 Series is an advanced high performance CMOS gate array family manufactured using 1.5 micron drawn gate length dual layer metal silicon gate CMOS technology with metal one pitch of 4.5 micron and metal two pitch of 5.0 microns. With its extremely high performance, high gate count the C1000 Series is ideally suited to meet requirements for system integration. Operating from a 5 Volt supply the C1000 Series exhibits extremely low power dissipation, typically 16  $\mu$ W/gate/MHz

Device Number	Gate Complexity	Maximum Pads	Gate Speed	
			Typ.	Max.
C1026	2,600	90	.68 ns	1.3 ns
C1032	3,200	98	.68 ns	1.3 ns
C1045	4,500	116	.68 ns	1.3 ns
C1058	5,800	134	.68 ns	1.3 ns
C1082	8,200	164	.68 ns	1.3 ns
C1105	10,500	196	.68 ns	1.3 ns
C1145	14,500	236	.68 ns	1.3 ns
C1185	18,500	276	.68 ns	1.3 ns

**C5000 SERIES****Features**

- Ultra high performance 1.2 micron silicon gate dual layer metal CMOS
- ECL equivalent speeds: .52 ns through 2-input NAND gate
- Up to 280 signal pins
- Full military capability
- Workstation support of schematic capture and simulation
- Extensive selection of high lead count plastic and ceramic packages

**Description**

The C5000 Series of gate arrays is manufactured using an industry leading 1.2 micron drawn gate length dual layer metal silicon gate CMOS process. The C5000 Series is ideally suited for those applications requiring maximum operating performance. With typical power dissipation being 16  $\mu$ W/gate/MHz these arrays have an outstanding speed/power ratio.

Device Number	Gate Complexity	Maximum Pads	Gate Speed	
			Typ.	Max.
C5025	2,500	110	.52 ns	.97 ns
C5055	5,500	140	.52 ns	.97 ns
C5080	8,000	186	.52 ns	.97 ns
C5080M	*8,000	208	.52 ns	.97 ns
C5100	10,000	208	.52 ns	.97 ns
C5150	15,000	240	.52 ns	.97 ns
C5200	20,000	272	.52 ns	.97 ns
C5250	25,000	304	.52 ns	.97 ns

\* C5080M includes 4K bits of high speed static RAM

**GAL8000 SERIES (PRELIMINARY)****Features**

- Gallium arsenide enhancement-depletion process technology
- Drawn gate length of 1.0 micron
- Typical gate speeds of 70 picoseconds
- Complexities from 500 to 2,500 gates
- Second sourcing available from Tachonics

**Description**

The GAL8000 Series is an advanced family of Gallium Arsenide gate arrays designed for systems requirements that exceed CMOS or ECL. The arrays, with drawn gate lengths of 1.0 micron, have typical propagation delays to 70 picoseconds.

CALIFORNIA MICRO DEVICES CORPORATION, ASIC DIVISION  
215 TOPAZ STREET, MILPITAS, CA 95035 (408) 263-3214



California Micro Devices offers standard cells and cell-based custom designs in multiple process technologies so that the best technology is available for each application. For predominantly digital applications, we utilize our industry leading 1.5 micron and 1.2 micron dual layer metal silicon gate CMOS cell libraries. For applications suited for switch capacitor filter design we utilize our

2.0 micron dual layer poly dual layer metal silicon gate CMOS cell library. For designs with demanding digital and analog requirements that are not suited to switch capacitor filter solutions, we utilize a 2.0 micron dual layer metal silicon gate BiCMOS cell library. Finally for those designs requiring operating voltages up to 30 Volts we utilize our Bipolar and ISO CMOS cell libraries.

### Standard Cell and Cell-Based Custom Products

Family Name	CSC200	CSC300	CSC400	CSC500	CSC600	CSC700
Technology	2.5 Mircon Silicon Gate Single Layer Metal CMOS	2.0 Mircon Silicon Gate Dual Layer Metal CMOS	1.5 Mircon Silicon Gate Dual Layer Metal CMOS	1.2 Mircon Silicon Gate Dual Layer Metal CMOS	2.0 Mircon Silicon Gate Dual Layer Poly CMOS <sup>1</sup>	2.0 Mircon BiCMOS Dual Layer Metal
Maximum Complexity	7,500 Gates	18,000 Gates	40,000 Gates	50,000 Gates	16,000 Gates	15,000 Gates
Typical Gate Delay	2.2 ns	1.1 ns	.6 ns	.47 ns	1.1 ns	1.1 ns
Typical D Flip-Flop Toggle Frequency	25 MHz	80 MHz	150 MHz	250 MHz	80 MHz	80 MHz
Typical Power Dissipation	25 $\mu$ W/Gate/MHz	20 $\mu$ W/Gate/MHz	16 $\mu$ W/Gate/MHz	16 $\mu$ W/Gate/MHz	20 $\mu$ W/Gate/MHz	20 $\mu$ W/Gate/MHz <sup>2</sup>
Operating Voltage Range	3 V to 7 V	3 V to 7 V	3 V to 7 V	3 V to 7 V	3 V to 7 V	3 V to 7 V
Ambient Operating Temperature Range	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C
Package Options	Ceramic: DIP, CLCC, PGA, FP, LCC  Plastic: DIP, PLCC, PGA, FP	Ceramic: DIP, CLCC, PGA, FP, LCC  Plastic: DIP, PLCC, PGA, FP	Ceramic: DIP, CLCC, PGA, FP, LCC  Plastic: DIP, PLCC, PGA, FP	Ceramic: DIP, CLCC, PGA, FP, LCC  Plastic: DIP, PLCC, PGA, FP	Ceramic: DIP, CLCC, PGA, FP, LCC  Plastic: DIP, PLCC, PGA, FP	Ceramic: DIP, CLCC, PGA, FP, LCC  Plastic: DIP, PLCC, PGA, FP
Maximum Output Current	48 milliamps	48 milliamps	48 milliamps	48 milliamps	48 milliamps	48 milliamps
I/O Compatibility	CMOS, TTL	CMOS, TTL	CMOS, TTL	CMOS, TTL, ECL <sup>3</sup>	CMOS, TTL	CMOS, TTL, ECL
Cell Library Includes:	120 SSI, 200 MSI, 30 I/O, 30 Analog Macros, RAM, ROM, PLA, Thin film resistors and capacitors	120 SSI, 200 MSI, 30 I/O, 30 Analog Macros, RAM, ROM, PLA, 2901 Bit Slice Family, 8250 UART, 8237, 8254, 8251, 8255, 8-bit and 16-bit core microproces- sors, Thin film resistors and capacitors	120 SSI, 200 MSI, 30 I/O, 30 Analog Macros, RAM, ROM, PLA, 2901 Bit Slice Family, 8250 UART, DMA Controller, Floppy Disk Controller, 8237, 8254, 8251, 8255, 8-bit and 16-bit core microprocessors, Thin film resistors and capacitors	120 SSI, 200 MSI, 30 I/O, 30 Analog Macros, RAM, ROM, PLA, 2901 Bit Slice Family, 8250 UART, DMA Controller, Floppy Disk Controller, 8237, 8254, 8251, 8255, 8-bit and 16-bit core microprocessors, Thin film resistors and capacitors	120 SSI, 200 MSI, 30 I/O, 40 Analog Macros including switch capacitors and thin film integration, RAM, ROM, PLA	120 SSI, 200 MSI, 50 I/O including CMOS and Bipolar, 30 Analog Macros including CMOS and Bipolar, RAM, ROM, PLA, Thin film resistors and capacitors
Second Sources	Ricoh	Ricoh	Ricoh	T.R.W.	I.T.T.	Ricoh

1. 1.5 Micron Silicon Gate Dual Layer Poly CMOS is also available.

2. If BiPOLAR buffers are used, power dissipation will be greater.

3. ECL input compatability only.





CYPRESS  
SEMICONDUCTOR

# CMOS Reprogrammable 20-pin and 24-pin PLDs

## Features

- CMOS EPROM technology for reprogrammability
- Commercial and military temperature ranges
- High reliability
  - 2000V ESD input protection
  - 100% AC/DC tested
  - 100% programming and functional testing
- High speed

## PALC 22V10

- Low Power
  - 55 mA commercial/100 mA military
- Up to 22 input terms and 10 outputs
- Variable product terms
- Programmable output macro cells
  - Polarity control
  - Registered or combinatorial

## PLDC 20G10

- Generic 24 pin PLD, replaces many existing PAL® 24 devices
- Low power
  - 55 mA commercial/80 mA military

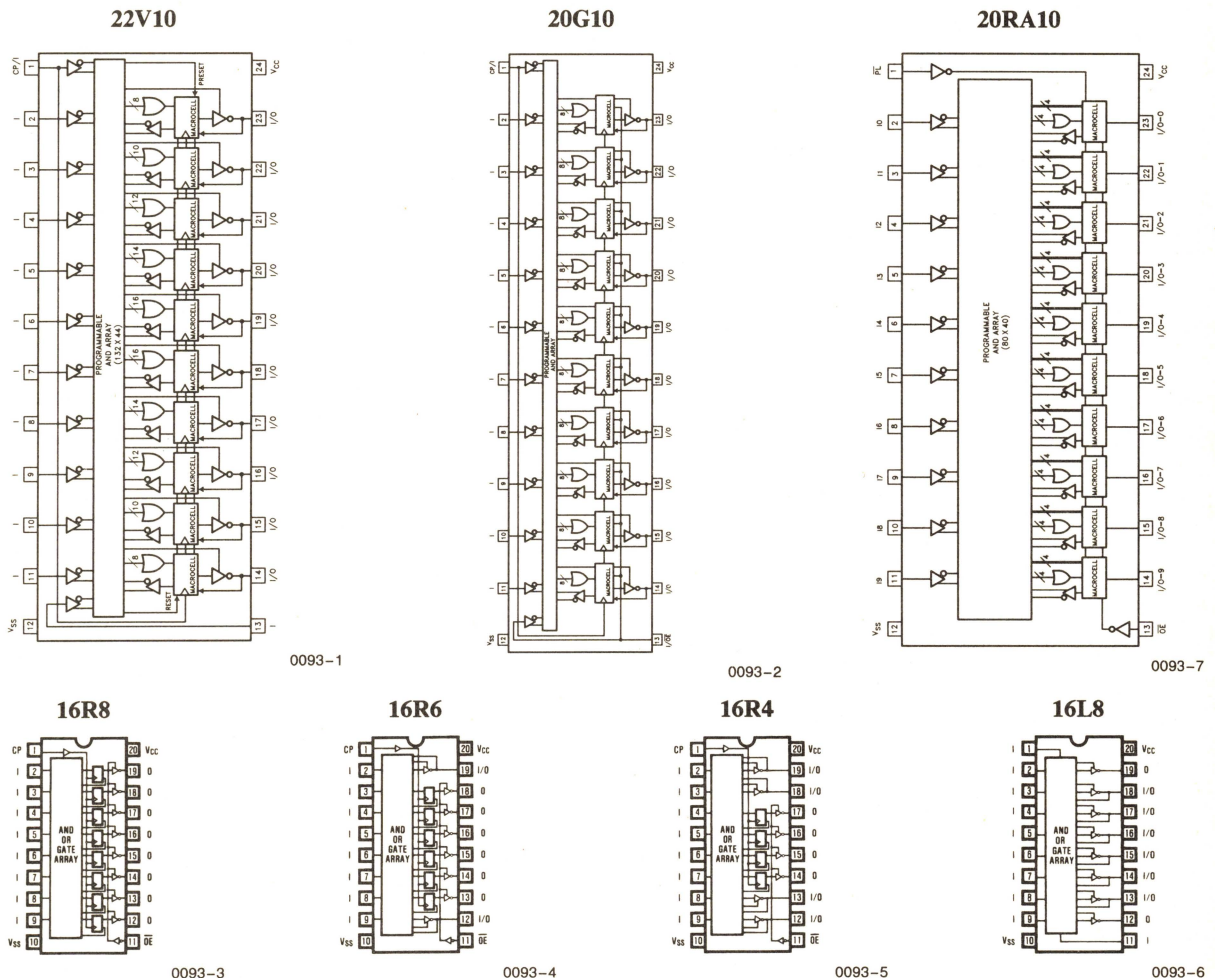
## PLDC 20RA10

- Superior performance
  - $t_{PD} = 20$  ns
- Low power
  - 80 mA commercial/100 mA military
- Programmable output macro cells
  - Combinatorial or asynchronous registered

## PALC 20 Family

- Low power
  - 45 mA commercial/70 mA military

## Logic Symbols and Pin Configurations



PAL® is a registered trademark of Monolithic Memories Inc.

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October 1987



## Product Description

Cypress Semiconductor offers a broad product line of Programmable Logic Devices. They are the "glue logic" solution to those applications that require fast devices and low power consumption. Utilizing a 1.2 micron CMOS EPROM technology all Cypress PLDs are reprogrammable, fast, and low power. Additionally, they all feature: 2000V Electro-Static Discharge protection on all inputs and outputs, 10% power supply tolerances, Security fuse to protect patterns, and 100% factory testing of programmability and functionality made possible by EPROM technology. Each product family has unique features.

The PALC 22V10 is a very flexible logic design solution. This 24 pin device has up to 22 inputs, 10 outputs, and a variable number of product terms dedicated to each output. User-programmable Macro Cells control each output. Each Macro-Cell output can be programmed for output polarity, whether it is registered or combinatorial, and whether it will feedback to the array. Since each output has a Macro-Cell, the 22V10 is very flexible and can emulate just about any PAL® 24 device, or serve as a "custom" design. Additional features include a synchronous PRESET and asynchronous RESET product term that controls all the outputs for initialization purposes.

The PLDC 20G10 is the "GENERIC" PAL 24 solution. It is designed to emulate many existing PAL 24 devices including the 20L10, 20L8, 20R8, 20R6, 20R4, 20L2, 18L4, 16L6, 14L8, and the 12L10. Again Macro-Cells are used on each output to control whether it is Registered or Combinatorial. The 20G10 can actually be configured to emulate any combination of inputs and registered or combinatorial outputs. The 20G10 is the lower cost solution that still features flexibility, high speed, and low power.

The PALC 20 Family includes the 16L8, 16R8, 16R6, and 16R4. These reprogrammable devices feature propagation delays of 25 ns commercial and 20 ns military at 45 mA and 70 mA respectively. They are designed to directly replace existing devices while offering the high speed, low power, and high reliability solution.

The PALC20RA10 provides a superior-performance CMOS replacement for the bipolar 20RA10. With propagation delays of 20 ns commercial and 25 ns military at 80 mA and 100 mA respectively, this device qualifies as a truly high performance solution. Since all registered functions are controlled by product terms, the 20RA10 is capable of fully asynchronous operation.

## Selection Guide

Generic Part Number	I <sub>CC</sub>			T <sub>PD</sub>		T <sub>S</sub>		T <sub>CO</sub>	
	L	Com	Mil	Com	Mil	Com	Mil	Com	Mil
22V10-15	55	90	—	15	—	12	—	10	—
22V10-20	—	—	120	—	20	—	17	—	15
22V10-25	55	90	120	25	25	15	20	15	20
22V10-30	—	—	120	—	30	—	25	—	20
22V10-35	55	90	—	35	—	30	—	25	—
22V10-40	—	—	100	—	40	—	35	—	25
20G10-15	—	70	—	15	—	12	—	10	—
20G10-20	—	—	100	—	20	—	17	—	15
20G10-25	—	55	—	25	—	20	—	15	—
20G10-30	—	—	80	—	30	—	25	—	20
20G10-35	—	55	—	35	—	30	—	25	—
20G10-40	—	—	80	—	40	—	35	—	25
20RA10-20	—	80	—	20	—	10	—	20	—
20RA10-25	—	—	100	—	25	—	15	—	25
20RA10-30	—	80	—	30	—	15	—	30	—
20RA10-35	—	—	100	—	35	—	20	—	35
16XX-20 [1]	—	—	70	—	20	—	20	—	15
16XX-25 [1]	45	70	—	25	—	20	—	15	—
16XX-30 [1]	—	—	70	—	30	—	25	—	20
16XX-35 [1]	45	70	—	35	—	30	—	25	—
16XX-40 [1]	—	—	70	—	40	—	35	—	25

**Note 1.** The 16R8's outputs are all registered, so it doesn't have a t<sub>PD</sub> spec. The 16L8's outputs are all combinatorial, so it doesn't have t<sub>S</sub> or t<sub>CO</sub> specs. XX = R8, R6, R4 or L8.

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CYPRESS  
SEMICONDUCTOR

# CMOS Reprogrammable Synchronous State Machine

CY7C330

ASICs/CUSTOM

Cypress Semiconductor

## Features

- 12 I/O macro cells each having:
  - registered, three-state I/O pins
  - input register clock select multiplexer
  - feed back multiplexer
  - output enable (OE) multiplexer
- All twelve macro cell state registers can be hidden
- User configurable state registers—JK, RS, T, or D
- 50 MHz operation
  - 5 ns input setup and 15 ns clock to output
  - 20 ns input register to state register
- Low power
  - 30 mA quiescent  $I_{CC}$
  - 120 mA maximum  $I_{CC}$
- 28 pin 300 mil DIP, LCC
- Erasable and reprogrammable

- 256 product terms—32 per pair of macro cells, variable distribution

## Product Characteristics

The CY7C330 is a high-performance, eraseable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

The unique architecture of the CY7C330, consisting of the user-configurable output macrocell, bi-directional I/O capability, input registers, and three separate clocks, enable the user to design high performance state machines that can communicate either with each other or with microprocessors over bi-directional parallel busses of user-definable widths.

The three separate clocks permit independent, synchronous state machines to be synchronized to each other. The two input clocks, C1, C2, enable the state machine to sample input signals that may be generated by another system and that may be available on its bus for a short period of time.

The user-configurable state register flip-flops enable the designer to designate JK, RS, T, or D type devices, so that the number of product terms required to implement the logic are minimized.

The major functional blocks of the CY7C330 are (1) the input registers and (input) clock multiplexers, (2) the EPROM (AND) cell array, (3) the twelve I/O macrocells and (4) the four hidden registers.

## Block Diagram and DIP Pinout

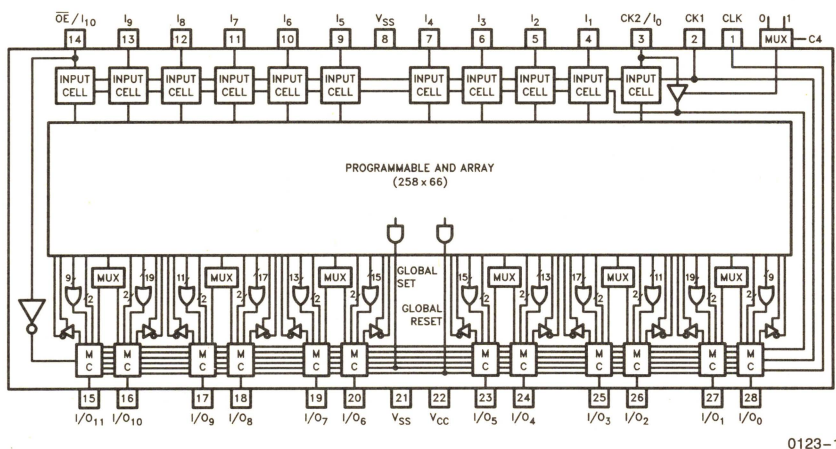
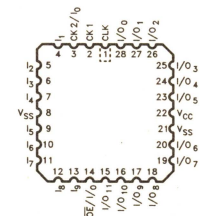


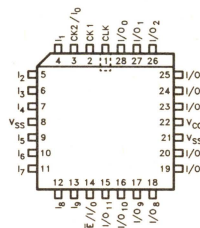
Figure 1

### LCC Pinout



0123-2

### PLCC Pinout



0123-3

## Selection Guide

		CY7C330-50	CY7C330-40	CY7C330-33	CY7C330-28
Maximum Operating Frequency (MHz)		50	40	33	28
Maximum Operating Current (mA)	Commercial	120		120	
	Military		150		150

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October 1987





CYPRESS  
SEMICONDUCTOR

# CMOS Reprogrammable Asynchronous Registered EPLD

CY7C331

## Features

- 12 I/O Macrocells each having:
  - One state Flip-Flop with an XOR sum or products input
  - One feedback Flip-Flop with input coming from the I/O pin
  - Independent (product term) set, reset, and clock inputs on all registers
  - Asynchronous bypass capability on all registers, under product term control ( $r = s = 1$ )
  - Global or local output enable on tristate I/O
  - Feedback from either register to the array
- 192 product terms with variable distribution to macrocells
- UV-Eraseable and Reprogrammable

- 13 inputs, 12 feedback I/O pins, plus 6 shared I/O macrocell feedbacks for a total of 31 true and complementary inputs
- High speed/low power
- Programming and operation 100% testable

## Product Characteristics

The CY7C331 is the most versatile PLD available for asynchronous designs. Central resources include 12 full D-type Flip-Flops with separate set, reset and clock capability. For increased utility, XOR gates are provided at the D-inputs and the product term allocation per Flip-Flop is variably distributed.

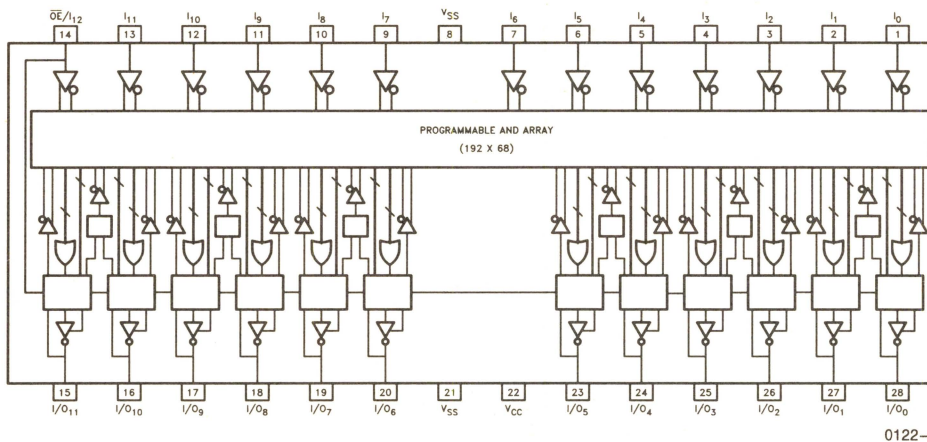
## I/O Resources

Pins 1 through 7 and 9 through 14 serve as array inputs; pin 14 may also be used as a global output enable for the I/O macrocell tristate outputs. Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be managed as inputs or outputs depending on the configuration and the macrocell OE terms.

Twin ground connections placed centrally on the package help minimize ground loop noise when outputs are driven simultaneously into heavily capacitive loads.

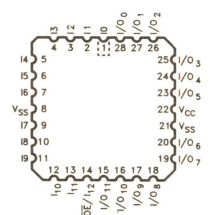
Innovative I/O cell design allows the macrocell state register to be hidden while preserving use of the input register.

## Block Diagram and Pinouts



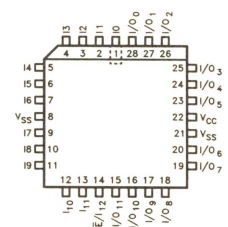
0122-1

### LCC Pinout



0122-2

### PLCC Pinout



0122-3

## Selection Guide

Generic Part Number	I <sub>CC</sub> mA		tpd/t <sub>CO</sub> ns		T <sub>S</sub> ns	
	Com	Mil	Com	Mil	Com	Mil
7C331-25 (-30 Mil)	180	200	25	30	20	25
7C331-35 (-40 Mil)	180	200	35	40	25	30

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October 1987





CYPRESS  
SEMICONDUCTOR

## PROM/PLD Programmer CY3000

Quick-Pro™

### Features

- Combined PROM, PLD, and EPROM programmer
- Programs all Cypress CMOS PLDs and PROMs. (All future devices will also be supported)
- Reads bipolar PLDs and PROMs
- Easy to use, menu-driven software
- New device updates via floppy disk
- IBM-PC® plug-in card format, external ZIP-DIP socket
- Compatible with the IBM PC family of computers and plug compatibles
- Programs 24- and 28-pin NMOS and CMOS EPROMs
- One long slot and 256K bytes of memory required
- Designed for present and future NMOS and CMOS devices
- Optional LCC socket adapter

### Description

QuickPro is a development tool for present and future CMOS PROM and PLD devices, and is used within the IBM PC and compatible environment. Older generation bipolar PLDs and PROMs required special programming voltages and current difficult to generate within the IBM PC.

QuickPro is designed for new generation of CMOS PLDs and PROMs which obsolete the older technology, and use a programming technique which is more compatible with low cost programming methods.

QuickPro can also program standard NMOS and CMOS EPROMs and in packages up to 28 pins. And QuickPro is fast; intelligent programming is used to reduce programming time to a minimum.

QuickPro is future oriented. Each I/O pin is fully programmable, allowing the parameters and timing of each device to be handled via software. As new devices become available, they will be supported by QuickPro. Updates are managed by a simple exchange of floppy disks.

QuickPro includes a comprehensive set of commands to make programming PLDs and PROMs as easy as possible.

For PLDs, QuickPro uses the JEDEC standard data format, so present and future logic design tools such as ABEL™, CUPL™, and PALASM™ can be used. QuickPro avoids serial download problems from a PC to a stand-alone programmer. For PROMs, QuickPro reads PCDOS binary files for use with assemblers and compilers. And QuickPro is low cost, each workstation can have one, eliminating the inconvenience of sharing one expensive programmer. All actions are menu-driven, with complete explanations provided on-screen, in clear text. There is no need to look up manufacturer's codes in a table.

### QuickPro Commands

Program device	Read disk file
Select device type	Write disk file
Edit memory	Verify device
Display memory	Blank check device
Read device	Program security fuse
Test PLD device	Fill memory
Calculate checksum	Convert PLD type

### Technical Information

#### Size

IBM PC standard full length card.  
Uses port addresses 300-31F hex.

### Power

+ 5V	1.0 amp
+ 12V	1.0 amp (peak) 0.4 amp average
- 12V	0.05 amp

### Socket Pod

This is the external socket for connection to the device to be programmed or read. It provides a 28-pin 300/600 mil socket for compatibility with a wide range of devices. Other adapters for leadless packages also available. Five filter switches are located on the pod for bypass capacitors according to manufacturers' published programming specifications.

### Memory

256K bytes of total memory is sufficient to operate QuickPro.

### Devices Supported

Cypress CMOS PROMs:

CY7C225, CY7C235, CY7C245, CY7C245A, CY7C251, CY7C254, CY7C261, CY7C263, CY7C264, CY7C268, CY7C269, CY7C271, CY7C281, CY7C282, CY7C291, CY7C291A, CY7C292, CY7C292A, CY7C293A

Cypress CMOS PLDs:

PALC16L8, PALC16R4, PALC16R6, PALC16R8, PALC22V10, PLDC20G10, PALC20RA10

QuickPro can read 20 and 24 pin Bipolar PLDs, for conversion to Cypress PLDs.

EPROMs: (NMOS and CMOS)

2716, 2732, 2732A, 2764, 2764A, 27128, 27256

QuickPro is a trademark of Cypress Semiconductor Corporation.

IBM and IBM PC are registered trademarks of International Business Machines Corporation.

ABEL™ is a registered trademark of Data I/O Corporation.

CUPL™ is a registered trademark of Assisted Technology.

PALASM™ is a registered trademark of Monolithic Memories Inc.

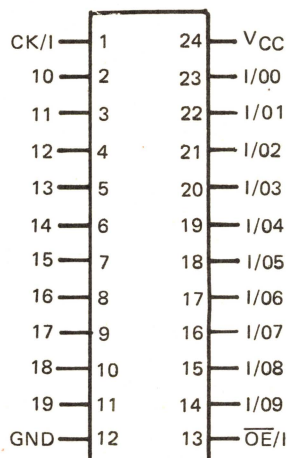
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October 1987



EXEL Microelectronics, Inc.  
A Subsidiary of EXAR Corporation

# ERASIC™ 78C800-CMOS E<sup>2</sup>PLD



## XL 78C800 (E<sup>2</sup>PLD) ELECTRICALLY REPROGRAMMABLE ASIC (ERASIC™)

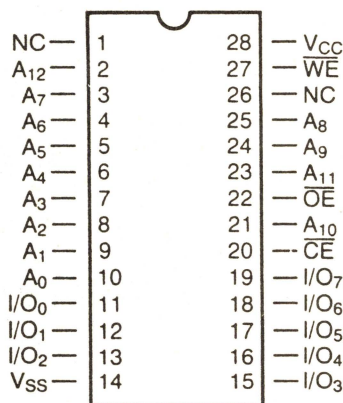
### FEATURES

- 800 Gate Equivalent Complexity
- 24 Pin Skinny DIP
- PAL Pin Out Compatible
- Advanced Logic Architecture
  - Unlimited Boolean Levels with Optional Flip Flops At Any Level
  - Unlimited Term Sharing at Any Level
- 10 K Flip Flops - Any or All of Which May be Buried
- 5 Second Program and Erase Time
- 10 mA Typical Current
- 10 ns I/O + 20 ns/Level Typical Delay

ERASIC is a trademark of EXEL Microelectronics, Inc., 2150 Commerce Drive, San Jose, CA 95131, a subsidiary of EXAR Corp.

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2150 Commerce Drive, PO Box 49007  
San Jose CA 95161-9007 (408) 432-0500  
A Subsidiary of EXAR Corporation

# EXEL'S FAMILY OF ADVANCED E<sup>2</sup>PROMs



## XL2864 A 8K X 8 BIT ELECTRICALLY ERASABLE PROM

### FEATURES

- Fast Read Access Time — 250 ns
- 5 Volt-Only Operation — Including Write
- Fast Nonvolatile Write Cycle — 10 ms max.
  - Automatic Write Timeout
  - Internally Latched Data
  - Internally Latched Address
  - Automatic Erase Before Write
  - DATA Polling Status Indicator
- Automatic Page Write
  - 1 to 32 Bytes in 10 ms max.
- On-Chip False Write Protection
- TTL Compatible Inputs and Outputs
- 10,000 Data Retention
- 10 Year Data Retention
- JEDEC Approved Byte Wide Memory Pinout

### EXEL PRODUCTS

Part Number	Description	Technology
XL2865A	8K x 8 - RDY/BSY	NMOS
XL2864A	8K x 8	NMOS
XL2816A	2K x 8	NMOS
XL2804	512 x 8	NMOS
XL46C15	2K x 8 High Speed	NMOS
XL46C16	2K x 8 High Speed	NMOS



**PRODUCTS, TECHNOLOGY AND SERVICES**

EXAR, early in 1971, pioneered the semi-custom approach to manufacture user specific integrated circuits (USICs) based on the **Master-Chip** concept. Today, EXAR offers a wide variety of linear arrays utilizing more technologies than any of its competitors, and provides the most comprehensive user specific programs in the industry.

**MASTER-CHIP NRE CHARGES****1. 20V Bipolar Technology**

(Industry Standard)

Bipolar	\$ Layout	\$ Integration
A-100		
B-100		
C-100		
D-100 (36V)		
E-100	CONTACT FACTORY	
F-100		
G-100		
H-100		
J-100		
L-100		
M-100		

**2. Bi-FET Technology (36V)**

(Ion Implant Resistors/On-Chip Capacitors)

U-100	
V-100	CONTACT FACTORY
W-100	

**3. 20V Bipolar-Cellular Technology**

(Ion Implant Resistors/On-Chip Capacitors)

CA-100	CONTACT FACTORY
--------	-----------------

**4. 12V Bipolar-High Speed Technology (1.5GHZ)**

Available in full custom.

For semi-custom Master-Chip information, please call factory.

**5. 75V Bipolar-High Voltage Technology**

X-100	CONTACT FACTORY
-------	-----------------

EXAR **Master-Chips**, even though specifically designed for linear circuits, are equally suitable for digital and linear/digital combined circuit implementations.

**MASTER-CHIP DELIVERY SCHEDULES\***

Designs	4-6 weeks
Layouts	2-4 weeks
Integrations	6-8 weeks
Changes	4-6 weeks
Production	10-12 weeks**

\*Schedules are based on moderate circuit complexity and fab workload.

\*\*After approval of prototypes and test specifications.

Note 1: **Master-Chip** is the trade name for EXAR's semi-custom (Bipolar Array) chips.

Note 2: The layout and integration prices are based on less than 80% utilization of the chip area.

Note 3: Integration prices include fifty (50) electrically tested prototypes in Cerdip packages. These prototypes are for electrical evaluation purposes only and are not intended for qualification, unless specifically requested.

Upon request, special packaging (SO, SIP, PGA, PLCC, LCC, Flat Pack, etc.) is available for an additional cost. EXAR can also supply up to 500 additional Cerdip prototypes at a unit cost of \$12.00 each.

Note 4: Integration prices are based on customer submitting a complete Integration Package which consists of:

- ☐ Circuit Schematic
- ☐ Layout (200X Layout Sheet)
- ☐ Bonding Diagram
- ☐ Test Specifications
- ☐ Circuit & Application Description

Note 5: Layout prices are based on customer submitting a complete package which consists of:

- ☐ Circuit Schematic
- ☐ Circuit & Application Description
- ☐ Test Specifications

It is important to recognize that the interconnect of your circuit, based on the layout, is an integral part of your circuit design. It is, therefore, extremely important to indicate all the critical paths, matched resistors and transistors on your circuit schematic.

Note 6: Every effort is made by the Engineering Staff at EXAR to achieve an optimum layout of your circuit. If the finalized layout requires any changes from the original circuit schematic or from circuit specifications you will be notified. Upon agreement, the integration phase will resume.

Note 7: Integration Changes/Modification—If changes are required through no fault of EXAR, additional charges will be required and will depend on the extent of the necessary changes.

Note 8: EXAR has minimum production requirements that are dependent on engineering workload. Please contact EXAR for minimum production requirements.



## SERVICES OFFERED

Depending on the annual volume requirements of the customer and the selectivity criteria, EXAR offers a wide variety of Engineering services. These services are briefly outlined below:

**1. System Design:** This type of design service evolves from the conceptual system description and specification. It requires EXAR to come up with the system design using a block diagram approach. It requires definition of the functional blocks and system implementation with discrete IC blocks to verify the performance, as per the objective specs. Discrete IC implementation of each functional block and determination of the product or circuit specifications required to meet the system performance concludes the System Design.

**2. Circuit Design:** In this type of service, the system is well-defined by the customer in block diagrams and at the discrete IC level. EXAR determines the partitioning of the system and the definition of the product and objective specs. Then the transistor level design of the circuit is implemented to meet the IC specs. For circuit simulation, EXAR's **Master-Chip** models with SPICE/ASPEC programs are also available.

The circuit is breadboarded using the kit parts of the appropriate **Master-Chip**. A fully evaluated and finalized breadboard is submitted to the customer together with the evaluation results and performance characteristics for approval.

**3. Design Assistance:** This service is intended as a joint effort between EXAR and the customer's engineering staff. EXAR's Engineering Staff will work very closely with the customer to define the system and the objective IC specs to achieve the desired performance. EXAR's Engineering Staff will then provide the customer with a conceptual transistor level paper design of the circuit. It will be the customer's responsibility to breadboard and troubleshoot the circuit. EXAR will provide "handholding" during this stage, and assist the customer in determining the test specs and layout of the circuit (optional).

**4. Layout:** After the transistor level circuit schematic of the breadboard is finalized, the 200X **Master-Chip** layout sheets or Electronic Layout Sheets are used to do the interconnect. Since the interconnections of the circuit on the **Master-Chip** is an integral part of the design and can have a significant effect on the performance of the circuit, all critical paths and matched circuit components must be identified and taken into consideration in achieving an optimum layout. This layout sheet along with the test specification of the circuit, provided by the customer, and the pin-out (bonding diagram) form the integration package.

**5. Integration:** This service involves generating silicon from the layout sheet. After the Integration Package is ready, EXAR will take the layout sheet and digitize it. At this stage, EXAR will check the digitized plots versus transistor level circuit schematic. After digitization, Design Rule Check (DRC) is performed to eliminate any violations. The final digitized plots are then used to generate masks (working plates) using automated techniques.

Finally, metallization and passivation (glass or nitride) masking steps are performed on EXAR's premises to finish fabrication of the **Master-Chip** wafers. After the wafer fabrication is completed, prototypes are built at EXAR's in-house Hi-Rel assembly facility.

The prototypes are then fully evaluated and sent to the customer along with a prototype binder which includes all pertinent information. These prototypes are for electrical evaluation purposes only.

**6. Wafer Foundry:** EXAR utilizes its in-house state-of-the-art Class 10 wafer (5" to 6") fabrication line which includes all diffusion processes epi, ion implantation, and a wide variety of deposition processes. Technologies offered cover all bipolar processes, high voltage and silicon gate CMOS. Services are also available for partial or full processing of wafers using customer-owned emulsion or chrome tooling.

## CAE/CAD CAPABILITIES

For years EXAR has been using CAE/CAD design tools extensively for digital gate arrays. Capitalizing on this expertise and implementing technical innovations, we are proud to be the first to introduce design automation utilizing CAE/CAD tools into the area of linear semi-custom arrays. The linear CAE workstation concept, by eliminating the handcrafted layout methods, takes the black magic out of linear semi-custom design. This new, fully-automated linear, semi-custom design methodology utilizes CAE/CAD Daisy "Gate Master" workstations and dual layer metal linear semi-custom arrays.

Auto placement and auto routing workstations drastically reduce the layout and digitizing turnaround times with added reliability. This built-in "correct by construction concept" is attained through on-line layout versus schematic (LVS) check, design rule check (DRC), and electrical rule check (ERC) features included in the design automation software. An additional benefit of design automation is the achievement of higher packing density (higher percent utilization) which enables EXAR to use smaller **Master-Chips** and to pass the cost savings on to our customers.

## MODELS AVAILABLE

For running simulations, SPICE model parameters (AC/DC) are available on bipolar (20V, 36V and 75V) and Bi-FET (36V, ion implant) processes. Contact EXAR for further information.



## ► FULL CUSTOM DESIGNS

EXAR offers direct full custom designs to its customers. However, recognizing the risks, costs, and longer turnaround times involved in full custom development, EXAR also provides full custom conversions.

Full custom conversion is a two-step approach that provides the best of both worlds; quick turnaround time with minimum risk of semi-custom arrays, and the efficient use of silicon with full custom which invariably means reduced unit costs.

The first step is to implement customer's design on one of EXAR's **Master-Chips** to take advantage of the fast integration times as well as very easy, fast and low risk design iteration cycle in comparison to full custom. This enables customers to design and penetrate their product into the market in a short time frame and qualify the product for production rapidly. In addition, any application or production problems that may require design iterations can be implemented at a low cost and with a fast turn-around time. This way, all production oriented problems are fully debugged and the device is production proven in semi-custom form.

The second step, then, would consist of a straightforward full custom conversion to minimize the chip size and hence the unit cost when the device is in full production. This ensures a risk free and a very smooth transition to shipping cost effective, high volume products.

## ► STANDARD CELL LIBRARY

EXAR has developed an extensive library of fully characterized linear standard cells, and is in the process of expanding the library continuously. EXAR presently has over 100 different, fully characterized linear standard cells.

Linear standard cell technique allows customers to design an entire integrated circuit from base layer up, similar to a full custom development without suffering from some of its disadvantages. Please contact EXAR for further information on its Standard Cell Library.

Again, EXAR's state-of-the-art in-house wafer fabrication facility is a key factor in providing highly reliable full custom and standard cell products.

## ► DESIGN MANUALS AND KIT PARTS

A Linear Master-Chip Design Manual is available from EXAR for \$99. This manual shows a step-by-step approach to the design and layout of circuits. It covers one of the most comprehensive and useful analog circuit design aids in the industry, including extensive device characterization, modelling, pre-designed circuit examples and circuit building blocks as well as layout examples. Also contained in this manual are bread-board kit parts which will be used to prove the performance of your circuit. These kit parts come from the same bipolar process that will be used to integrate your circuit. Additional kit parts are available at \$2.50 each.

## ► THREE STEPS TO SUCCESS

Get EXAR To Work For You

### Step 1: Discuss Your Needs With EXAR

We are proud of our quick and flexible response to your needs. During the conception stage of your project, our highly talented Design Engineers can go through the technical options and variations available to you through EXAR. This is done at absolutely no cost to you.

### Step 2: Get a Quotation From EXAR

To help us get an accurate and complete quotation to you faster your request for quotation (RFQ) should contain:

- ☐ A block diagram of your application
- ☐ A schematic at discrete or transistor level
- ☐ The circuit specifications
- ☐ Your volume requirements

The more information you supply us, the sooner we can respond. EXAR can also assist you in compiling this information.

### Step 3: Relax and Enjoy The Services Offered by EXAR

Depending on your requirements, a project may be started with EXAR at YOUR desired level of involvement. EXAR engineering having successfully completed over 1000 user specific projects (automotive, industrial control, telecom, modems, computer peripherals, medical and switch capacitor filter applications), has the necessary expertise to be involved in system design, IC design, layout or integration level. YOUR CHOICE. In either case, throughout the development process, a close contact is maintained between EXAR and your staff. NO SURPRISES.

In addition to our extensive engineering expertise in various user specific applications, as a standard IC manufacturer, EXAR brings years of accumulated engineering know-how and expertise in telecommunications, computer peripherals, data communications, including switch capacitor filters and modems, industrial control, and instrumentation to our customers. All this design expertise is available to you. Make use of our easily accessible wealth of valuable engineering resources now.

EXAR also offers a variety of DIGITAL GATE-arrays. These include state-of-the-art dual metal 3 $\mu$  Si-GATE arrays for high speed applications.



# FLEXAR BETA-array

## ANALOG SEMICUSTOM GATE ARRAYS AS EASY AS DIGITAL

The FLEXAR BETA SERIES revolutionizes linear semicustom with a TWINSTOR, metal mask programmable to either an NPN or a PNP, and a multifunction bonding pad. A cell composed of three TWINSTORS and two resistor groups is repeated throughout all the arrays in the family. With EXAR's Softmacro library (to be 200 circuits) the designer can place and repeat a layout virtually anywhere—they are not limited to specific locations. Analog designs now approach digital.

### SEMICUSTOM AT FULL CUSTOM PRICING

BETA-array implementations are extremely efficient in silicon utilization. Component programmability coupled with the cellular architecture minimizes layout real estate. The area under the bonding pads can also be used as NPNs, PNPs, resistors, and capacitors. Because the optimum ratio of PNP to NPN transistors is always available anywhere on the chip, selection of the BETA-array is based ONLY on the total number of active components.

### FEATURES

**FAST DESIGN TIME:** Use the Softmacro library with the EXAR Development System for the fastest design time ever.

**FAST LAYOUT:** All devices on a grid with repeatable cell structure and programmable NPNs, PNPs and passive components. Shorten layout time further by using Softmacro circuit blocks on the IBM PC/AT.

**MORE RELIABLE:** A new four layer passivation system, improved step coverage, ESD protection, excellent low current performance of NPN/PNPs, and parasitic protection diodes.

**KIT PARTS:** Build a working breadboard of your circuit from the available kit arrays, containing all Softmacros, and kit parts, containing TWINSTORS, PADSTORS, and high current TWINBOOSTORS.

**DESIGN WITH THE IBM PC/AT:** Design your circuit, capture the schematic, simulate it and lay it out with the FLEXAR Integrated Design System (FIDS).

### ONLY THREE COMPONENTS

**TWINSTOR:** The workhorse. It is composed of a dual collector PNP (common base) merged with a dual-emitter common collector NPN. With 9 contacts you can create over 20 active or passive functions.

**PADSTOR:** The bonding pad is merged with a 5 emitter NPN and a large vertical substrate PNP. Use it as a capacitor, high voltage, high current clamp diode or resistor, as well as medium current NPN and PNP.

**TWINBOOSTOR:** Our Sledgehammer! The two TWINBOOSTORS on the largest array are capable of handling up to 500 mA each as NPNs.

### COMPONENT COUNT

	BETA-240	BETA-180	BETA-100
CELLS	80	60	33
TWINSTORS	240	180	99
PADSTORS	48	42	34
TWINBOOSTORS	2	0	0

### KEY SPECIFICATIONS

Breakdown voltage, min BVCEO 26 volts

NPN Current Gain—TWINSTOR BETA @ 1 Ma, 3V = 200 Typical

PADSTOR BETA @ 5 Ma, 5V = 250 Typical

TWINBOOSTOR BETA @ 20 Ma, 3V = 250 Typical

**TEST DEVELOPMENT:** Test Development program is required for all production IC's that are to be tested and guaranteed by EXAR.

**DESIGN REVIEW (Optional):** Prior to start of production, at the customer's request, EXAR will perform a design review. Costs for schematic vs specification analysis will be quoted.

**LAYOUT** 1-3 WEEKS (a function of circuit complexity and percent utilization of silicon)

**INTEGRATION** 3 WEEKS (typical)

### PROTOTYPES

Customer design ..... 25 untested prototypes  
EXAR full turnkey design ..... 25 tested prototypes

### FLEXAR INTEGRATED DESIGN SYSTEM (FIDS)

#### SOFTWARE

(purchased from EXAR)

Shell Development Software  
Schematic Entry Software  
Simulation Software  
Layout Software  
Communications Software  
(at customer's discretion)  
Annual Update

#### HARDWARE

(customer provided)

IBM PC/AT—with 20 Megabyte hard disk, 640K RAM, EGA card, color EGA monitor, modem, co-processor, and 132 column printer. Contact EXAR for details.

### TECHNICAL MANUALS AND KIT PARTS

**ENGINEERING DESIGN MANUAL** (supplied with FIDS) ..... \$99.00  
Array Descriptions, Component Characterization, Softmacro Library, Layout Hints, General System Usage.

**FIDS USERS MANUAL** (supplied with FIDS) ..... \$99.00  
System description, operation, schematic entry, circuit simulation, layout, TYMNET data communications, training.

**KIT PARTS FLA101-FLA104A** ..... each \$3.50

**SOFTMACRO KIT ARRAYS FLA300 SERIES** ..... each \$7.50



## PRODUCTS, TECHNOLOGY AND SERVICES

### ► SERVICES OFFERED

EXAR offers four well-defined levels of interface in the development of user specific CMOS circuits. The level of interface is determined by the customer's needs and EXAR's selectivity criteria. The four service levels are briefly described below. In all cases, throughout the development process, a close contact is maintained between EXAR and the customer.

### ► LOGIC DESIGN

In this type of service, the system is well-defined by the customer. The system is then designed at a functional block diagram level. The next step involves partitioning of the system and determining the objective IC specs.

If verification of the logic design by a breadboard is required, EXAR will submit a breadboard and the evaluation results for customer approval.

### ► LOGIC SIMULATION

In this service, the logic design is captured on EXAR's CAD system using EXAR's well-defined and characterized library of cells. The logic simulation is then performed using CSVs (Circuit Stimulus Vectors), which are generated jointly with the customer. After design verification, if the simulation results dictate any design changes these are implemented jointly with the customer.

If the schematic capture has been done by the customer using a generic library, or that of a leading vendor's, EXAR will perform an automatic programmed conversion to EXAR's library. A logic simulation, as described above, is subsequently performed.

EXAR also offers its cell library on a floppy disk. These are available for Mentor workstations. Customers can start a design at the system level using EXAR's library of cells and run logic simulations on their own system.

### ► LAYOUT

Layout is performed on EXAR's in-house Design Automation System. The mask layout is done by the automatic placement and routing programs with the netlist as the input. Since the netlists are generated as the output from simulations, this guarantees a zero continuity error in the first attempt. More thorough automatic checks such as LVS (Layout vs. Schematic), DRC (Design Rules Check) and ERC (Electrical Rules Check) are then performed to eliminate other possible errors.

When EXAR engineering is satisfied that the design is totally error free, the PG (Pattern Generation) tape is released for mask generation.

Note: If the customer has full IC design capabilities, EXAR can supply the needed layout information upon request. The floppy disks to load these symbolic structures are available from EXAR. After the design and layout is completed, the customer can submit a GDS-II tape to EXAR. In this case, it is very important that the customer also supply EXAR with the test procedures and test specs so that EXAR can evaluate the prototypes prior to submitting them for the customer's final approval.

### ► INTEGRATION

This service involves generating silicon from the PG tape. The PG tape is used to generate the working plates which are subsequently used to process wafers in EXAR's in-house wafer fab facilities. After the wafer fabrication is completed, prototypes are assembled at EXAR's in-house Hi-Rel assembly facility. The prototypes are then fully evaluated and sent to the customer along with a prototype binder which includes all pertinent information. These prototypes are for electrical evaluation purposes only.

### Semi-Custom Development Flow

#### System Design

#### Logic Design

- ☐ System Partitioning
- ☐ Logic Design
- ☐ Objective Specs

#### Logic Simulation

- ☐ Schematic Capture
- ☐ Logic Simulation
- ☐ Netlist Generation

#### Layout

- ☐ Auto-Place
- ☐ Auto-Route
- ☐ Timing Verification
- ☐ DRC/ERC/LVS

#### Integration

- ☐ PG Tape
- ☐ Working Plates
- ☐ Wafer Processing
- ☐ Packaging
- ☐ Testing

► E<sup>2</sup>PLDs**ERASICs™**

These are electrically erasable reprogrammable devices designed for logic replacement.

ERASICs are designed in the state-of-the-art 2 micron, N-well CMOS technology that includes EEPROM devices. They are ideally suited for low volume requirements, where board space, flexibility and performance are at a premium. Since ERASICs are available off-the-shelf, lead-time to prototypes can be as short as hours.

The ERASIC family of devices is offered through EXEL.

► **GATE-ARRAYS****XR-30,000 Series:**

The XR-30,000 series of Gate-Arrays is designed for high speed CMOS applications. These arrays are ideally suited for SSI/MSI packages replacements.

Designed in 3 micron, Dual-layer Metal, P-well CMOS technology, these arrays offer a very high utilization factor. With modest development costs and a short development cycle, the XR-30,000 series can lower product costs significantly.

► **STANDARD CELLS****XR-P3000:**

The XR-P3000 Standard Cell family is designed to handle applications requiring high-speed digital circuitry. The library offers a full range of characterized digital cells, resulting in a significant reduction in lead-time to prototypes.

In addition, the P3000 library contains several analog cells. These cells allow your digital circuitry to communicate with analog devices such as sensors, motors, and oscillators.

Devices designed using the XR-P3000 library of cells are fabricated in 3 micron, dual-layer metal P-well CMOS technology.

**XR-N2000:**

The XR-N2000 Standard Cell library offers some very unique possibilities for product enhancement through technology migration without redesign of the existing design.

The basic technology for the XR-N2000 Standard Cell is 2 micron N-well CMOS. Dual metal layers, dual poly layers, bipolar devices and EEPROM devices can be added on the same basic technology. The cost of these enhancements is incurred only when they are added.

**Analog Cells:**

The N2000 Standard Cell library also has an impressive array of analog cells. These have been designed for most commonly-used analog functions. However, when special analog cells are needed, EXAR provides engineering assistance for designing cells that meet special requirements.

**Macro-cells:**

Macro-cells implement MSI-level functions using primitives from the XR-N2000 library. Functions planned for the XR-N2000 library include modular counters and registers, multiplexers, adders, and magnitude comparators.

Macro-cells are actually software descriptions of the functions, a fact that is made transparent by EXAR's CAD interface, which allows them to be captured and simulated as if they were primitives.

**Mega-cells:**

Unlike Macro-cells, which are actually constructed with cell library primitives, Mega-cells are fully customized, functional blocks. Since Mega-cells are either hand-packed or compiled, extremely high levels of performance and density can be achieved.

Because of their outstanding capability for high density, Mega-cells can be used in implementing the most complex functions. Proposed Mega-cells for the N2000 library include various types of memories, programmable timers, UARTs, microprocessors and high-level analog functions.

**EEPROM cells:**

For many applications, the ability to incorporate some form of non-volatility into the custom design is becoming more and more important. These EEPROM cells are as easy to include in a design as a D flip-flop. They can be electrically erased and reprogrammed.

► **SILICON COMPILERS**

Compiler technology is the wave of the future. Silicon compilers are knowledge-based expert systems that allow system designers (with no IC design expertise) to design ICs, starting with high-level language-like descriptions of the problem.

Promising to transform IC design methodology, compilers will allow designers to focus on creation and definition, instead of implementation.

As compiler technology matures, EXAR will lead the way by offering a mixed analog/digital compiler capability unmatched in the industry.

ERASIC is a trademark of EXEL Microelectronics, Inc., 2150 Commerce Drive, San Jose, CA 95131, a subsidiary of EXAR Corp.

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2150 Commerce Drive, PO Box 49007  
San Jose CA 95161-9007  
A Subsidiary of EXAR Corporation



# Fujitsu Gate Array and Custom Product Guide

## CMOS Technology

GATE ARRAY	Part Number	Basic Logic Cells	I/O Count	Special Functions
<b>UH Series</b>				
1.0 ns Typ./1.5 ns Max. 1.5μ Dual-Well CMOS 3 Layer Metal	C2000UH	20,160 Gates	220 w/Optional Output Drive 3.2 ma/6.4 ma	Internal Clock Drivers, Scan Test Auto-Test Prog. Gen.
<b>UM Series</b>				
1.0 ns Typ./1.5 ns Max. 1.5μ Dual-Well CMOS 3 Layer Metal	C15006UM	15,120 Gates	219 w/Optional Output Drive 3.2 ma/6.4 ma	6,144 Bits RAM 4 x (24 x 64) Single Port 4 x (18 x 64) Dual Port
	C10012UM	10,080 Gates	219 w/Optional Output Drive 3.23 ma/6.4 ma	12,288 Bits RAM 2 ea. 4 x (24 x 64) S-Port 2 ea. 4 x (24 x 64) D-Port
<b>UHB Series</b>				
1.0 ns Typ./1.5 ns Max. 12 ma Balanced Output 1.5μ Dual-Well CMOS 2 Layer Metal	C1200UHB C8700UHB C6000UHB C4100UHB C3000UHB C2200UHB C1700UHB C1200UHB C830UHB C530UHB C330UHB	12,734 Gates 8,768 Gates 6,000 Gates 4,174 Gates 3,066 Gates 2,220 Gates 1,724 Gates 1,233 Gates 830 Gates 530 Gates 336 Gates	220 190 160 160 144 127 112 96 76 68 60	Output Current Options: 3.2 ma, 12 ma, and 24 ma Absolute number of outputs will be determined by the output current option.
<b>AV Series</b>				
1.4 ns Typ./2.2 ns Max. 1.8μ CMOS 2 Layer Metal	C8000AV C6600AV C5000AV C3900AV C2600AV	8,000 Gates 6,664 Gates 5,022 Gates 3,900 Gates 2,640 Gates	160 160 127 127 106	Standard I/O Options Include TTL Compatible, Schmitt Trigger and Tri-State Functions.
<b>AVB Series</b>				
1.4 ns Typ./2.2 ns Max. 10 ma Buffered Output 1.8μ CMOS 2 Layer Metal Low Voltage Series *	C2000AVB C1600AVB C1200AVB C850AVB C540AVB C350AVB	2,052 Gates 1,674 Gates 1,245 Gates 852 Gates 549 Gates 357 Gates	88 76 68 58 48 40	All AVB Outputs Have Buffered High Output Current Options.  * Special low voltage "AVL" series is available
<b>AVM Series</b>				
1.4 ns Typ./2.2 ns Max. 1.8μ CMOS 2 Layer Metal	C4002AVM C2301AVM C1502AVM	4,087 Gates + RAM 2,375 Gates + RAM 1,564 Gates + RAM	120 117 110	2,304 Bits RAM or 4,608 Bits ROM 1,024 Bits RAM or 2,048 Bits ROM 2,304 Bits RAM or 4,608 Bits ROM
STANDARD CELL	Compilable Cells	Super-Macros (2 Input Gate)	Basic Logic Cells (2 Input Gate)	Performance
<b>AU Series</b>				
1.3μ Dual-Well CMOS 2 & 3 Layer Metal	32K RAM, 128K ROM PLAs, Registers Multipliers, ALU	Standard LSI Equiv. Functions (29XX, 68XX, 82XX)	> 40K Gates < 0.8 ns Typ. 2 Input Gate Equivalent	< 1.3 ns Worst Case
<b>AV Series</b>				
1.8μ CMOS 2 Layer Metal	16K RAM, 64K ROM PLAs, Registers	Special LSI Functions	> 13K Gates < 1.4 ns Typ. 2 Input Gate Equivalent	< 2.2 ns Worst Case

CMOS gates have TWO (2) logic inputs.

CMOS I/O gate count and special clock buffer gates are NOT included in the Basic Logic Cell count

The gate count number shown for "Basic Logic Cells" is based upon the maximum usable number of "gates" within the logic array. This number does not include any logic gates associated with the output buffers. It also excludes special clock and bus driver logic that may be included on the chip for enhanced system performance. At Fujitsu, the total number of gates associated with a part type will be greater than the "Basic Logic Cell" number and with some logic applications permit an apparent gate utilization greater than 100%. Fujitsu guarantees a minimum of 90% utilization of the number of "Basic Logic Cells" shown.


**FUJITSU**

## Fujitsu Gate Array and Custom Product Guide

### Bipolar Technology

ECL GATE ARRAY	Part Number	Basic Logic Cells	Equivalent Gates (Full Adder = 11 Gates)	I/O Count & Special Functions
1.0 Micron	ET750	192 Cells	1,056 Gates	64 I/O, 64 ECL Outputs
	ET1500	384 Cells	2,112 Gates	88 I/O, 64 ECL Outputs
220 ps/800 MHz	ET3000	768 Cells	4,224 Gates	120 I/O, 72 ECL Outputs
ECL, TTL, or Mixed	ET4500	1,120 Cells	6,160 Gates	120 I/O, 84 ECL Outputs *
Interface	ET2009M	480 Cells	2,640 Gates	120 I/O, 9.2Kbit RAM *
	ET3004M	720 Cells	3,960 Gates	120 I/O, 4.6Kbit RAM *
				* 136 I/O Optional

BiCMOS GATE ARRAY	Part Number	Basic Logic Cells (Three Input Gates)	Equivalent Gates (Two Input Gates)	I/O Count
1.5 Micron	BC400	430 Cells	645 Gates	52 @ 24mA
	BC800	812 Cells	1,218 Gates	72 @ 24mA
0.8 ns/180 MHz	BC1200	1,248 Cells	1,872 Gates	96 @ 24mA
	BC2000	2,160 Cells	3,240 Gates	112 @ 24mA

LSTTL GATE ARRAY	Part Number	Basic Logic Cells (Three Input Gates)	Equivalent Gates (Two Input Gates)	I/O Count
1.25 ns/150 MHz	B240	240 Cells	360 Gates	40 @ 24mA
1.25 ns/150 MHz	B350	360 Cells	540 Gates	48 @ 24mA
2.4 ns/70 MHz	B350B	352 Cells	528 Gates	60 @ 48mA
1.25 ns/150 MHz	B600	616 Cells	924 Gates	64 @ 24mA
2.4 ns/70 MHz	B700B	720 Cells	1,080 Gates	88 @ 48mA
1.25 ns/150 MHz	B1100	1,120 Cells	1,680 Gates	88 @ 24mA
0.95 ns/185 MHz	B2000	2,108 Cells	3,162 Gates	112 @ 8mA

LSTTL and BiCMOS cells have THREE (3) logic inputs. I/O gate count is not included in Bipolar Logic Cell or Equivalent Gate density numbers.

### Fujitsu Microelectronics Headquarters and Field Sales Offices

California	Santa Clara (HQ)	(408) 562-1000	- Technical Resource Center -
	Campbell	(408) 866-5600	
	Newport Beach	(714) 720-9688	
Texas	Richardson	(214) 233-9394	- Technical Resource Center -
Illinois	Itasca	(312) 250-8580	
Minnesota	Eagan	(612) 454-0323	
Massachusetts	Newton Centre	(617) 964-7080	- Technical Resource Center -
Georgia	Norcross	(404) 449-8539	- Technical Resource Center -
New York	Hauppauge	(516) 361-6565	
Oregon	Lake Oswego	(503) 684-4545	



**FUJITSU**  
MICROELECTRONICS, INC.



### DESCRIPTION

The Fujitsu MB65xxxx/MB66xxxx/MB67xxxx family are a series of high performance CMOS gate arrays designed to provide high density, low power, and operating speeds that are comparable to standard bipolar logic. The AV (MB65xxxx) series is an ideal choice for LSI and VLSI applications that require up to 8000 gates, 2304 bits of RAM, 4608 bits of ROM or for bus interface circuits with high-drive requirements. The AVB (MB67xxxx) series include optional 10 mA buffered outputs and input pull-up/pull-down resistors for easy interfacing with bus organized logic. The AVM (MB66xxxx) series of memory arrays include, in addition to the 1.5K, 2.3K, and 4K gates of logic, two basic sizes of static registered memories:

The C4002 and C1502 have up to 2304 bits of RAM organized in an optional by-nine memory configuration that is system compatible with most modern designs. The 2301 has 1024 bits of RAM that may be configured into any by-four multiple from 256-by-4 to 32-by-32.

The AVM memories contain duplicate decoder and address register logic so that they may be split and used as two independent memories without borrowing any of the unit cells.

All AV, AVB and AVM arrays use the same basic internal cell structure and common logic Macros.

### FEATURES

- 1.4 ns gate delay typical.  
(2-input NAND gate, F.O.=2)
- Static RAM or ROM on chip.
- Silicon-gate 1.8 micron dual metal.
- 100% automatic placement and routing with guaranteed 90% cell utilization.
- Three-state and bidirectional outputs available.
- High-drive output.  
Buffers,  $I_{OL} = 10.0 \text{ mA}$ , available.
- Pull-up/pull-down input buffers available.
- Single 5V power supply.
- TTL compatible I/O, CMOS  
Input and Schmitt trigger input.
- Popular CAE workstations supported.
- Over 100 unit cells available for design.
- Predesigned software macros available. (F-Macros).
- Fast turnaround: 5 weeks after final validation.
- Evaluation samples available.
- Extended temperature range available.

### AV-CMOS SERIES

Device	Part No.	Gates	I/O	Gate Speed	Features
C2600AV	MB654xxx	2640	106	1.4 ns	High Density
C3900AV	MB653xxx	3900	127	1.4 ns	High Density
C5000AV	MB652xxx	5022	127	1.4 ns	High Density
C6600AV	MB651xxx	6664	160	1.4 ns	High Density
C8000AV	MB650xxx	8000	160	1.4 ns	High Density

### AVB-CMOS SERIES

C350AVB	MB675xxx	357	38 (42) <sup>1</sup>	1.4 ns	High-Drive
C540AVB	MB674xxx	549	48 (50) <sup>1</sup>	1.4 ns	High-Drive
C850AVB	MB673xxx	852	58 (60) <sup>1</sup>	1.4 ns	High-Drive
C1200AVB	MB672xxx	1245	68 (68) <sup>1</sup>	1.4 ns	High-Drive
C1600AVB	MB671xxx	1674	74 (76) <sup>1</sup>	1.4 ns	High-Drive
C2000AVB	MB670xxx	2052	88 (92) <sup>1</sup>	1.4 ns	High-Drive

### AVM-CMOS SERIES

C1502AVM	MB662xxx	1564	107 (109) <sup>2</sup>	1.4 ns	4K ROM/2K RAM <sup>3</sup>
C2301AVM	MB661xxx	2375	117 (119) <sup>2</sup>	1.4 ns	2K ROM/1K RAM <sup>3</sup>
C4002AVM	MB660xxx	4087	120 (122) <sup>2</sup>	1.4 ns	4K ROM/2K RAM <sup>3</sup>

### Notes:

1. I/O numbers in parentheses indicate I/O available when no high-drive outputs are used.
2. When ROM is provided.
3. Available options.





# UH CMOS SERIES GATE ARRAYS

**C20000UH**  
**C15006UM**  
**C10012UM**

 January 1987  
 Edition 1.0

## DESCRIPTION

The Fujitsu C20000UH family is a series of highly integrated, low power, ultrahigh speed gate arrays that use silicon gate, triple-layer metal, twin-tub CMOS technology. Ideal for ultrahigh speed LSI applications requiring TTL flexibility, the C20000UH family offers a choice from devices that have a range of 10,000 – 15,000 gates, with RAM on board, to a device with a full complement of 20,000 gates. The UH-CMOS series gate arrays are designed to fulfill your LSI requirements.

Fujitsu's sophisticated LSI Computer Aided Design system, LCAD, optimizes the user interface and fully automates your LSI design. This process gives you error-free LSI devices in a short development time. Fujitsu's LCAD also provides efficient Automatic Test Generation.

The Fujitsu C20000UH family contains three array types: the C20000UH, the C15006UM and the C10012UM. The C20000UH is a 20,000 gate array. The C15006UM is a 15,000 gate array with 6K-bit RAM. The C10012UM is a 10,000 gate array with 12K-bit RAM. Each array type is configured in four blocks of logic gates or RAM, with input/output buffers on the device periphery. A logic gate block is configured in a matrix of 5040 Basic Cells arranged in columns positioned side by side. One Basic Cell is equivalent to a 2-input gate. A RAM block consists of four RAM Cells, with independent address decoders for each RAM Cell. One RAM Cell is equivalent to a 64-word by 24-bit RAM. Your LSI function is fabricated on the chip by interconnecting the Basic Cells, the RAM Cells and the input/output buffers with triple-layer metallization patterns.

## FEATURES

- 1.5 micron silicon gate twin-tub CMOS technology with triple-layer metallization.
- Three array types: 20,000 gates, 15,000 gates with 6K RAM, 10,000 gates with 12K RAM.
- High speed and low power, with 1.0 ns typical gate delay and 15 ns RAM access time.
- Fully supported by Fujitsu's LCAD systems and on popular engineering workstations.
- Fully supported RAM testing.
- Fully supported scan testing for automatic test vector generation.
- More than 100 logic macros, and 38 I/O macros.
- Variety of flexible, expandable RAM macros with control logic.
- Variety of input/output buffer options with TTL compatible levels – inverting and non-inverting, single and multiple I/O's, two 3-state control signals, plus a high output drive option.
- Optimized clock signal distribution for minimized clock skew, fixed layout of 4 clock phases.
- +5 volt single power supply.
- Space-saving pin grid array packages.
- Clock buffer layout options of fixed 4 phase clocking.
- Memory test pin.
- Four levels of design hierarchy for optimal performance and best layout.
- Multiport RAM.

## PRODUCT OUTLINE

Device Name	Part Number	Complexity <sup>1</sup>	Signal Pin (max)
C20000UH	MB600xxx	20160-gate <sup>2</sup>	220
C15006UM	MB610xxx	15120-gate and 6K-bit RAM <sup>3</sup>	219
C10012UM	MB611xxx	10080-gate and 12K-bit RAM <sup>4</sup>	219

### Notes:

1. 2-input gate equivalent
2. Additional 800 gates available for clock distribution circuit
3. Additional 600 gates available for clock distribution circuit
4. Additional 400 gates available for clock distribution circuit



### DESCRIPTION

The UHB series of 1.5μ CMOS gate arrays evolved from the C20K series of 1.5μ 20,000 gate arrays, originally introduced in 1985. Its enhanced performance and increased user flexibility result from the use of a system proven, dual column gate structure and a two layer metal automatic interconnect system.

Internal high-drive clock drivers minimize clock skew across the chip while internal bus performance and integrity is assured by incorporating 3-state transmission gate logic buried beneath the routing channels.

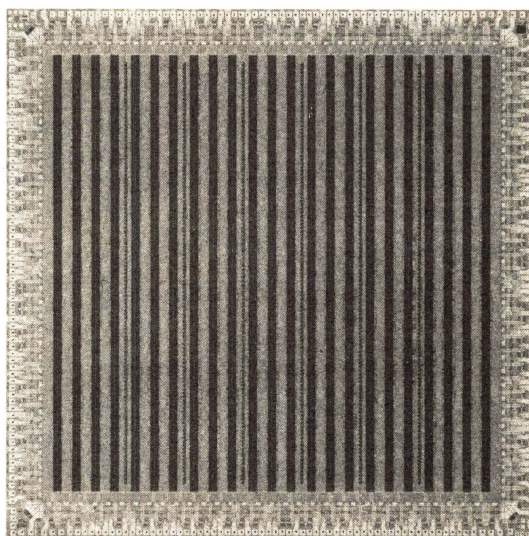
The high-drive output buffers provide highly symmetrical output waveforms. The unique dual-column gate structure increases both density and speed performance, while at the same time optimizing very high gate utilization.

### FEATURES

- High density silicon gate CMOS technology
  - 330 to 12,000 usable gates
  - 80% (to be upgraded to 90%) minimum utilization
- Ultra high speed
  - typical 0.9 ns gate delay
- High sink current capability
  - sink current up to 24 mA
- Built-in feedback resistors for oscillators
- High-current clock drivers
  - low skew clock signal distribution
- Automatic test pattern generation
- Dual column gate structure
- Buried cells within the routing channels
  - high performance internal 3-state bus
- Proven 1.5 micron 2-layer metal technology
  - enhanced from 20,000 gate array family
- Increased number of signal pins for smaller arrays
  - 60 logic I/O for 336 gates
- Passive pull-up/pull-down input buffers
  - on-chip pull-up/pull-down resistors

Device	Utilizable Gates	Max# Logic I/O <sup>1</sup>
C330UHB	336	58 (60)
C530UHB	530	64 (66)
C830UHB	830	74 (76)
C1200UHB	1,233	88 (92)
C1700UHB	1,724	102 (108)
C2200UHB	2,220	115 (123)
C3000UHB	3,066	140 (149)
C4100UHB	4,174	155 (163)
C6000UHB	6,000	155 (163)
C8700UHB	8,768	188 (188)
C12000UHB	12,734	220 (220)

1: The values in parenthesis show the I/O max when no high driving capability ( $I_{OL} = 12mA$  or  $24mA$ ) is used.





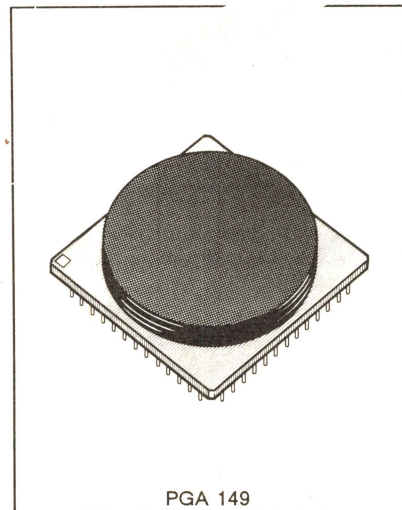
## DESCRIPTION

The Fujitsu ECL Series Gate Arrays family is a group of high speed gate arrays with flexible I/O access. Designed to provide fast ECL internal cells with TTL, ECL, or mixed TTL/ECL input/output buffers, the ET3000 and the ET4500 are ideal choices for LSI and VLSI applications that require up to 4480 gates, with high speed internals and a choice of I/O accesses.

Used in conjunction with Fujitsu's proprietary integrated design system software on popular CAE workstations, the Fujitsu ECL Series Gate Arrays family of devices lets you define the logical functions to be implemented in the array, and gives you the convenience of TTL with the fast computational power of ECL. You get 100% place and route with 90% utilization guaranteed.

The ET3000 and the ET4500 Gate Arrays consist of up to a range of 3072 to 4468 equivalent gates, each made up of a basic cell which may be designed into certain logic functional blocks.

Basic Cell	Equivalent Gate Counts
D Latch	4 gates
Dual 2-input NOR	2 gates
2-input OR-AND/NAND	3 gates
4-input OR/NOR	1 gate



PGA 149

The maximum equivalent gate count for any basic cell is 4 gates. The typical equivalent gate count is 2.5 gates. Eight basic cells form a major cell. The ET3000 chip contains 96 of these major cells for a typical chip total of 768 basic cells used. The ET4500 chip contains 140 of these major cells for a total of 1120 basic cells.

## GENERAL FEATURES

- High speed series gated ECL internal cells.
- Mixed ECL(10K)/TTL input/output buffers.
- 100K series supported upon request.
- tpd = 0.22 ns/gate (no load)
- tpd = 0.50 ns/gate (typical load)
- 5.0 ns/pair of TTL I/O buffer.
- 0.7 ns/gate for each ECL output buffer.

## ET3000 FEATURES

- Up to 3072 equivalent gates
- 72 fixed pin ECL output buffers
- 120 TTL input buffers
- 72 non-fixed pin TTL output buffers
- Typically 6 - 7 W power dissipation
- 149 pin grid array package

## ET4500 FEATURES

- Up to 4480 equivalent gates
- 84 fixed pin ECL output buffers
- 120 TTL input buffers
- 84 non-fixed pin TTL output buffers
- Typically 9 - 10.2 W power dissipation
- 149 pin grid array package

## ECL SERIES

Device	Part No.*	Gates	I/O	Gate Speed	Features
ET3000	MB125△XXX	3072	72/120	0.22 ns/gate (F/I = F/O = 1, L = 0 mm)	High Speed Flexible I/O
ET4500	MB128△XXX	4480	84/120	0.50 ns/gate (F/I = F/O = 3, L = 3 mm)	High Speed Flexible I/O

Note: \* △ will be T, E, or M, based on I/O cell. T means TTL I/O only. E means ECL I/O. M indicates a mixture of TTL and ECL I/O.

## Flexible I/O

I/O Buffer	Power Supply			I/O Buffer	Power Supply		
TTL Level (Pseudo ECL supported upon request)	+5 V	0 V	-	Mixed ECL/TTL Level	+5 V	0 V	-5.2 V
				ECL Level	-	0 V	-5.2 V

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November 1986



# Application Specific Integrated Circuit (ASIC) Products



**GE Solid State**

## Why Turn to GE Solid State for ASICs?

### Full Range of Cost-Effective Design Elements

#### Standard Cells

SC2500	3 micron, double-level metal, bulk Si
SC2800	4 micron, single-level metal, SOS
SC3000	2 micron, double-level metal, bulk Si
SC4000 ADVANCELL™ Family	1.5 micron double-level metal, bulk Si

#### Gate Arrays

PA40000 Series	3 micron, single-level metal, bulk Si
PA50000 Series	3 micron, double-level metal, bulk Si
PA60000 Series	4 micron, single-level metal, SOS
CGA10	2 micron, double-level metal bulk Si
CGA100	1.5 micron, double-level metal bulk Si

### Fully Supported Design Automation Software

**MIMIC** — Logic simulation and fault analysis plus user-definable behavioral modeling with the industry's most extensive hazard analysis.

**FASTRACK** — The most automated design system in the industry. Converts logic netlist to pattern generator types.

**MP2D** — Automated placement and routing of interconnections for Standard Cells.

**VITAL** — Automated placement and routing of mixed standard cell/macro cell chips.

**AUA & MERLYN** — Automatic placement and routing of interconnections for Gate Arrays with utilization capability exceeding 90 percent.

**AFTER** — Test program generation.

**CONCERT** — Connectivity check and parasitic capacitance and resistance extraction of interconnects for both single- and double-level metal.

Accessible from Daisy Systems, Valid Logic, and Mentor Graphics workstations as well as P-CAD and FutureNet on IBM PC.

### Quality and Reliability

In addition to GE Solid State's traditional total commitment to the very highest levels of quality and reliability in the development and manufacture of its products, GE Solid State provides a comprehensive design audit system to assure the customer that the design will work the first time. Moreover, by supplying the design verification samples

and the subsequent production quantities from the same factory and fabrication equipment, the customer is assured of a reliable and quality product that is replicated throughout its production run.

### Service and Support

GE Solid State provides a Training Course in automated Semicustom LSI circuit design as well as technical documentation covering both hardware and software.

The GE/RCA ASIC design program can be entered at several different levels, depending on customer needs.

Engineering support is provided for Daisy Systems, Valid Logic, and Mentor Graphics engineering workstations as well as P-CAD and FutureNet on the IBM PC.

Application Engineers are assigned to the customer for continued design consultation support and service.

Fast turnaround time is available to customer. Production quantities can be delivered 10 to 12 weeks after customer approval of Design Verification sample.

### Long Experience

With more than 20 years of experience producing custom and semicustom parts, GE/RCA products have satisfied the most demanding customers in data processing, industrial, consumer, automotive, and military markets. Over 10 million circuits have been sold in the automotive market alone.

**GE/RCA ASICs have a first-time-success rate of over 95% for the history of the product line.**

## RCA CMOS Application Specific Integrated Circuit Design

GE/RCA ASICs fall into two product groups:

- Gate Arrays
- Standard Cells

Gate Arrays are the simplest semicustom IC. For a logic circuit design based on a gate array, the starting point is the user's list of simulated network connections (net list) and a standardized CMOS base array provided by RCA containing NMOS and PMOS transistors. By the addition of either a single or double layer of metallization, the base array is converted into an LSI logic circuit. The metallization layer is custom designed for a specific application by the customer using RCA software at a computer terminal.

Standard Cells are also building blocks for LSI circuit designs. An extensive library of GE/RCA standard cells and supercells, each designed to provide a specific logic function, are characterized and verified. As with the Gate Arrays, the customer, with GE/RCA training and GE/RCA software, combines these cells into the configuration that best serves the application.



# Application Specific Integrated Circuit (ASIC) Products


**GE Solid State**

After the user-specified circuit design is completed, GE Solid State provides design verification samples for pre-production review. At the customer's option, and after design verification samples are approved, production can be started.

## Gate Arrays

A GE/RCA gate array is a CMOS LSI chip consisting of p devices, n devices, and tunnels in a repetitive ordered structure on either a silicon or a sapphire substrate. All device nodes (gates, drains, and sources) are accessible. Gate arrays are available for both double-level and single-level metallization.

Each gate consists of two p and two n devices and is equivalent to a two-input gate. Although some small number of gates may be inaccessible because of interconnect restrictions, the GE/RCA automatic design process permits utilization of 80% of the total gates available for any one application with single-level metal and often as high as 95% with double-level metal.

Table I gives the basic characteristics of the PA40000, PA50000, PA60000, CGA10 and CGA100 series of gate arrays. The PA50000-series gate-array family is an alternate source for LSI Logic (TM) LSI5000 series. The PA60000 series uses the CMOS/SOS technology and has the advantage of high-speed high-latchup resistivity, and high radiation tolerance.

The CGA10 and CGA100 gate arrays feature a continuous gate-array technology and are an alternate source to VLSI Technology Inc.

An additional CGA10 gate array engineering workstation library (PA70000) is available which is compatible with the LSI logic LSI7000 series.

## Standard Cells

The GE/RCA computer-automated design approach to LSI is based on a group of standard building blocks, called standard cells, that can be automatically chosen, placed, and interconnected by means of computer programs to provide an LSI circuit design.

A large and expanding GE/RCA library of previously designed and verified standard cells and supercells is available in several technologies. The major characteristics of these cell families are given in Table II.

By using a Standard Cell DATABOOK, the designer can match the desired circuit configuration with the available standard cells and generate an input net list. Each multiport standard cell is characterized by its input and output pin connections. Pin connections are accessible for interconnect wiring at both the top and the bottom of each cell. Sophisticated algorithms automatically select the most appropriate I/O connections to minimize wire length and area and to produce a densely packed, efficient layout.

**Table I - Basic Characteristics of the PA40000, PA50000, and PA60000 Series of Gate Arrays**

Library	Technology	Typical Gate Delay at 5V (ns)	Operating Voltage Range (V)	Total Number of Gates	Total Number of Pads
PA40000	3-micron	2.5	3-6	650	74
	Single-Level			850	86
	Metal, Bulk			1000	94
	Si-Gate CMOS			1200	102
PA50000 *	3-micron	2.5	3-6	880	74
	Double-Level			1400	92
	Metal, Bulk			2200	114
	Si-Gate CMOS			3200	138
				4200	156
				6000	180
PA60000	4-micron	2	3-10	650	74
	Single-Level			1200	102
	Metal, Si-Gate				
CGA10 †	CMOS/SOS	2 (Max.)	3-6		
	2-micron			1600	56
	Double-Level			2400	68
	Metal, Bulk			3700	84
	Si-Gate CMOS			6400	108
	Continuous			8400	124
	Gate Technology			10600	140
CGA100 †	1.5-micron	1.4 (Max.)	3-6	1200	152
	Double-Level			16000	172
	Metal, Bulk			20000	196
	Si-Gate CMOS			27000	224
	Continuous			40000	272
	Gate			53000	312
	Technology			67000	348

Note: For 2-input NAND gate operated at 5 volts; fanout = 2, local interconnect.

\* PA50000-Series Gate Array Family is a fully licensed alternate source of LSI Logic's LSI5000-series gate arrays.

† CGA10 and CGA100 Continuous Gate Array® Technology Families are a fully licensed alternate source of VLSI Technologies Inc.

® Trademark of VLSI Technologies Inc.

**GE/RCA Products**



# Application Specific Integrated Circuit (ASIC) Products



**GE Solid State**

**Table II - Major Characteristics of Three Standard Cell Families**

	Double-Level Metal SC2500	Double-Level Metal SC3000	Double-Level Metal SC4000
Gates — maximum number	5000 †	10,000	33000
Operating Voltage Range — Volts	3-6	3-6	3-6
Stage Delay * — nanoseconds	2.3	2.0	0.75
Cell Height — microns	139.7	106.7	88
Pin Spacing — microns	10.67	14.22	8
Channel length — microns	2.6 †	1.5 †	1.5 **
Cell Density — sq. mils/trans.	3	1	0.6
Chip Density — sq. mils/trans.	9	5	3.8

\* For 2-input NAND gate operated at 5 volts; fanout = 2, no interconnect.

† Effective channel length.

\*\* Drawn

## Services Available

The customer of the GE/RCA CMOS ASIC design program is provided with five separate and distinct services for optimizing semicustom circuit requirements. These services are:

**TRAINING** — An extensive network of GE/RCA Design Centers and Design Representatives, utilize the best circuit-design software tools available in the industry. Contact the nearest GE Solid State Sales Office for a list of GE/RCA ASIC Design Centers and Training Facilities.

**SOFTWARE** — Computer library support on P-CAD, FutureNet, Daisy, Mentor, and Valid engineering workstations to simplify net list generation and logic simulation. In addition, GE/RCA MIMIC software can be supported on the user's mainframe VAX computer (VMS 11/730 or larger).

**COMPUTER ACCESS SERVICE** — Minimal charges for use of local terminal and CPU time.

**NRE** — A one-time all-inclusive non-recurring engineering development charge. There are no hidden costs, no add-on extras for design consultation and the like. One half of the charge is payable upon receipt of order. The balance is payable upon delivery of functional design-verification samples (DVs). Production quantity commitments are **not** required for this design development service.

**PRODUCTION** — GE Solid State can deliver production quantities 10 to 12 weeks after approval of the design verification sample. Production is from the same factory that produced the original samples for design verification.

## The ABC's of GE/RCA Semicustom LSI Design

One of the reasons GE Solid State is successful in the semicustom marketplace is the flexibility it provides for

the customer-interface procedure. Because of this flexibility, GE Solid State and the customer can determine the procedure that is in the customer's best interest for an LSI circuit design. The customer's entry level into the design program and the degree of GE Solid State participation are both selected by the customer. The customer, consequently, has maximum control of both the design and the costs.

The three-step design process is charted in Table III below.

## GE/RCA Training Course

A three-day Training Course is conducted at GE/RCA Design Centers. The course is set up to teach customers how to design ASICs using standard cells and gate arrays and design software tools from the GE/RCA comprehensive ASIC Design System.

At this training course the customers review introductory material to MIMIC, learn how to use RCA's VAX 11/782, 8600, or 8800 computers, learn the command structures of the VAX computer and MIMIC, and become familiar with the techniques involved in using engineering workstations. At the workstation, customers start working on their own designs, preferably ones brought with them to the training program.

The training course is so organized that by the afternoon of the first day the customer will begin inputting a network to MIMIC, during the second day start on his own design, and by the end of the training session accomplish the transition from logic designer to integrated-circuit designer.

For additional information on GE/RCA Training Courses, contact the nearest GE Solid State Sales Office.

**Table III - Chart of the Design Process Showing User-Selectable Alternatives**

Entry Level	STEP A Logic Design and Simulation	STEP B Automatic Placement, Routing, and Connectivity Check	STEP C Mask Tooling and Prototype Production
1	GE/RCA	GE/RCA	GE/RCA
2	User	GE/RCA	GE/RCA
3	User	User	GE/RCA

**GE/RCA Products**

# Application Specific Integrated Circuit (ASIC) Products


**GE Solid State**

## 20C51 Microprocessor Macrocell

### Features:

- Industry-standard 8-bit architecture
- 80C51 instruction set
  - Object-code compatible
  - Machine-cycle equivalent
  - Multiply and divide instructions
  - Bit-control Boolean instructions
- 2-Micron CMOS technology - compatible with SC3000 cell library
- IDLE and POWER DOWN modes
- On-chip oscillator
  - 12 MHz at 5 V
  - 3.5 MHz min. freq.
- Temperature range: -40 to +85° C
- Operating-voltage range: 5 volts  $\pm$  20%
- Minimum data-retention voltage: TBD
- Six vectored interrupts - compatible with all five 80C51 interrupt vector address
- Test modes
- 16K program memory-address space - expandable to 64K
- 16K data memory-address space - expandable to 64K
- Emulator chip available for hardware system verification
- Behavioral model available for simulation

The following types are LSI cells in the RCA Cell Library. As such, they can be combined with other cells to build high-performance CMOS application-specific integrated circuits.

## CMOS III 5901

### CMOS 4, 8, 16, or 32-Bit High-Speed Bit-Slice Macro

#### Features:

- 2901 Architecture in CMOS
- Drop in replacement for 2901C
- Expandable in 4-bit increments
- High-speed — Max. clock frequency of 43 MHz (23ns)
- Very low power — 30 mA max. (commercial temperature)
- Eight function ALU — Performs addition, two subtraction operations, and five logic functions on two operands.
- Multiple-address architecture — Provides simultaneous independent access to two working registers.

## CMOS III 5910A

### CMOS Microprogram Controller Macro

#### Features:

- High-Speed Operation — 50 ns clock period
- Low-power — 125 mW
- On-Board Stack — 9 words deep
- Bipolar replacement — Fully compatible with AM2910A
- Four address sources — Microprogram address counter register, LIFO stack, direct data input lines, or register counter.
- Sixteen powerful microinstructions — unconditional and conditional on either register counter state or external condition input or on both.

## CMOS II 4046A

### Phase-Locked-Loop with VCO

#### Features:

- Operating frequency range of up to 18 MHz (typ.) at  $V_{CC} = 5V$
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3V to 6V; digital section 2V to 6V

**GE/RCA Products**



## CUSTOM AND SEMICUSTOM — FROM PLANNING TO PRODUCTION

In the fiercely competitive world of electronics, cost-effective solutions to complex problems are crucial. The move to reduce costs by reducing PCB size and component counts and increasing reliability has led many to the custom IC market. Once you have decided on proprietary circuitry, you may need expert assistance that can be mobilized to do the job quickly and efficiently. Gennum Corporation can provide that assistance.

## YOU DESIGN OR WE DESIGN — CAD

Design your own circuit function with the aid of our design tools or use our team of semi and full custom design experts. Gennum Corporation supports a wide variety of computer aided design tools and platforms for all phases of semicustom circuit design, simulation and every step of circuit development through to physical layout.

## TOTAL IN-HOUSE PRODUCTION CAPABILITIES

We can produce your circuit on one of our semicustom chips — or in full custom, whichever suits your needs. Either way, our team of professionals has the solution to your analog and analog/digital problems. Our fully integrated manufacturing facility allows us to follow through on the total job, from design and masking to prototyping, testing and production.

## INTERNATIONAL REPUTATION

A pioneer in linear bipolar IC design, GENNUM products are sold in almost every country in the world where electronic systems and subsystems are manufactured. We are proud to number some of the world's leaders in electronics among our customers.

SEMICUSTOM BIPOLAR ARRAY COMPONENT LIST (20 V MAX. OPERATING VOLTAGE)						
	LA250			LA200		
ACTIVE COMPONENTS	LA251	LA252	LA253	LA201	LA202	LA204
Small NPN — standard	122	92	52	83	46	17
— schottky clamped	18	12	8	—	—	8
— low noise	8	8	8	—	—	—
Total	148	112	68	83	46	25
Large NPN — $I_c \leq 100$ mA	—	—	2	2	2	2
— $I_c \leq 300$ mA	4	4	—	—	—	—
Total	4	4	2	2	2	2
Lateral PNP — split collectors (2)	36	24	16	26	14	9
— multiple collectors (6)	13	10	4	—	—	—
Total	49	34	20	26	14	9
Zener Diode	4	4	4	1	1	1
Large Diode	2	2	—	—	—	—
PASSIVE COMPONENTS						
Junction Capacitor — 75 pF capacitors	4	4	4	3	3	—
— 56 pF capacitors	—	—	—	—	—	3
Total	4	4	4	3	3	3
Various P - Diffused Resistors (total resistance)	1000 K	670 K	340 K	450 K	240 K	170 K
40 K Pinch Resistors	28	28	20	10	8	6
BONDING PADS						
	40	32	24	24	18	14
CHIP SIZE (mils)						
	150 × 144	151 × 111	92 × 111	127 × 94	78 × 94	56 × 91

Complete data and applications information is available. Call us toll-free 1-800-263-9353.

GENNUM CORPORATION P.O. Box 489, Sta. A, Burlington, Ontario, Canada L7R 3Y3 Tel: (416) 632-2996 Telex: 061-8525 Fax: 416-632-2055  
— an LTI Company —





# GigaBit Logic

## GaAs STANDARD CELL LIBRARY

### DISTINCTIVE CAPABILITIES

- Automated GaAs circuit design
- Wide selection of pre-designed cells
- Optimized for 1 - 2 GHz operation
- Low power dissipation of 1-2 mW per gate
- Typical loaded gate delays of 50 - 150 ps
- Configured for auto place and route
- Guaranteed AC and DC specifications
- Production proven process technology
- ECL, TTL and CMOS I/O capability
- Circuit complexities to 5K gates
- 0°C to +85°C operating temperature range
- Military temperature range available
- Superior radiation tolerance
- Packaging and test support included

### PROGRAM DESCRIPTION

GigaBit Logic's SC1 Gallium Arsenide Standard Cell Library contains a variety of pre-designed, pre-characterized subcircuits (cells) which provide an automated and straightforward approach to high speed, low power integrated circuit design. The cell library software from GigaBit is supported on merchant CAD workstations.

The cells are based upon GigaBit's production proven Gallium Arsenide metal-semiconductor field effect transistor (MESFET) process and follow the ECL I/O standards and GaAs power supply voltages established by the PicoLogic™ family of standard GaAs components. Each cell has been optimized to offer ultra-fast operation at minimum power levels.

Standard cell design techniques offer the performance, design flexibility and low production costs normally associated with full custom design while, at the same time, minimizing development time, cost and risk. The front end design implementation is identical to a gate array approach, however, unlike gate arrays, standard cell designs use only those cells and interconnections actually needed to complete the design, resulting in higher performance, smaller die sizes and lower power dissipation.

First time standard cell customers are invited to host a full day training seminar at their location. The cost of the session is included in the cell library package when purchased from GigaBit.

Prototype devices are tested for functionality utilizing customer generated test vectors. High speed performance is tested to the customer's specification by GigaBit and guaranteed over temperature. Volume production is supported.

### DESIGN KIT

- Standard Cell Library Software
- Comprehensive Design Manual
- Detailed Cell Datasheets
- Full Day on-Location Training Course
- Design and Applications Support

### SC1 STANDARD CELL REFERENCE GUIDE

CELL NAME	FUNCTIONAL DESCRIPTION	TpLH/TpHL (ps) F.O.=1	CLOCK FREQ.	POWER (mW)
<b>I/O CELLS</b>				
BICB	ECL DIFF. INPUT (COMPL. OUTPUTS)	104/83		35.2
BII	ECL INVERTING INPUT BUFFER	92/41		8.3
BIICK	ECL INVERTING CLOCK BUFFER	125/46		41.6
BIIT	TTL INVERTING INPUT BUFFER	80/33		7.5
BINR	ECL 3 INPUT NOR GATE	136/56		13.1
BOI	ECL INVERTING OUTPUT BUFFER	106/85		21.4
<b>SSI CELLS</b>				
AOI	TWO INPUT AND-OR-INVERT	93/61		2.8
FDC	D FLIP FLOP WITH COMPL. INPUTS		1.0 GHz	10.7
FDRH	D FLIP FLOP (RESET & OUTPUT ENABLE)		1.6 GHz	22.6
FDRHM2	DUAL INPUT D FLIP FLOP		1.6 GHz	22.6
IV	INVERTER	89/48		1.9
IVB	INVERTER BUFFER	75/35		2.3
ND2	TWO INPUT NAND GATE	93/53		2.5
NIV	NON-INVERTING BUFFER	18/9		11.2
NR2	2 INPUT NOR GATE	105/52		2.0
NR2B	2 INPUT NOR GATE BUFFER	90/39		2.3
NR3	3 INPUT NOR GATE	120/57		2.0
NR4	4 INPUT NOR GATE	134/60		2.0
NR5	5 INPUT NOR GATE	143/64		2.1
XX2	2 INPUT EXCLUSIVE NOR GATE	132/130		4.2
XO2	2 INPUT EXCLUSIVE OR GATE	132/131		6.8
<b>MSI CELLS</b>				
ACC2	2 BIT ACCUMULATOR		1.1 GHz	50
CPG1	CLOCK PULSE GENERATOR			40
DEC38	3 TO 8 DECODER	244/255		112
DIFF1	DIFFERENTIAL LINE DRIVER	100/100		10
DIV2	DIVIDE BY 2 PRESCALER		2.3 GHz	50
FDC2	D FF (COMPL. INPUTS, PRESET, CLEAR)		2.0 GHz	50
FDM2	D FLIP FLOP WITH MULTIPLEXED INPUTS		1.6 GHz	50
LD1	D TYPE LATCH ELEMENT	204/109		5
MD89	DIVIDE BY 8/9 PRESCALER		800 MHz	65
MUX4	4 TO 1 MULTIPLEXER	400/400		74
PDF1	PHASE FREQUENCY DETECTOR		500 MHz	
SYNC4	4 BIT SYNCHRONOUS COUNTER		1.0 GHz	100

### TYPICAL GIGABIT MILESTONES

- CIRCUIT LAYOUT: 4 to 8 weeks
- BACK-ANNOTATED SIMULATION: 2 to 4 weeks
- MASK SET: 2 weeks
- FABRICATION: 6 to 8 weeks
- ASSEMBLY AND TEST: 2 to 4 weeks
- DELIVERY OF FINAL PROTOTYPES: 16 to 26 weeks after receipt of schematic

### CUSTOMERS TRANSFERS TO GIGABIT

- VERIFIED NETLIST
- DEVICE FUNCTIONAL DESCRIPTION
- PRELIMINARY FLOORPLAN
- SUGGESTED PINOUT
- FUNCTIONAL TEST VECTORS
- SIMULATION FILES
- DEVICE TIMING SPECIFICATIONS





# GigaBit Logic

## GALLIUM ARSENIDE FOUNDRY SERVICES

### DISTINCTIVE CAPABILITIES

- Enhancement/Depletion mode processes
- High yield DSW lithography
- Fully implanted active layers
- All "dry" processing - 1 $\mu$ m design rules
- Sputtered/plasma CVD thin films
- Planar metal and via interconnects
- Two level metal interconnect standard
- Three level metal interconnect available
- 3 inch LEC GaAs wafers
- Proven high volume production
- Demonstrated yield and reliability
- Typical gate delays of 50 to 150 ps
- Digital logic to 4 GHz
- Static RAM and ROM to 1 ns access time
- Analog/RF to 5 GHz
- Proprietary SPICE models

### AVAILABLE SERVICES

- Individualized design training seminars
- Technology transfer includes design rules, SPICE models, and process description
- CAD support services: SPICE and logic simulation, DRC, ERC, and LVS
- Mask set composition and generation
- Prototype or production wafer runs
- Wafer saw and die processing
- Die assembly in JEDEC outline 40 and 68 pin high speed packages
- Functional and DC parametric test on die or packaged units
- Reliability testing and environmental screening facilities
- Ingot qualification services
- Silicon Nitride wafer capping service

### PROGRAM SUMMARY

For high speed integrated circuit applications well above the maximum frequency range of silicon bipolar IC's, GigaBit Logic's one micron (1 $\mu$ m) depletion or enhancement/depletion mode MESFET gallium arsenide (GaAs) processes are ideal.

GigaBit's state-of-the-art GaAs wafer processing technology utilizes the most advanced equipment in an ultra-clean Class 10 environment. High volume standard device production experience allows GigaBit customers to take advantage of rapid improvements in both yield and performance. In-house training seminars by GigaBit experts enable customers to quickly move up the GaAs IC design learning curve.

More than just a foundry service, GigaBit is a complete IC company offering design, development, manufacturing, testing, and reliability services in a commercial production environment.

Complete testing and packaging facilities support GigaBit's volume shipments of standard and custom products.

### AVAILABLE PROCESSES

- Depletion mode MESFET (D-mode)
- Low Power Depletion mode MESFET (LPD)
- High Margin Enhancement/Depletion mode MESFET (HME/D)
- Enhancement/Depletion mode MESFET (E/D)

#### TYPICAL DEVICE PERFORMANCE PARAMETERS

DEVICE PARAMETER	PROCESS:	D-MODE	LPD	HME/D		E/D	
	FET TYPE:	D-MESFET	D-MESFET	E/D	D	E	D
Pinchoff Voltage, Vp (Volts) (note 1)		-0.6, -1.0 (note 2)	-0.5	-0.25	-0.6	+0.15	-0.5
Current (Vds = 2.5V)							
IDSS (mA/50μm) (Vgs=0V)		2.0, 5.0	2.2	---	2.8	----	2.2
IDS (mA /50μm) (Vgs=0.6V)		---	8	5.6	9	2.2	8
Ke-value (external) (μA/V <sup>2</sup> *μm) (note 3)		115, 105	145	165	140	195	145
Transconductance (external)							
Gme (mS/mm), Vgs=0V		125, 155	140	---	160	----	140
Gme (mS/mm), Vgs=0.6V		---	245	235	255	180	245
SPICE Parameters (note 4)							
Ki (internal) (μA/V <sup>2</sup> * μm)		150, 145	220	225	200	320	220
Source Resistance, Rs (Ω*μm)		2000, 1750	1150	1300	1050	1500	1150
f <sub>T</sub> (GHz)		>15	>18	>18	>18	>18	>18
Peak current gain-bandwidth product							
Gate Length (μm)		<1.0	<1.0	<1.0	<1.0	<1.0	<1.0
Number of Masks Levels		9	9	11	11		

- Notes:
1.  $V_p$  is analogous to  $V_{TO}$  in the SPICE JFET model.
  2. D-mode pinchoff voltage can be customer specified from -0.6V to -1.0V.
  3.  $K_e$  is useful for estimating  $I_{ds} = K_e (V_{gs(EXT)} - V_p)^2$ ; it is lower than the  $K_i$  (or SPICE BETA) value because of source resistance degeneration.
  4.  $K_i$  is analogous to BETA and  $R_s$  to  $R_S$  and  $R_D$  in the SPICE JFET model.

### CUSTOM DESIGN KIT

- Extensively documented design rules
- Fully correlated SPICE models
- PCM test patterns and specifications
- One full day training included
- Optional extended training seminar

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**GoldStar**  
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**SEMI-CUSTOM IC**

ASICs/CUSTOM

Gold Star Semiconductor

## CMOS GATE ARRAY

### • GCL3000 Series

Device Number	Gate Count	% Max AUR <sup>7</sup>	Max <sup>3</sup> I/O	V <sub>DD</sub> Pads	V <sub>SS</sub> Pads	V <sub>SS2</sub> Pads	Max Pads	Gate Speed (ns) <sup>1</sup>	
								Typ	Max <sup>2</sup>
GCL3020	272	95	32	1	3	0	36	5.0	9.0
GCL3030	342	95	36	1	3	0	40	5.0	9.0
GCL3040	420	90	40	1	3	0	44	5.0	9.0
GCL3060	600	90	48	1	3	0	52	5.0	9.0
GCL3080	812	90	56	1	3	0	60	5.0	9.0
GCL3110	1056	85	64	1	3	0	68	5.0	9.0
GCL3130	1332	85	72	1	3	0	76	5.0	9.0
GCL3170	1722	85	82	1	3	0	86	5.0	9.0
GCL3210	2162	80	92	1	3	0	96	5.0	9.0
GCL3250	2550	80	100	1	3	0	104	5.0	9.0

### • GCL5000 Series

Device Number	Gate Count	% Max AUR <sup>7</sup>	Max <sup>3</sup> I/O	V <sub>DD</sub> Pads	V <sub>SS</sub> Pads	V <sub>SS2</sub> Pads	Max Pads	Gate Speed (ns) <sup>1</sup>	
								Typ	Max <sup>2</sup>
GCL5080	880	90	66	2	4	2	74	2.5	4.5
GCL5140	1404	90	84	2	4	2	92	2.5	4.5
GCL5220	2224	90	106	2	4	2	114	2.5	4.5
GCL5320	3192	85	130	2	4	2	138	2.5	4.5
GCL5420	4202	85	144	4	4	4	156	2.5	4.5
GCL5600	5902	80	168	4	4	4	180	2.5	4.5

### • GCL7000 Series

Device Number	Gate Count	% Max AUR <sup>7</sup>	Max Pads		Max I/O Pads <sup>3</sup>		Max Package Pins <sup>5</sup>		Gate Speed <sup>1</sup>	
			Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic	Type	Max <sup>2</sup>
GCL7080	880	90	52	68	44	60	52	68	1.4	2.4
GCL7140	1443	90	66	86	58	78	66	86	1.4	2.4
GCL7220	2224	85	78	106	70	98	80	106	1.4	2.4
GCL7320	3192	85	96	128	80	112	96	128	1.4	2.4
GCL7420	4242	85	114	150	98	134	114	150	1.4	2.4
GCL7600	6072	80	138	186	122	170 <sup>6</sup>	138	180 <sup>4</sup>	1.4	2.4
GCL7840	8370	80	166	222	150	204 <sup>6</sup>	166	180 <sup>4</sup>	1.4	2.4
GCL71000	10013	70	174	232	158	212 <sup>6</sup>	174	180 <sup>4</sup>	1.4	2.4

- Notes: 1. 2-input NAND gate, fanout=2, and statistically necessary interconnection  
2. T<sub>A</sub>=0 to 70°C, V<sub>DD</sub>=5V±5%  
3. It may be necessary to configure additional I/O pads for V<sub>DD</sub> and V<sub>SS</sub> depending on the number and drive of the output buffers.  
4. Limited by the largest package currently available.  
5. Due to the present limitations in available bonding technology for 2-micron based products, GSS recommends that all 7000 series designs be configured for use in plastic packages. This will permit upward compatibility to ceramic packages from plastic, where required for extended temperature range.  
6. May be limited to 160 pins due to tester capability.  
7. Maximum array usage recommended

### Package families include;

- Plastic DIPs: 16,20,22,24,28,40,48 and 64 leads
- Ceramic DIPs (Side Braze): 16,20,22,24,28,40,48 and 64 leads
- Ceramic DIPs (CerDIP): 20,24,28 and 40 leads other packages can be made available on special order.
- Ceramic Pin-Grid Arrays: 64,68,84 and 124 leads
- Ceramic Chip Carriers: 24,28,36,40,44,52,68, and 84 leads
- Plastic Chip Carriers: 28,32,44,52,68 and 84 leads

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**GS**





## HCMOS STANDARD CELL

### — GENERAL DESCRIPTION

GS Standard Cell Library provides high-performance, cost effective design solutions for integrating a variety of system functions on a single chip. High complexity memory and basic logic can all be combined on the same device. The result is a circuit which approaches full-custom in performance and price, but at greatly reduced development time and cost. GS's advanced and proven CAD system software tools and design procedures virtually eliminated errors and takes the worry out of Semicustom design. Applications in which GS devices are found include low and mid-priced peripherals, telecommunications systems including modems and data concentrators, audio, image processing and security systems.

GS logic cells are fabricated using 1.5 micron and 2 micron HCMOS process technology with two-level metal interconnection. This provides superior AC performance and significant reduction in die size. Circuit performance is enhanced by routing through the dual layers of metal, thereby eliminating the skew introduced by using polysilicon. Careful attention has been paid to ratioing the P-channel devices to be approximately twice the size to the N-channel devices which effectively compensates for the difference in carrier mobility between the two. The net result is a circuit with a more symmetrical rise and fall time, a higher toggle rate, and which behaves more predictably.

### — FEATURES

- Up to 50,000 Equivalent Gates
- Allows up to 200 MHz Toggle Rates
- RAM and ROM Functions Available
- Ratioed "N" and "P" Devices Minimize Pulse Skew
- Full Simulation Capabilities
- Cell Compaction Software Reduces Die Size and Increases Yield
- Wide Range of Packaging Options

### — PRODUCT DESCRIPTION

GSC 2000 SERIES	GSC 4000 SERIES	GSC 6000 SERIES
<p>Silicon gate 2 micron (drawn) Twin-tub HCMOS technology.</p> <p>Dual layer metal interconnection.</p> <p>Propagation delay of 1.2 ns through a 2-input NAND gate, <math>T_A=25^{\circ}\text{C}</math>, fanout=1 <math>V_{DD}=5\text{V}</math>.</p> <p>Digital, RAM and ROM function on a single chip.</p> <p>Up to 20,000 equivalent gates.</p> <p>Allows 100 MHz toggle rate.</p> <p>Output drive up to 10 mA.</p> <p>Ratioed "N" and "P" devices minimize pulse skew.</p> <p>100% auto place and route.</p> <p>Proprietary software reduces die size and increases yield.</p> <p>All inputs and outputs protected from over voltage and latch-up</p>	<p>Silicon gate 2 micron (drawn) enhanced Twin-tub HCMOS technology.</p> <p>Dual layer metal interconnection.</p> <p>Propagation delay of 1.0 ns through a 2-input NAND gate, <math>T_A=25^{\circ}\text{C}</math>, fanout=1 <math>V_{DD}=5\text{V}</math>.</p> <p>Digital, RAM and ROM functions on a single chip.</p> <p>Up to 30,000 equivalent gates.</p> <p>Allows 150 MHz toggle rate.</p> <p>Output drive up to 12 mA.</p> <p>Ratioed "N" and "P" devices minimize pulse skew.</p> <p>100% auto place and route.</p> <p>Proprietary software reduces die size and increases yield.</p> <p>All inputs and outputs protected from over voltage and latch-up.</p>	<p>Silicon gate 1.5 micron (drawn) n-well HCMOS technology.</p> <p>Dual layer metal interconnection.</p> <p>Propagation delay of 0.7 ns through a 2-input NAND gate, <math>T_A=25^{\circ}\text{C}</math>, fanout=1 <math>V_{DD}=5\text{V}</math>.</p> <p>Digital, RAM and ROM functions on a single chip.</p> <p>Up to 50,000 equivalent gates.</p> <p>Allows 200 MHz toggle rate.</p> <p>Output drive up to 16 mA.</p> <p>Ratioed "N" and "P" devices minimize pulse skew.</p> <p>100% auto place and route.</p> <p>Proprietary software reduces die size and increases yield.</p> <p>All inputs and outputs protected from over voltages and latch-up.</p>

### — DESIGN LIBRARY

#### BASIC CELL

- Inverters
- 2,3,4-Inputs NANDs and ANDs
- 2,3,4-Inputs NORs and ORs
- Exclusive ORs and NORs
- AND-OR-INVERT Gates
- "D" Flip-Flops and Latches
- D F/F with Set and Reset
- J-K Flip-Flops
- R-S Latches

#### MACROFUNCTIONS

- Adder-Subtractor
- UP-DOWN Counters
- Presettable Up-Down Counters
- Dual 4-Bit shift Registers
- 4 Bit ALU Cell

#### MEMORY LIBRARY

- \* RAM
  - 4 wordsX4 bits
  - 8 wordsX8 bits
  - 16 wordsX4 bits
  - 16 wordsX8 bits
  - 16 wordsX16 bits
  - 32 wordsX8 bits
  - 32 wordsX16 bits
  - 64 wordsX8 bits
  - 64 wordsX16 bits
  - 128 wordsX8 bits
- \* ROM
  - 128 wordsX3 bits
  - 256 wordsX8 bits
  - 256 wordsX16 bits
  - 256 wordsX32 bits
  - 512 wordsX8 bits
  - 512 wordsX16 bits
  - 512 wordsX16 bits
  - 1024 wordsX8 bits
  - 1024 wordsX16 bits

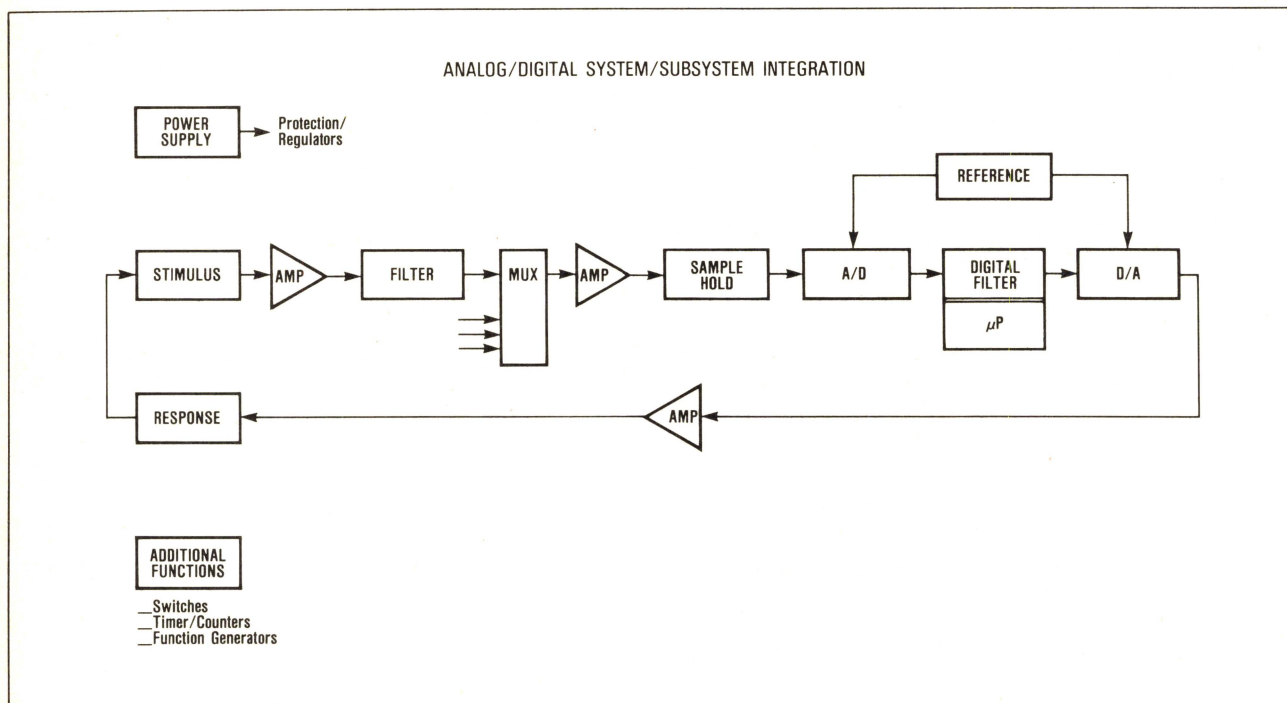
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- EXPERT ASIC™ family of cell compilers and services provides customized circuits without compromises
- More than 10 years experience with complex single chip A/D integration for communications, automotive and industrial applications
- Over 200 digital standard cells
- Bit-slice microprocessor megacells
- RAM, ROM and PLA megacell generators
- Over 20 Analog megacells include:
  - 8 bit D/A converter
  - 8 bit A/D converter
  - Band gap voltage reference
  - Analog input buffer/sample hold
  - Analog output buffer/sample hold
  - Input operational amplifier
- Analog cell generators create custom switched capacitor filters and op amps in just hours

## Analog/Digital Integration



Gould provides total system/subsystem integration. In addition to analog and digital building blocks, Gould provides the analog "glue" that holds the system/subsystem together—from stimulus to response.

**For complete technical databooks and further information call (408) 554-2311 or check the IC Master manufacturers/distributors directory for the office nearest you.**



### CMOS Programmable Logic Devices

- CMOS EEPROM technology for low power and high speed
- Re-programmability gives convenience and flexibility
- Ideal for low gate density and low development cost requirements

### CMOS Gate Arrays

- CMOS 2-micron and 1.2 micron families
- Over 200 7400 TTL soft cells for easy designs with familiar functions
- Gould's GATE GOBBLER™ service optimizes your design by reducing gate count, without affecting function or performance
- NETTRANS™ netlist translator service gives you an alternate source for circuits previously designed in other formats

### Gould Gate Array Configurations

2μ Double Metal Family Part No.	Equivalent 2-Input Gates	Total Pads	General I/O	Power Only
GB-1000D	1120	68	60	8
GB-2000D	2128	84	76	8
GB-3000D	3264	104	96	12
GB-4000D	4256	120	108	12
GB-6000D	5880	144	132	12
GB-8000D	7872	184	168	16
GB-10000D	9776	208	192	16

1.2μ Double Metal Family	2-Input Gate		Total Pads	General I/O	Power Only
	Total Available	Usable			
GC5000	5280	2240	62	50	12
GC7500	7488	3456	86	64	12
GC10000	10320	4128	84	72	12
GC15000	15000	5970	96	84	12
GC20000	19840	7960	112	100	12
GC25000	25344	10560	124	112	12
GC30000	30000	12000	130	118	12
GC35000	38976	14016	150	138	12

### Macrocell Gate Delay

Gate		2.0μ	1.2μ
Internal Gate Delay	typ	1.0 ns	0.5
D-Type Flip Flop Toggle Freq		50 Mhz	100 Mhz
Input Buffer	typ	2.3	1.8
Output Buffer (50 pf Load)	typ	5.0	4.0 ns

Conditions:  $V_{DD} = 5$  Volts,  $T_A = 25^\circ$ . Typical Process Parameters  
 F.O. = 2 + 40 Mils At Interconnect (Unless Specified)



## APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASIC)

### The Harris ASIC Commitment

Provide a single graphics interface for today's designer that ties together many design tools, operates in a single framework, is capable of accessing multiple technology libraries, and operates on multiple UNIX 68XXX-based platforms.

Harris Semiconductor, a leader in custom micro-electronic products for over two decades, is firmly established in the ASIC market and now brings the designer a combination of state-of-the-art proven process technologies and the most widely used and efficient designs systems in the industry.

### The Harris Trackrecord

Harris ASIC customers benefit from the experience, resources and stability of a major IC manufacturer. Harris Semiconductor is presently the eighth largest merchant semiconductor supplier in the United States and is widely considered the foremost manufacturer of radiation hardened and dielectrically isolated (DI) devices. Harris introduced the world's first low power CMOS versions of the 8086, 8088, and 80286 microprocessors. Harris is well known for its high performance, high reliability analog ICs which are used in the world's most demanding systems.

### The Harris Design Libraries

In addition to working with a full capability semiconductor vendor, the Harris ASIC customer gains full access to our semiconductor design tools, libraries, databases, and process technologies. Libraries include standard cell CMOS, bipolar DI, radiation-hardened, and gallium arsenide. Harris libraries are available through designer use of Daisy™, Mentor™, SDA™, or FutureNet™ software. Of course, design migration from one library to another is always available.

### Standard Cell CMOS library Group:

Included in this group are 2.5 micron, 2.0 micron and 2.0 micron "hard field" double level metal (DLM) libraries. For military applications, class S and rad-hard designs are available. When a design is done in one library, it can be easily migrated to another library whenever necessary. The powerful Harris FORCE (FORTH Optimized RISC Computing Engine) core cell and peripherals are available in this library group.

### Bipolar DI Library:

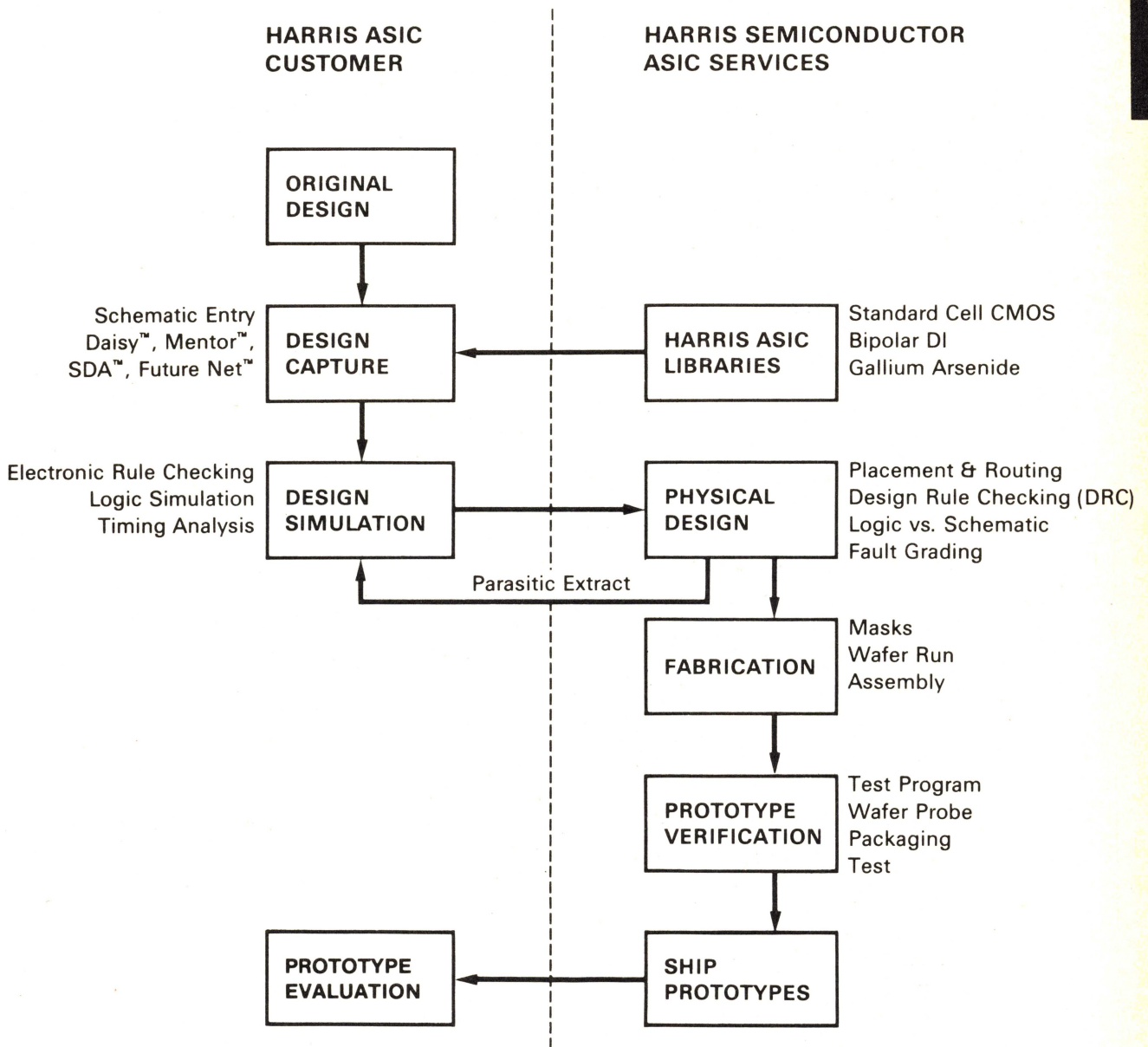
Harris is the world's leader in dielectrically isolated (DI) IC processing — years of linear design experience and leadership is made available to designers who can take full advantage of the same tools and processes used to manufacture Harris' exemplary low noise, high speed circuits. The design system is highly integrated, with SPICE (industry standard circuit simulator) capability. Designers can mix n-p-n and p-n-p transistors in the same circuit.

### Gallium Arsenide Library:

The Harris Microwave Standard Cell (HMS) library is a broad and growing collection of predefined standard cell — consisting of basic logic functions, gates, and appropriate I/O circuitry. Each is fully characterized to support custom placement, routing and simulation of your circuit design.



# ASIC DESIGN FLOW



# Standard Cell

HSC 250 CMOS Cell Library

September 1987

## Features

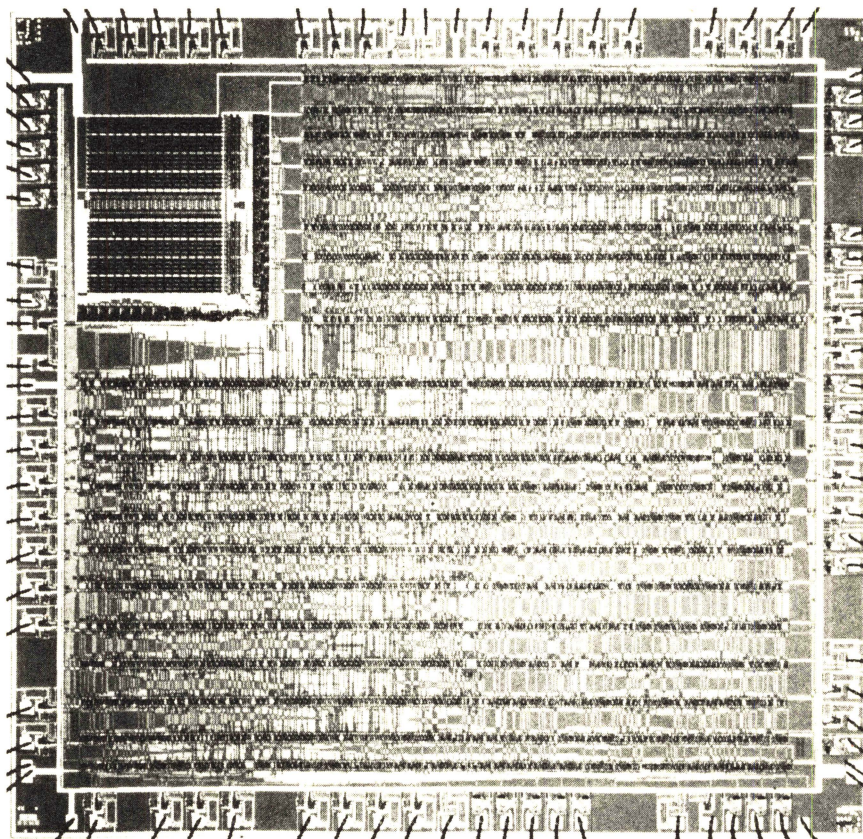
- 1.5 Micron Effective Channel Length, 2-Layer Metal CMOS
- 1.2ns Typical Gate Delay Through 2-Input NAND
- Up to 100MHz Flip-Flop Toggle Rate
- Over 200 Primitive and Macrocell Functions
- Complex Function Megacells
- Customer Definable RAM and ROM
- Supported on Multiple CAE Platforms
- CMOS/TTL Compatible I/O's
- Commercial-Industrial-Military Temperature Ranges
- Proven Reliable and Manufacturable Process
- Extensive Range of Packaging Options
- Minimum 4kV ESD Protection
- Screening and Qualification to Mil-Std-883 Method 5004/5005, Class B
- Fully Compatible with the HSC200-RH Rad-Hard Library

## Description

The HSC 250 STANDARD CELL LIBRARY is a proven, high performance dual-level metal library. The library offers a broad range of predesigned and fully characterized cells,

macros, complex megacells and compilable RAM and ROM for developing reliable, cost effective customer specific IC's.

## Die Photo





## HSC250 CMOS Standard Cell Library

### Complex Function Megacells

To enhance the level of system integration, and reduce the design cycle time Harris has developed a series of complex function megacells. These functions consist of a family of

highly integrated microprocessor peripherals, communication elements, high performance multipliers, and bit slice elements. A list of the available megacells follows:

#### • Microprocessor Peripherals

82C37A .....	DMA Controller
82C50A .....	Asynchronous Communication Element
82C50B .....	Asynchronous Communication Element
82C52 .....	UART/BRG
82C54 .....	Programmable Interval Timer
82C55A .....	Programmable Peripheral Interface
82C59A .....	Priority Interrupt Controller
82C84A .....	Clock Generator
82C88 .....	Bus Controller

#### • Communication Elements

HD4702 .....	Programmable Bit Rate Generator
HD6402 .....	UART
HD6406 .....	UART/BRG/Modem Control
HD6408 .....	ASMA
HD6409 .....	Manchester Encoder/Decoder
HD15530 .....	Manchester Encoder/Decoder
HD15531 .....	Programmable Manchester Encoder/Decoder

#### • Other Functions

H2901 .....	4-Bit Slice ALU
*HMU16, HMU17, HMU18 .....	16 x 16 Multipliers
**HMU1010 .....	16 x 16 Multipliers/Accumulator

### Compilable Cells

Harris has further expanded user definability by providing high performance, module compilation. This capability allows

the customer to quickly generate design specific RAM and ROM cells.

RAM .....	Compilable to 16K
ROM .....	Compilable to 64K

\*Contact Factory for availability

\*\*Available Q1, CY'88

# Design Interface with Harris C1CD

Recent advances in design automation tools have allowed users of custom and semicustom integrated circuits to become involved in the design of their chips, utilizing the silicon vendor only as a manufacturing facility, or "foundry", to fabricate the devices with little or no knowledge of the function of the circuit designed by the customer.

Although Harris has the engineering staff to implement customer designs given only a functional description or logic diagram and test vectors (and prefers to do this for bipolar designs), we certainly recognize the benefits to the customer by participation in the design process. Harris encourages this, and is willing to provide documentation, tools, design centers and training to enable customers to participate in the design process at the level of detail with which they feel comfortable.

Customers may elect to implement IC designs in a variety of ways including:

- Standard cell design using Harris cell libraries
- Full custom design to Harris layout rules
- Transfer to Harris of a complete IC layout which is compatible with Harris layout rules and processes

Regardless of the implementation technique chosen, the preferred division of responsibilities for a customer/foundry relationship is as follows:

## Customer Responsibilities

- Design capture
- Simulation
- Design for testability
- Package selection
- Critical path analysis
- ERC checks
- Test vector generation

- Negotiable
  - Layout for packaging considerations
  - Overall layout
  - Test program generation
  - DRC checks
  - Testing
  - Packaging/assembly
  - Screening

## Harris Responsibilities

- Providing accurate, complete and understandable process performance, cell library and design rule information
- Definition of expected design transfer format
- Design limits (number of pins, tester limitations, die size, etc.)
- Updates as required for cell or process information
- Mask manufacture
- Wafer fabrication

## Workstation Support

Workstation support is available for Harris cell libraries on Daisy and Mentor workstations, and SDA (Silicon Design Automation software). Silicon Compiler Systems design tools are supported for some processes and other tool interfaces are being developed. Please contact the factory or your local sales office to discuss your workstation interface needs.

## Harris CMOS Foundry / Semicustom Process Summaries

### DIGITAL CMOS

PROCESS	L <sub>drawn</sub> N/P (MICRONS)	L <sub>eff</sub> N/P (MICRONS)	CONTACT SIZE (MICRONS)	METAL PITCH		POLY PITCH		BVN TYP (VOLTS)	BVP TYP (VOLTS)	V <sub>t</sub> field N/P (VOLTS)	CELL LIBRARY SUPPORT	*RAD- HARD OPTION
				METAL 1 (MICRONS)	METAL 2 (MICRONS)	POLY 1 (MICRONS)	POLY 2 (MICRONS)					
SAJI I	3/4	2.0/3.2	5 x 5	12 (6.6)	N/A	10 (5.5)	12.5 (5.75)	22	20	13/8	No	Yes
SAJI IV	2.5/3.0	1.8/2.2	2 x 2	8 (5.3)	N/A	8 (4.4)	N/A	22	16	20/15	Yes	Yes
Scaled SAJI IV	2.5/3.0	1.5/2.7	3 x 3	8 (4.4)	N/A	6.5 (3.35)	N/A	14	14	18/20	Yes	Yes
SAJI VH	2.0/2.5	1.35/1.85	2 x 2	5.0 (3.2)	8.0 (5.5, 2.5)	5.0 (2.0, 3.0)	N/A	8.0	8.0	25/8	Yes	Yes
RH7	1.2/1.2	1.0/1.0	1.2 x 1.2	3.6 (1.8, 1.8)	3.8 (2.0, 1.8)	2.6 (1.2, 1.4)	N/A	9.0	9.0	22/27	Future	Yes

### APPLICATIONS

- Satellites
- Industrial controls
- Memories
- Telecommunications
- Nuclear reactor controls
- Computers
- Interface circuits
- Digital Processing
- Data communications
- Military (Custom and semicustom cell library)



## Harris Bipolar Digital Process Summary

### BIPOLAR DIGITAL

PROCESS	COMPLEXITY	SPEED	OUTPUT DRIVE	RAD-HARD OPTION	APPLICATION
Dielectric Isolation and Junction Isolation Low Power Schottky (LPSTTL)	400 gates/chip	6ns/gate	4mA	Yes	<ul style="list-style-type: none"> <li>Digital gates</li> <li>MSI memories</li> <li>PROMs</li> </ul>
Dielectric Isolation Advanced Schottky (LPSTTL)	1000 gates/chip	6ns/gate	8mA	Yes	<ul style="list-style-type: none"> <li>Static RAMs</li> <li>LSI logic</li> <li>MPU peripherals</li> </ul>
Dielectric Isolation Interface	—	Application dependent	100mA	No	<ul style="list-style-type: none"> <li>Line drivers</li> <li>Line receivers</li> <li>ARINC 429 driver</li> </ul>

## Harris Bipolar Linear Process Summary

### BIPOLAR LINEAR

PROCESS	TYPE	h <sub>fe</sub>		F <sub>T</sub> (MHz)		BV <sub>CEO</sub>		RAD-HARD OPTION	APPLICATIONS
		NPN	PNP	NPN	PNP	NPN	PNP		
Junction Isolation	—	150	50	300	2	40	40	No	<ul style="list-style-type: none"> <li>Low-to-medium frequency amplifiers</li> <li>Low speed, non-saturated logic</li> </ul>
Dielectric Isolation	Switching NPN	50	—	500	—	75	—	Yes	<ul style="list-style-type: none"> <li>Mixed digital/analog switching</li> <li>Sense amplifiers</li> <li>Line drivers</li> <li>Line receivers</li> </ul>
Dielectric Isolation	Bi FET*	150	100	600	300	40	40	Yes	<ul style="list-style-type: none"> <li>Analog switches</li> <li>Operational amplifiers</li> <li>Sample-and-holds</li> </ul>
Dielectric Isolation	High Frequency	150	100	600	300	40	40	Yes	<ul style="list-style-type: none"> <li>High-frequency amplifiers</li> <li>Rad-hard amplifiers</li> <li>Comparators</li> </ul>
Dielectric Isolation	High Current	150	100	500	250	40	40	Yes	<ul style="list-style-type: none"> <li>Power relay drivers</li> <li>Clock drivers</li> <li>Voltage regulators</li> </ul>
Dielectric Isolation	High Voltage	225	50	200	25	100	90	Yes	<ul style="list-style-type: none"> <li>High-voltage amplifiers</li> </ul>
Dielectric Isolation	CMOS/Bipolar	150	100	600	300	35†	35**	Yes	<ul style="list-style-type: none"> <li>Analog switches</li> <li>High-performance amplifiers</li> <li>Data conversion</li> <li>Pin diode driver</li> </ul>
Dielectric Isolation	NPN Schottky	50	—	500	—	8	—	Yes	<ul style="list-style-type: none"> <li>Flash converters</li> <li>Sense amplifiers</li> </ul>
Dielectric Isolation	VHFP	100	100	1.5 GHz	1.0 GHz	15V	15V	Yes	<ul style="list-style-type: none"> <li>High speed amplifiers</li> <li>Mixed analog/digital</li> </ul>

\*V<sub>p</sub> = 1V to 2V, BV<sub>DSS</sub> = 40V

\*\*V<sub>TP</sub> = 1V to 3V, BV<sub>DSS</sub> = 40V

†V<sub>TN</sub> = 1V to 3V, BV<sub>DSS</sub> = 40V

## Harris CMOS Analog/Digital Standard Cells

This proven high-performance cell library uses the Harris Scaled Self Aligned Junction Isolated IV Analog process (S4A). Typical 25°C performance features of S4A include 5 ns/gate digital speed (FO=3)...9 mil<sup>2</sup> 2-input NAND area...1-10 MHz op amp bandwidth...and 300 mil<sup>2</sup> op amp area.

Cells include op amps, comparators, analog switches, voltage references and current generators. The library is optimized for moderate-complexity digital functions, including microprocessor interface, control, and combinational logic circuitry.

Important considerations of this cell library include:

- Bringing the advantages of integration to the analog world
- Reduced size of PCB—to lower system cost, material cost and weight

- Few components, fewer connections — lower system cost, lower assembly cost, increased reliability
- Integration eliminates chip-to-chip delays, allows addition of new functions
- Rad-hard cells in development
- Available now for custom development
- Proven cells reduce risk, layout time
- Low power - CMOS
- High performance
- CMOS and TTL compatible inputs and outputs
- Switched capacitor methods provide a wide variety of analog circuit functions.

### ANALOG/DIGITAL CMOS

PROCESS	L <sub>drawn</sub> N/P (MICRONS)	L <sub>eff</sub> N/P (MICRONS)	CONTACT SIZE (MICRONS)	METAL PITCH		POLY PITCH		BVN TYP (VOLTS)	BVP TYP (VOLTS)	V <sub>field</sub> N/P (VOLTS)	CELL LIBRARY SUPPORT	*RAD- HARD OPTION
				METAL 1 (MICRONS)	METAL 2 (MICRONS)	POLY 1 (MICRONS)	POLY 2 (MICRONS)					
SAJI IV Analog	4.0/5.0	2.2/2.7	3 x 3	9 (5, 4)	N/A	8 (4, 4)	8 (4, 4)	16	17	> 22	Yes	Future

### APPLICATIONS

- Mixed Analog/Digital
- Comparators
- Analog switches
- Voltage/current references
- Hybrid Conversion
- Op amps
- Oscillators
- Switched capacitor filter
- Voltage amplifiers

Information provided for process selection only. Further detailed information packages are available from Harris

Notes: N/A = Not Applicable. Interconnect = Pitch (width, space)

All Processes are P-well except Relaxed SAJI VII which is twin well. All N+ EPI on N- to provide latchup immunity

\*Rad-Hard option may change some parameters

Harris processes are designated SAJI (Self Aligned Junction Isolation)

## Mixed Digital And Analog Process Options

Due to the nature of unusual requirements presented by analog circuits, process options have been developed as "bolt-ons" to address specific performance needs.

This table summarizes some of the available process options for standard Harris processes.

### Harris Custom Process Options

BASIC PROCESS	OPTIONS									
	RESISTORS			FETs			SCHOTTKYS			MNOS
	I <sup>2</sup>	NiCr	POLY	N-JFET	P-JFET	MOS	PtSi	TiW	Al	
Complementary Bipolar DI	•	•		•	•	•				•
Bipolar Digital	•	•	•				•	•	•	•
Si Gate CMOS	•	•	•			•				•

## Rad-Hard Bipolar Linear/Digital Array (in development)

- Based on advanced Very High Frequency Process (VHFP)
- Complementary Dielectric Isolation process
- Produces transition frequency of NPN and PNP > 1 GHz
- Being developed for use in 8-channel pre-amp array for tactical missiles
- Radiation testing results show devices retain useful gain and frequency response after 3 x 10<sup>6</sup> rads (Si) and 3 x 10<sup>14</sup> n/cm<sup>2</sup>
- Digital circuits include fast ECL/EFL cells
- Demonstration vehicles: 8-bit A/D and sampled data signal processor



## EPIC : Extensive Possibilities for Integrated Circuits

HOLT INTEGRATED CIRCUITS.... THE RIGHT CHOICE FOR CUSTOM AND SEMI-CUSTOM CIRCUITS.

Holt has been designing and manufacturing analog/digital circuits for over ten years. Our new standard cell library makes customer designed integrated circuits a reality. The large selection of analog functional blocks are a real solution for turning PCB designs into monolithic circuits. Consider the (extensive) possibilities with these standard cells :

### ANALOG STANDARD CELLS :

- OPERATIONAL AMPLIFIERS  
LOW NOISE  
GENERAL PURPOSE  
SWITCHED CAPACITOR DEDICATED  
HIGH DRIVE FOR OFFCHIP LOADS
- OSCILLATORS  
VOLTAGE CONTROLLED OSCILLATORS  
LOW POWER CRYSTAL OSCILLATOR  
RC (TRIMMABLE) OSCILLATORS
- REFERENCE CIRCUITS  
REGULATORS  
BANDGAP REFERENCES  
PROGRAMMABLE CURRENT REFERENCE  
BINARY WEIGHTED CURRENT MIRRORS
- VOLTAGE CONVERSION CIRCUITS  
VOLTAGE DOUBLERS  
TRANSLATORS
- COMPILER CELLS  
USER SELECTABLE NMOS/PMOS SIZES  
USER SELECTABLE RESISTORS/CAPACITORS
- COMPARATORS

### DIGITAL STANDARD CELLS :

- GATE FUNCTIONS  
ANDS / NANDS / ORS / NORS - STANDARD DRIVE  
ANDS / NANDS / ORS / NORS - HIGH DRIVE  
XORS / XNORS ... COMPLEX A-O-I STRUCTURES  
BUFFERS / INVERTERS / CLOCK DRIVERS
- FLIP-FLOPS  
TOGGLE FLIP-FLOPS (WITH/WITHOUT RESET)  
D-TYPE FLIP-FLOPS (WITH/WITHOUT SET/RESET)  
J-K FLIP-FLOPS (RESETTABLE)
- SPECIAL FUNCTIONS  
CLOCK GENERATORS  
MAGNITUDE COMPARATORS  
ONE SHOTS  
COUNTERS (UP/DOWN, BINARY, PRESETTABLE)
- LATCHES
- MULTIPLEXERS
- DECODERS
- TTL COMPATIBLE INPUTS / OUTPUTS
- SELECTABLE DRIVE OUTPUTS

• AND MANY OTHERS

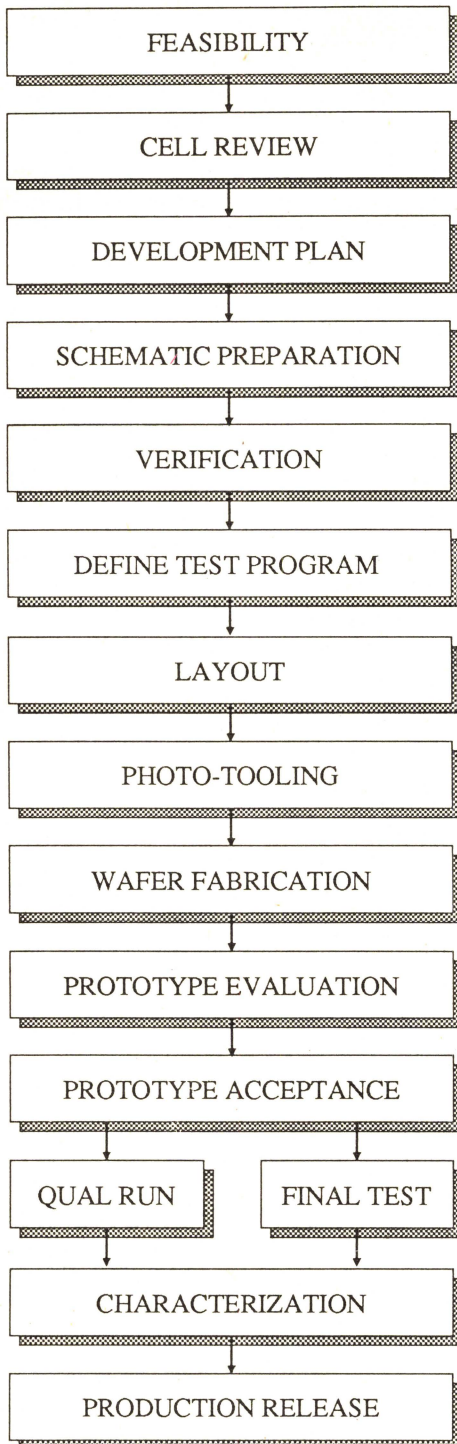
STANDARD EPIC FEATURES AND SPECIFICATIONS							
<ul style="list-style-type: none"> <li>• POWER-OFF INPUT ON ANALOG CELLS ( STATIC CURRENT &lt; 100NA .)</li> <li>• BUILT-IN LATCHUP IMMUNITY AND ESD PROTECTION</li> <li>• ADJUSTABLE BIAS CURRENTS IN OP-AMPS TO OPTIMIZE PERFORMANCE</li> <li>• EXTREMELY WIDE OPERATING RANGE ( TYPICALLY 1.5V TO 15 VOLT )</li> </ul>							
GENERAL PURPOSE OP-AMP						TTF	LOGIC
SUPPLY	IDD	BANDWIDTH	AOL	CMMR	ISINK	FMAX	DELAY
VDD=1.5	0.6 UA	60 KHz	112 dB	144 dB	.2 MA	9 MHz	29 NS
VDD=5.0	6.0 UA	200KHz	96 dB	120 dB	7 MA	20 MHz	4.8 NS
VDD=9.0	120 UA	800KHz	80 dB	93 dB	27 MA	39 MHz	2.9 NS
VDD=15	240 UA	1.6 MHz	76 dB	76 dB	80 MA		
CONDITIONS: 25 DEG. , 4-UM TECHNOLOGY, WORST-CASE PROCESSING							

## HOLT INTEGRATED CIRCUITS

9351 Jeronimo Road, Irvine, CA 92718

Contact : Roger Smith at (714) 859-8800 or (800) 222-HOLT





## HOLT DEVELOPMENT PROCESS

## WHY HOLT IS THE RIGHT SOURCE FROM FEASIBILITY TO PRODUCTION :

- 1) DEDICATED TO BECOMING THE LEADER IN GENERAL APPLICATION ASICS.
- 2) EXPERIENCE - PRESENT AND FUTURE CELLS EMBODY MORE THAN 10 YEARS EXPERTISE IN DEVELOPING AND PRODUCING HIGHLY COMPLEX ANALOG/DIGITAL MIXED MODE IC'S.
- 3) IN-HOUSE DESIGN, LAYOUT AND CAD, SIMULATION, WAFER-FAB, TEST, HIGH RELIABILITY QUALITY SCREENING, BURN-IN, AND PROTOTYPE PACKAGING.
- 4) PROVEN RELIABILITY THROUGH YEARS OF SERVICE TO BIO-MEDICAL MARKET.
- 5) EXPERIENCED IN HIGH VOLUME COMMERCIAL PRODUCTION AS WELL AS LOW VOLUME HI-REL.
- 6) STRONG LIBRARY OF STANDARD CELLS.
- 7) COOPERATIVE DESIGN APPROACH ALLOWS CUSTOMER CONTROL OF CRITICAL PATH PRIOR TO TOOLING.
- 8) COMPLETE CAD/CAE TOOLS.

## WHY HOLT'S CELL LIBRARY IS THE OPTIMUM CHOICE :

- 1) 4 MICRON DIGITAL CELLS WITH WIDE OPERATING RANGE (1V TO 10V).
- 2) 3 MICRON DIGITAL CELLS WITH TYPICAL FLIP-FLOP TOGGLE FREQUENCY OF 20MHz @5V.
- 3) 4 MICRON ANALOG CELLS WITH WIDE OPERATING RANGE (1V TO 15V).
- 4) 2000V ESD ON ALL INPUT/OUTPUT CELLS.
- 5) BUILT-IN LATCHUP PROTECTION.
- 6) GRID STRUCTURE DESIGNED FOR ERROR FREE LAYOUT. SIMPLE RULES MAKE CUSTOMER LAYOUT A REALITY.
- 7) COMPONENT CELLS ALLOW CREATION OF CUSTOM CIRCUITS BY CUSTOMER.
- 8) MANY SPECIAL FUNCTION CELLS (VOLTAGE DOUBLERS, OSCILLATORS, HIGH VOLTAGE DRIVERS, ETC).
- 9) CELLS DEDICATED TO SOLVE LOW POWER/MIXED MODE APPLICATIONS.

## HOLT INTEGRATED CIRCUITS

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Contact : Roger Smith at (714) 859-8800 or (800) 222-HOLT



# HI-8010

## CMOS HIGH VOLTAGE DISPLAY DRIVER

**HOLT**  
INC.  
INTEGRATED CIRCUITS

### General Description

The HI-8010 high voltage display driver is constructed of MOS P Channel and N Channel enhancement mode devices in a single monolithic structure. It is designed to drive high voltage Liquid Crystal Displays by converting low level input signals, such as TTL or CMOS to high voltage drive signals.

The chip can drive up to 38 segments of LCD and requires minimal display-to-data source interfacing. Data is loaded serially and held in internal latches until new display data is received.

The HI-8010 is available in ceramic or plastic DIP; leaded or leadless chip carriers; J-lead PLCC packages; is also available in die form.

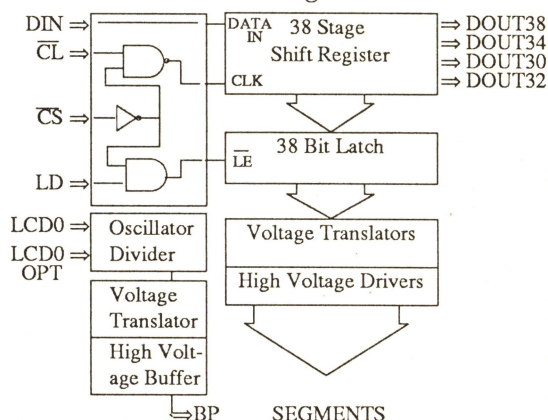
### Features

- High Voltage Outputs Controlled by 5 Volt Logic
- Pin-Out Adaptable to 30, 32, 34 or 38 Segments
- RC Oscillator or External Backplane Input
- TTL Compatible Inputs with Input Protection
- Low Power Consumption
- Wide Range Supply Voltage [ $V_{DD}$ ,  $V_{EE}$ ]
- Pin for Pin Compatible with AMI S4520 series
- Cascadable
- Military Level Processing Available

### Applications

- Standard Liquid Crystal Displays
- Dichroic Liquid Crystal Displays
- Vacuum Fluorescent Displays

### Functional Block Diagram



### Absolute Maximum Ratings

(Voltages referenced to  $V_{SS} = 0V$ )

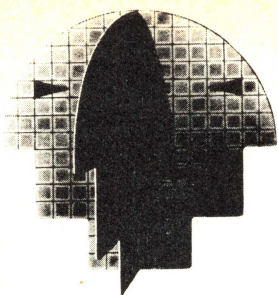
Supply Voltage	$V_{DD}$	.....	0.3V to +18V
	$V_{EE}$	.....	$V_{DD} - 35V$ to -0.3V
Voltage at any Input (except LCD0)		.....	-0.3V to $V_{DD} + 0.3V$
Voltage at LCD0 Input		.....	$V_{DD} - 35V$ to $V_{DD} + 0.3V$
DC Current Drain per Input Pin		.....	10mA
Power Dissipation		.....	AC = 30mW... DC = 250mW
Operating Temperature Range: plastic		.....	-40°C to +85°C
	ceramic	.....	-55°C to +125°C
Storage Temperature Range: plastic		.....	-50°C to +150°C
	ceramic	.....	-65°C to +150°C

### DC Electrical Characteristics

$V_{DD} = 5V$ ,  $V_{EE} = -25V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$  (Unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	$V_{DD}$		3		18	V
Supply Current	$I_{DD}$	No Load			200	$\mu A$
	$I_{EE}$	No Load $f_{BP} = 100HZ$			150	$\mu A$
Input Low Voltage (excluding LCD0)	$V_{IL}$		0		1.3	V
Input High Voltage (excluding LCD0)	$V_{IH}$		2		$V_{DD}$	V
Input Low Voltage (LCD0)	$V_{ILX}$		$V_{EE}$		2	V
Input High Voltage (LCD0)	$V_{IHx}$		2.5		$V_{DD}$	V
Input Current	$I_{IN}$	$V_{IN} = 0$ to 5V			1	$\mu A$
Input Capacitance	$C_i$				5	pf
Segment Output Impedance	$R_{SEG}$	$I_L = 10\mu A$			10,000	$\Omega$
Backplane Output Impedance	$R_{BP}$	$I_L = 10\mu A$			450	$\Omega$
Data Out Current	$I_{DOH}$	Source Current $V_{OH} = 4.5V$			0.6	mA
	$I_{DOL}$	Sink Current $V_{OL} = 0.5V$	-0.6			mA

Holt Integrated Circuits, 9351 Jeronimo Road, Irvine CA 92718 (714) 859-8800 (800) 222-HOLT



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  - 8 to 1 Micron Geometries
  - Gallium Arsenide
  - STD-Cell/Gate-Array Implementation
  - 2 Volts to 35 Volts
- **S SUPPORT — CAD LAYOUT**
  - Apollo/Mentor Workstations
  - Daisy Workstations
  - PC/AT Based Design Software
  - VAX 780
  - Calma GDSII
  - PDP/11
  - Schematic Capture
  - Logic Simulation
- **I C'S — CUSTOM/SEMICUSTOM**
  - Full Custom
  - Standard Cell
  - Gate-Array
- **C CUSTOM PACKAGES**
  - Plastic or Ceramic
  - DIP 8-64
  - PLCC 28-84
  - Pin Grid Array
  - Chip on Board
  - Module

### FOR MORE INFORMATION

Contact—Sales/Marketing Department (215) 265-8690 or Telex 846196



# 5CBIC PROGRAMMABLE BUS INTERFACE CONTROLLER

- Higher Integration Alternative to Transceivers, Latches, Multiplexers and PAL\* Functions
- Applications Include Dual Port Control, Multiplexed Bus Interface, DRAM Control and Similar Functions
- Port-Oriented Bus Management Unit Supports:
  - 3-Way Asynchronous Data Transfer on Byte-Wide Buses
  - Programmable Option of Latched or Real Time Data
  - True or Complement Data Path
- Macrocell-Based Programmable Logic Unit Provides:
  - Variable Input and Output Architecture
  - On-Chip Controls for the Bus Management Unit
- Up to Eight Buried Registers
- Programmable Registers can be Configured as Positive Edge-Triggered D-, J-K, R-S or T- Types
- Asynchronous Preset and Clear on All Registers
- Option of Latched Inputs
- Low Power: 75  $\mu$ A Typical Standby
- CHMOS EPROM Technology Based:
  - Max Bus Port Drive Capability: 16 mA
  - Typical Data Transfer Delay Between Ports = 25 ns
  - Logic Array Operating Frequency = 20 MHz
- Available in 44-Lead PLCC Package  
(See Packaging Spec., Order # 231369)

The Intel 5CBIC is useful in implementing bus interfacing logic functions that have traditionally been done using SSI/MSI TTL components. Core bus functions are provided that can be customized using EPROM bits for specific applications. Control logic can also be implemented through a sum of products architecture that is included in this 44-lead PLCC package. Such levels of integration are realized utilizing the benefits of Intel's advanced CHMOSII-E process.

This general purpose architecture is supported by iPLDS II, Intel's Programmable Logic Development System, to develop the design and program the devices. Several methods of entry facilitate the design resulting in shorter completion times.

\*PAL is a trademark of Monolithic Memories, Inc.

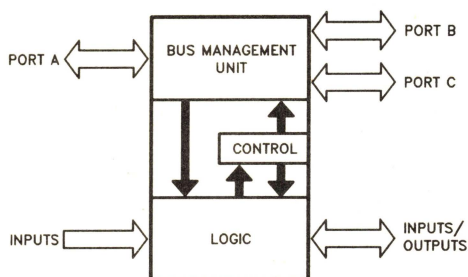


Figure 1. Block Diagram

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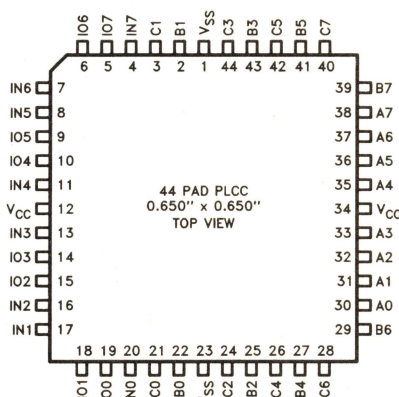


Figure 2. Lead Configuration

290126-2

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1987**  
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## iPLDS II THE INTEL PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM VERSION II

- Hardware and Software Necessary to Turn Design Concepts into Functional Erasable Programmable Logic Devices (EPLDs)
- Menu-driven Software with On-line Help Messages for All Stages of the Design Process
- iUP-PC Hardware Programs Intel EPLD's, EPROM's, E<sup>2</sup>PROM's, Peripherals, and Microcontrollers with one PC-based System
- All Equipment Interfaces with the IBM PC/XT\*, PC/AT\*, and True Compatibles
- JEDEC Standard Design File, Part Utilization Report, Minimized Equation File, and Compiler Error File All Available as Outputs
- Supports a Variety of Input Methods:
  - Schematic Entry
    - TTL Library
    - EPLD Primitives Library
  - Text Editor Entry
    - State Machine
    - Boolean Equations
- Macro Expander Accepts TTL, and User-Defined Macros and Expands Them into Equivalent EPLD Primitives
- Espresso\*\* Minimizer Reduces Logic Equations to Least Number of Product Terms
- Supports All Intel EPLD's Including the 5CBIC and 5AC312

Release 1.5 of Intel's Programmable Logic Development System II (iPLDS II) is a powerful set of tools for transforming a logic design into customized silicon. The system provides design entry, logic compilation, and device programming capability on a desktop using an IBM PC/XT, PC/AT, or compatible.



iPLDS II Components Picture

290134-1

\*IBM PC/XT, PC/AT are registered trademarks of International Business Machines Corporation.

\*\*ESPRESSO is a copyrighted by the University of California at Berkeley and is used with permission.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1987**  
© Intel Corporation, 1987 **Order Number: 290134-003**





## PEEL Family of EEPLDs

PEEL™ devices (Programmable Electrically Erasable Logic devices), combine CMOS and EEPROM technologies to offer an attractive alternative to conventional PLDs. PEEL devices eliminate PLD design tradeoffs by providing a balance of features most needed by logic designers today. These features include:

- Low power consumption
- High Speed
- Noise immunity
- Electrical reprogrammability
- 100% factory testability
- Enhanced architecture/design features
- Emulation of other PLDs
- Inventory simplification
- Foolproof design security
- Development and program support
- Cost effectiveness

Architectural flexibility and ease of design are the keys to efficient logic development. A variety of architectures combined with the flexibility of programmable I/O macrocells ensures that there is a PEEL device that can be tailored to the precise requirements of your design. Programming support and development tools are readily available from ICT and third-party developers

The PEEL family is divided into two groups: direct and super-set replacement.

### Direct Replacement PEEL Devices

These PEEL devices are JEDEC-file-compatible replacements for popular 24-pin PAL devices and 20 and 24-pin FPLAs. CMOS PEEL technology brings to these devices the advantages of low power, high noise-immunity, reprogrammability, complete testability, and foolproof design security.

### Superset Replacement PEEL Devices

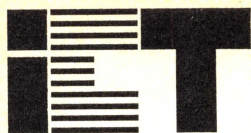
Superset replacement PEEL devices not only emulate all of the standard 20 and 24-pin PLDs but offer designers many other architectural and performance features unavailable in other devices.

### Programmable I/O Macrocell

A number of features differentiate the super-set replacement PEEL devices from conventional PLDs. One feature is the twelve-configuration output macrocell which provides control of output polarity, feedback path, output type (registered or combinatorial, dedicated input, output, or bidirectional I/O). This output macrocell not only allows one PEEL device to emulate an entire family of PLDs but also provides architectural options unavailable with any other PLD. Differences in product term allocation, the number of I/O pins, and special features such as "zero-power mode" and signature word also serve to set apart these devices from the PLDs which they superset.

	ARCHITECTURE							SPEED		POWER	
Superset	Pins	Inputs	I/Os	Registers	Macro Configs	Prog. Arrays	Product / Sum Terms	Prop Delay (nS) t <sub>CO</sub> t <sub>PD</sub>		Supply Current ICC (mA) Z-Mode*	
PEEL18CV8	20	10	8	8	12	AND	74	15-25	25-50	15+0.7/MHz	no
PEEL18CV8Z	20	10	8	8	12	AND	74	12-20	15-35	25+0.7/MHz	yes
PEEL22CV10Z	24	12	10	10	12	AND	132	12-20	25-35	45+0.5/MHz	yes
PEEL20CG10Z	24	12	10	10	12	AND	92	12-20	15-35	25+0.5/MHz	yes
PEEL253	20	8	10	0	2	AND/OR	42/20	N/A	30-40	35+0.5/MHz	no
PEEL273	24	12	10	0	2	AND/OR	42/20	N/A	30-40	35+0.5/MHz	no
*100µA Standby Current											
Direct	Pins	Inputs	I/Os	Registers	Macro Configs	Prog. Arrays	Product / Sum Terms	Prop Delay (nS) t <sub>CO</sub> t <sub>PD</sub>		Supply Current ICC (mA) Z-Mode	
PEEL22CV10	24	12	10	10	4	AND	132	12-20	25-35	45+0.5/MHz	no
PEEL20CG10	24	12	10	10	4	AND	90	12-20	15-35	25+0.5/MHz	no
PEEL153	20	8	10	0	2	AND/OR	42/10	N/A	30-40	35+0.5/MHz	no
PEEL173	24	12	10	0	2	AND/OR	42/10	N/A	30-40	35+0.5/MHz	no





PLDs Emulated by PEEL Devices

PEEL™ Device	Can Emulate These PLDs							
PEEL18CV8	10H8	10L8	12H6	12L6	14H4	14L4	16H2	16L2
	16L8	16R4	16R6	16R8	16P8	16RP4	16RP6	16RP8
	16V8	16HD8	16LD8	18P8	EP310	EP320		
PEEL18CV8Z	All of the above plus EP320 (in Zero-Power Mode)							
PEEL20CG10Z	12L10	14L4	16L6	18L4	20L2	20L10		
	20L8	20R4	20R6	20R8	20V8	20CG10		
PEEL22CV10Z	All of the above plus 22V10							
PEEL253	PLS153 (82S153)							
PEEL273	PLS173 (82S173)							

Development support

PEEL devices provide designers with several options for development support. These include PEEL device evaluation, programming, and development tools from ICT, as well as popular programmer and development tools from third-party manufacturers.

The PEEL Evaluation Kit

The PEEL evaluation kit contains ICT product literature, PEEL device samples and APEEL™ development software. APEEL software can be used to develop PEEL devices or to translate existing PLD (PAL, EPLD, FPLA) JEDEC files for programming PEEL devices.

The PEEL Development System

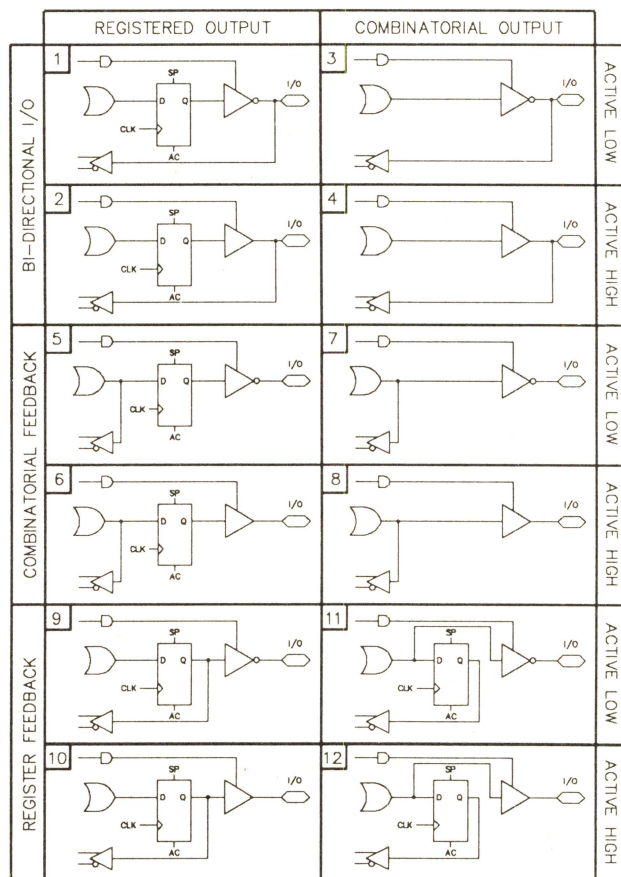
The PDS-1 PEEL Development System is a powerful, low-cost, PC-based system for designing with PEEL devices.

To fully support the advanced features of PEEL devices, the PDS-1 provides the tools needed to design from start to finish. Among them: a built-in word processor for design entry and editing; the APEEL Boolean-logic assembler; a complete PEEL-device programmer; and enhanced logic tester.

The PEEL Development System includes:

- APEEL Development Software
- PEEL Device Samples
- PEEL Programmer Board
- PEEL Device Programmer Module
- PEEL Development System Software

PEEL I/O Macrocell configuration equivalent circuits



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## PEEL<sup>TM</sup>173

# CMOS Programmable Electrically Erasable Logic Device

### Features

#### ■ FPLA ARCHITECTURE

- 12 inputs and 10 I/Os
- Programmable AND/OR arrays
- 42 product terms:
- 32 logic terms, 10 control terms
- 10 sum terms

#### ■ DROP-IN REPLACEMENT FOR PLS173

- Pin compatible
- JEDEC file compatible

#### ■ APPLICATION VERSATILITY

- Replace random SSI/MSI logic
- Create customized comparators, multiplexers, encoders, converters, etc.

#### ■ ADVANCED CMOS EEPROM TECHNOLOGY

#### ■ LOW POWER CONSUMPTION

- 35mA + 0.5mA/MHz max

#### ■ HIGH PERFORMANCE

- $t_{PD} = 30ns$  max,  $t_{OE} = 30ns$  max

#### ■ EE REPROGRAMMABILITY

- Superior programming and functional yield
- Low cost windowless package
- Erases and programs in seconds

#### ■ DEVELOPMENT SUPPORT

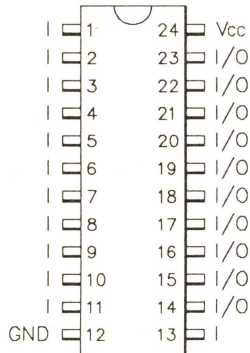
- Third-party software and programmers
- ICT PEEL Development System with APEEL<sup>TM</sup> Logic Assembler

### General Description

The ICT PEEL173 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional FPLAs. Designed in advanced CMOS EEPROM technology, the PEEL173 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL173 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

The PEEL173 provides both a programmable AND array and a programmable OR array to offer drop-in compatibility with the bipolar PLS173. Applications for the PEEL173 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL173 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

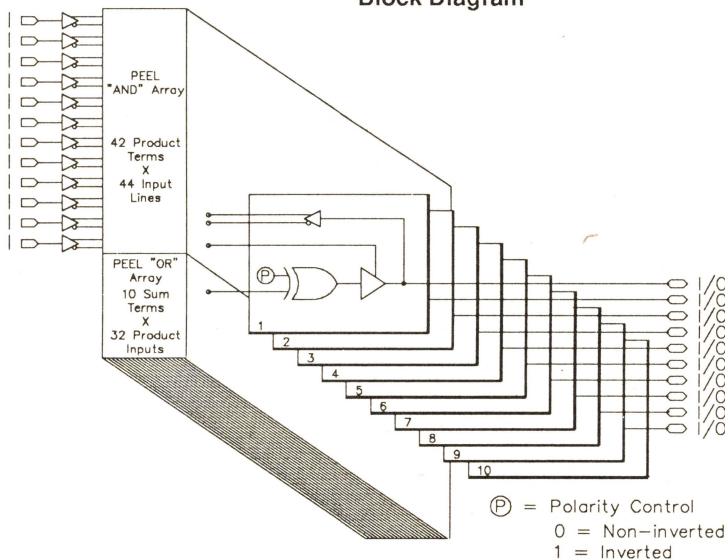
#### Pin Configuration



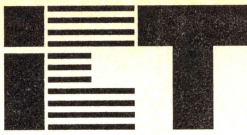
#### Pin Names

I = Dedicated Input  
I/O = Bidirectional I/O  
GND = Ground  
Vcc = Power Supply (5V)

#### Block Diagram







## PEEL<sup>TM</sup>273

# CMOS Programmable Electrically Erasable Logic Device

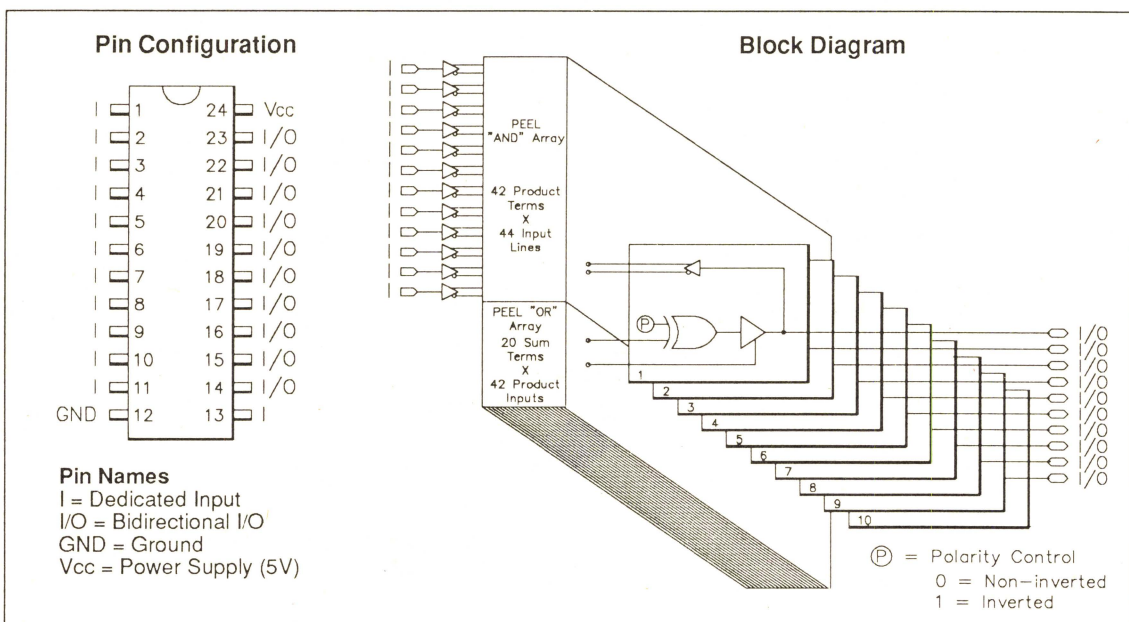
### Features

- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 35mA + 0.5mA/MHz max
- **HIGH PERFORMANCE**
  - $t_{PD} = 30\text{ns}$  max,  $t_{OE} = 30\text{ns}$  max
- **ARCHITECTURAL FLEXIBILITY**
  - 12 inputs and 10 I/Os
  - Programmable AND/OR arrays with 42 product terms/10 sum terms
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **FPLA ARCHITECTURE**
- **SUPERSET REPLACEMENT FOR PLS173**
  - Ten additional product terms
  - Output-enable terms in OR array
  - Signature word
  - Foolproof design security
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers, encoders, converters, etc.
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System with APEEL<sup>TM</sup> Logic Assembler

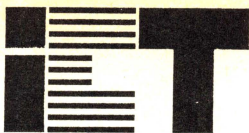
### General Description

The ICT PEEL273 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL273 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL273 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

The PEEL273 provides both a programmable AND array and a programmable OR array. It offers superset compatibility with the bipolar PLS173 with several architectural enhancements, including: output enable terms in the OR array, 10 additional product terms, and signature word. Applications for the PEEL273 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL273 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.







## PEEL<sup>TM</sup>153

# CMOS Programmable Electrically Erasable Logic Device

### Features

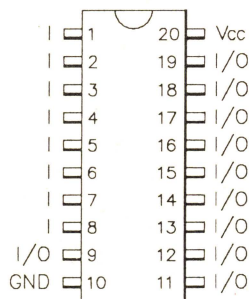
- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 35mA + 0.5mA/MHz max
- **HIGH PERFORMANCE**
  - $t_{PD} = 30ns$  max,  $t_{OE} = 30ns$  max
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System with APEEL<sup>TM</sup> Logic Assembler
- **FPLA ARCHITECTURE**
  - 8 inputs and 10 I/Os
  - Programmable AND/OR arrays
  - 42 product terms:
    - 32 logic terms, 10 control terms
  - 10 sum terms
- **DROP-IN REPLACEMENT FOR PLS153**
  - Pin compatible
  - JEDEC file compatible
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers, encoders, converters, etc.

### General Description

The ICT PEEL153 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional FPLAs. Designed in advanced CMOS EEPROM technology, the PEEL153 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL153 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

The PEEL153 provides both a programmable AND array and a programmable OR array to offer drop-in compatibility with the bipolar PLS153. Applications for the PEEL153 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL153 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

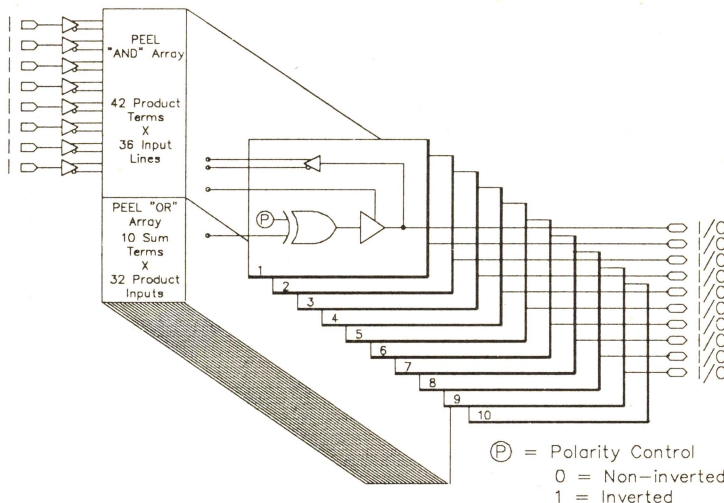
Pin Configuration



#### Pin Names

I = Dedicated Input  
I/O = Bidirectional I/O  
GND = Ground  
Vcc = Power Supply (5V)

Block Diagram







## PEEL<sup>TM</sup>253

# CMOS Programmable Electrically Erasable Logic Device

## Features

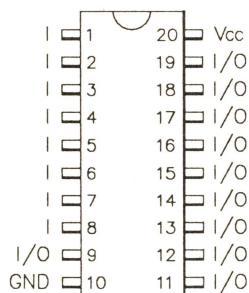
- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 35mA + 0.5mA/MHz max
- **HIGH PERFORMANCE**
  - $t_{PD} = 30ns$  max,  $t_{OE} = 30ns$  max
- **ARCHITECTURAL FLEXIBILITY**
  - 8 inputs and 10 I/Os
  - Programmable AND/OR arrays with 42 product terms/10 sum terms
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **FPLA ARCHITECTURE**
- **SUPERSET REPLACEMENT FOR PLS153**
  - Ten additional product terms
  - Output-enable terms in OR array
  - Signature word
  - Foolproof design security
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers, encoders, converters, etc.
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System with APEEL<sup>TM</sup> Logic Assembler

## General Description

The ICT PEEL253 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL253 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL253 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 20-pin, 300-mil DIP.

The PEEL253 provides both a programmable AND array and a programmable OR array. It offers superset compatibility with the bipolar PLS153 with several architectural enhancements, including: output enable terms in the OR array, 10 additional product terms, and signature word. Applications for the PEEL253 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL253 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

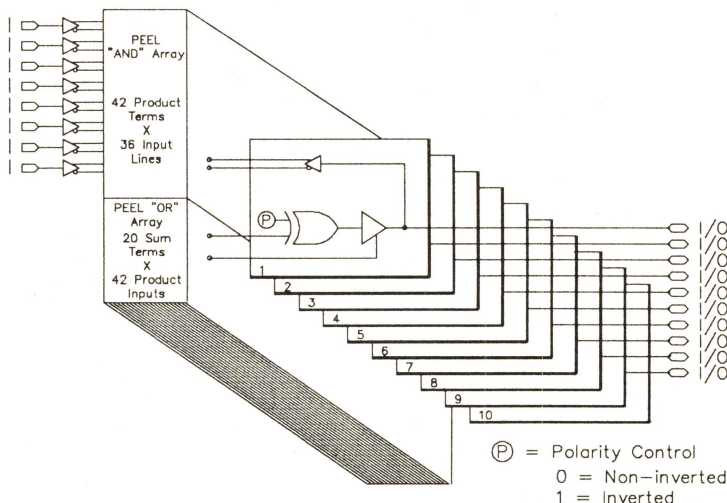
### Pin Configuration



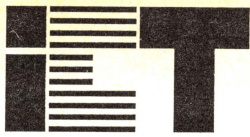
#### Pin Names

I = Dedicated Input  
I/O = Bidirectional I/O  
GND = Ground  
Vcc = Power Supply (5V)

### Block Diagram







# PEEL22CV10Z<sup>TM</sup>

## CMOS Programmable Electrically Erasable Logic Device

### Features

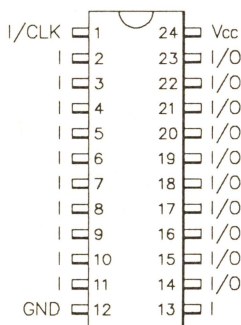
- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - Zero Power Mode - 100 $\mu$ A max standby
  - 35mA + 0.5mA/MHz max
- **HIGH PERFORMANCE**
  - $t_{pd}$ =25nS max,  $t_{CO}$ = 15nS max
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **DEVELOPMENT/PROGRAMMER SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System with APEEL<sup>TM</sup> Logic Assembler
- **ARCHITECTURAL FLEXIBILITY**
  - 132 product term X 44 input AND array
  - Up to 22 inputs and 10 outputs
  - Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - Independently programmable 12-configuration I/O macrocells
  - Synchronous preset, asynchronous clear
  - Independent programmable output enables
- **APPLICATION VERSATILITY**
  - Replaces random SSI/MSI logic
  - Emulates 24-pin bipolar PAL devices
  - Superset compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

### General Description

The ICT PEEL22CV10Z is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10Z rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption, along with a "zero-power" standby mode. The EE reprogrammability of the PEEL22CV10 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a 24-pin, 300-mil DIP.

The PEEL22CV10Z's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10 plus eight additional macrocell configurations (a total of twelve) that further expand its I/O and feedback design capabilities. Applications for the PEEL22CV10Z include: replacement of random SSI/MSI logic circuitry; emulation of 24-pin bipolar PAL devices; and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10Z is provided by ICT and third-party manufacturers.

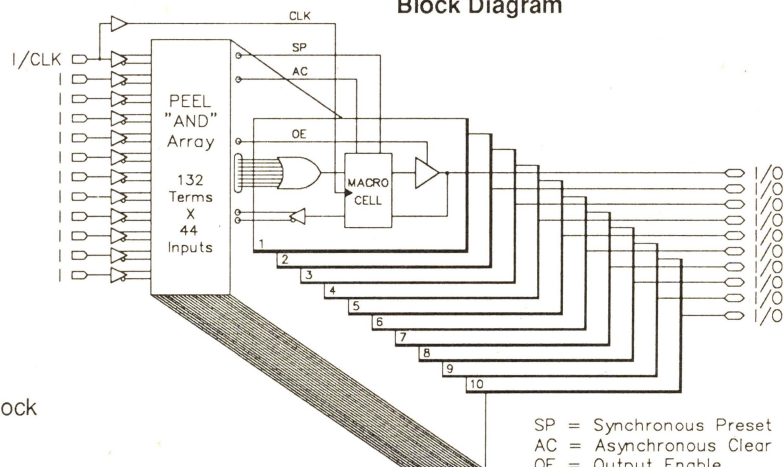
Pin Configuration



**Pin Names**

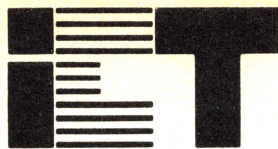
I/CLK = Dedicated Input/Clock  
I = Dedicated Input  
I/O = Bidirectional I/O  
GND = Ground  
Vcc = Power Supply

Block Diagram



SP = Synchronous Preset  
AC = Asynchronous Clear  
OE = Output Enable





# PEEL<sup>TM</sup>18CV8

## CMOS Programmable Electrically Erasable Logic Device

### Features

#### ■ ADVANCED CMOS E<sup>2</sup>PROM TECHNOLOGY

#### ■ LOW POWER CONSUMPTION

- CMOS: 15mA Standby + 1mA/MHz Max
- TTL: 25mA Standby + 1mA/MHz Max

#### ■ HIGH PERFORMANCE

- $T_{PD}$  25nS Max,  $T_{CO}$  18nS Max,  $T_{SC}$  15nS Min

#### ■ REPROGRAMMABILITY

- 100% factory tested
- Cost effective "window-less" package
- Erases and programs in seconds
- Adds convenience, reduces field retrofit and development cost

#### ■ FOOLPROOF DESIGN SECURITY

- Prevents unauthorized reading or copying of design

#### ■ ARCHITECTURAL FLEXIBILITY

- 74 Product Term X 36 Input array
- Up to 18 Inputs and 8 I/O pins
- Independently configurable I/O macro cells: polarity, register, combinatorial, bi-directional
- Synchronous preset, asynchronous clear
- Independent output enables

#### ■ APPLICATION VERSATILITY

- Replaces SSI/MSI logic
- Emulates bipolar PAL\* devices and the EP300/310
- Simplifies inventory control
- Allows new design possibilities

#### ■ DEVELOPMENT/PROGRAMMER SUPPORT

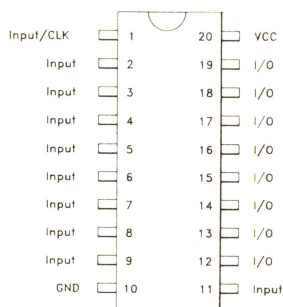
- PC based development tools and programmer support from ICT and third party manufacturers

### General Description

The ICT PEEL<sup>TM</sup>18CV8 is a CMOS Programmable Electrically Erasable Logic device that provides a high performance, low power, reprogrammable, and architecturally flexible alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS E<sup>2</sup>PROM technology, the performance of the PEEL18CV8 rivals speed parameters of standard bipolar PLDs with a dramatic improvement in power consumption. The electrically erasable reprogrammable technology of the PEEL18CV8 not only reduces development and field retrofit costs but enhances testability enabling ICT to ensure 100% field programmability and function.

Packaged in a cost effective "window-less" 20 pin DIP, the flexible architecture of the PEEL18CV8 allows for replacement of standard SSI/MSI logic circuitry or pin-out compatible emulation of 20-pin bipolar PAL\* devices and the Altera EP300/310. In addition, over a hundred new logic configurations, not possible with earlier generation PLDs, can be implemented. Development and programming support of the PEEL18CV8 is provided by popular third-party PC based development tools and stand-alone programmers. ICT also offers evaluation and development tools specifically for the PEEL18CV8 and other PEEL devices.

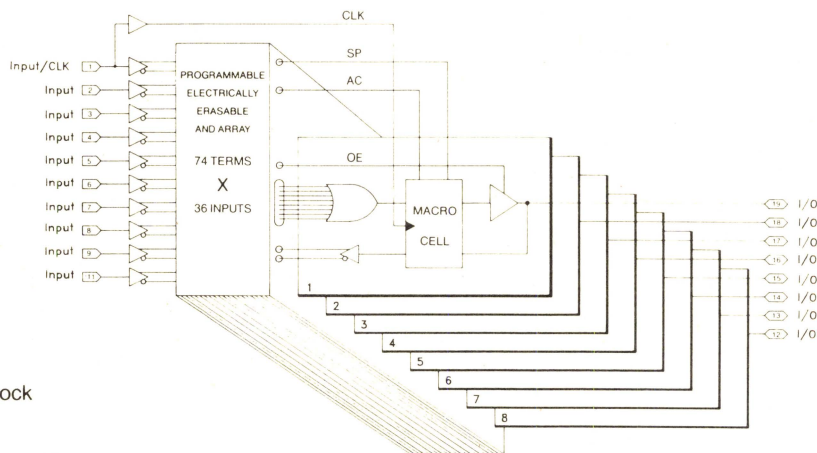
**Pin Diagram**  
(Figure 1)



#### Pin Names

INPUT/CLK	Input and/or Clock
INPUT	Input
GND	Ground
I/O	Bi-Directional Input/Output
V <sub>CC</sub>	Power Supply (+5V)

**Block Diagram**  
(Figure 2)



SP = Synchronous Preset  
AC = Asynchronous Clear  
OE = Output Enable

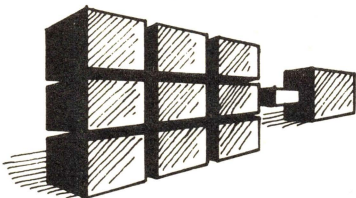


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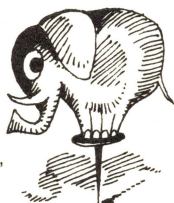
## EXTRA·CUSTOM SAVES YOU MONEY WITH MAXIMUM SYSTEM INTEGRATION:

our engineers examine your total system to put more components on your chip. That means fewer components for you to mount on your board. (This is not routinely done by semi-custom suppliers.)



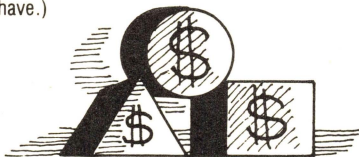
## EXTRA·CUSTOM SAVES YOU MONEY WITH MAXIMUM AREA EFFICIENCY AND MINIMUM PIN COUNT:

utilizing CAE/CAD to speed and verify the design, our engineers optimize your logic for MOS, and fully customize chip layout to reduce function area, interconnect, and pin count. The less silicon used, and the fewer pins, the lower the unit price for your chip. (Semi-custom provides little opportunity for such optimization.)



## EXTRA·CUSTOM SAVES YOU MONEY WITH THE RIGHT MOS PROCESS TECHNOLOGY:

the process our engineers recommend for your chip *will always be the most cost effective* for your requirements. (With semi-custom you *must* use the process they have.)



## EXTRA·CUSTOM MAKES MONEY FOR YOU WITH MULTI- SOURCED PRODUCTION:

our universal design rules let us use numerous fabricators, which ensures delivery of your chips on time. The more product you can ship on time, the more money you make. (With semi-custom, multi-sourcing is normally not available.)



## EXTRA·CUSTOM MAKES MONEY FOR YOU BECAUSE

our engineers concentrate on designing the chip and the test program that goes with it, while *your* engineers concentrate on developing new products. (With semi-custom, your engineers are all tied up designing the chip and test program.)

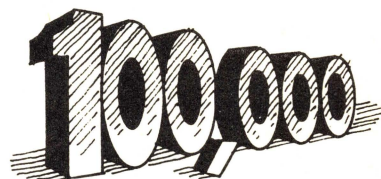
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- ☐ Programmable digital delay-timers
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- ☐ Autocorrelators ☐ PBX systems
- ☐ Sound generators for toys and alarms
- ☐ Security system auto-dialers and wireless transmitters ☐ Motor speed controllers
- ☐ Electronic music for greeting cards and consumer novelties ☐ Pay TV decoders
- ☐ Frequency and event counters
- ☐ Synchro-to-digital converters
- ☐ Remote tone-activated isolation devices for telephone lines ☐ Camera electronics
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- ☐ Police speed radar guns
- ☐ High frequency oscillator/dividers

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## LMB6000 Micro bASIC™ Arrays

<b>Description</b>	<p>The LMB6000 Micro bASIC Arrays offer high performance features for entry-level ASIC design. LSI Logic's Channel Free™ architecture provides design flexibility and reduced propagation delays while the LMB6000's 0.9-micron channel length (1.5-micron drawn gate length) 2-layer metal HCMOS technology offers low power consumption and high noise margin. Seven array sizes feature 700 to 6700 usable gates and speeds greater than 74S TTL (0.57 ns through 2-input NAND and interconnect at TA = 25°C and VDD = 5V). Industry standard plastic package types with predefined power and ground pins facilitate PC board design and chip layout. Package selection is optimized for array size. Choose from 28-, 40-, 48-, 68- and 84-pin implementations.</p>		<p>The versatile LMB6000 libraries contain industry standard logic elements for design applications such as TTL replacement, boardspace reduction and logic optimization. With LSI Logic's Logic Integrator™ software, LMB6000 designs are created schematically and then netlisted, verified and simulated. The completed design files are transferred to LSI Logic for circuit layout and prototype manufacturing. Logic Integrator design software contains all the library elements and algorithms necessary to easily and rapidly design an LMB6000 Micro bASIC Array.</p>
<b>Features</b>	<ul style="list-style-type: none"> <li>■ 0.9-micron channel length (1.5-micron drawn gate length), 2-layer metal HCMOS</li> <li>■ Seven array sizes: 1968, 3286, 4992, 7238, 9504, 14124 and 19000 available gates</li> <li>■ Micro bASIC macrocell library</li> <li>■ Non-power pads configurable as inputs, outputs or bidirects</li> <li>■ TTL/CMOS I/O compatibility</li> <li>■ Output drive: 1, 2, 4, 6 and 8 mA</li> <li>■ Full commercial operating range: 0°C to +70°C, 5 V ± 5%</li> <li>■ Channel-Free architecture</li> </ul>		<ul style="list-style-type: none"> <li>■ Slew rate control on outputs</li> <li>■ Input protection circuitry</li> <li>■ Optimized array size/package combinations</li> <li>■ Plastic package options: 28PDIP, 40PDIP, 48PDIP, 68PLCC and 84PLCC</li> <li>■ Pre-assigned primary VDD and VSS pins</li> <li>■ Fully supported by MDE™ for verification, simulation and layout</li> <li>■ Logic Integrator workstation software with schematic entry</li> <li>■ Compatible with LC6000, LL7000 and LL9000 macrocell libraries</li> </ul>
<b>Benefits</b>	<ul style="list-style-type: none"> <li>■ Fast prototype and production unit delivery</li> <li>■ Simplified design process with Logic Integrator design software</li> <li>■ Reduces board space and system size</li> <li>■ Up to 82 signal I/O capability</li> </ul>		<ul style="list-style-type: none"> <li>■ Increases system reliability with greater device integration</li> <li>■ Complete applications support from worldwide LSI Logic design resource centers</li> <li>■ Right-first-time guaranteed</li> </ul>

Table 1. Product Offerings

Device Number	Estimated <sup>(1)</sup> Usable Gates	Gate Complexity	Plastic Package Selection					Minimum VDD, Minimum VSS, Maximum Signal I/O Pins <sup>(2, 3)</sup>				
			28 DIP	40 DIP	48 DIP	68 PLCC	84 PLCC	28 DIP	40 DIP	48 DIP	68 PLCC	84 PLCC
LMB6020	700	1,968	X	X	X			1,1,26	1,1,38			
LMB6033	1,200	3,286	X	X	X			1,1,26	1,1,38	1,1,46		
LMB6050	1,750	4,992	X	X	X	X		1,1,26	1,1,38	1,1,46	1,1,66	
LMB6072	2,500	7,238	X	X	X	X	X	1,1,26	1,1,38	1,1,46	1,1,66	2,2,80
LMB6095	3,300	9,504	X	X	X	X	X	1,1,26	1,1,38	1,1,46	1,1,66	2,2,80
LMB6141	5,000	14,124	X	X	X	X	X	1,1,26	1,1,38	1,1,46	1,1,66	2,2,80
LMB6190	6,700	19,000	X	X	X	X	X	1,1,26	1,1,38	1,1,46	1,1,66	2,2,80

Notes:

1. Gates used will vary by design.
2. I/O pins may be configured as VDD/VSS, subject to the number and drive of output buffers.
3. Each package type has a minimum of two pre-assigned pins for VDD and VSS. Additional VDD/VSS pin options are available.

MDE, LSI Logic and design, bASIC, Channel-Free and Logic Integrator are trademarks of LSI Logic Corporation.



## LMA9000 Micro Array™ Series

<b>Description</b>	<p>The LMA9000 Micro Array series offers high gate density and high performance with the low power consumption and high noise margin of 0.9-micron channel length (1.5-micron drawn gate length) 2-layer metal HCMOS technology. The series is implemented in LSI Logic Corporation's Channel-Free™ architecture, in which potentially active transistors fill LMA9000 array cores. This allows flexible placement and routing of macrocells, macrofunctions and memories in any configuration for maximum design flexibility and reduced propagation delays. LMA9000 Micro Array devices provide from 700 to 12,500 usable gates and up to 172 I/O pads. High reliability, high gate density and on-board memory capabilities make an LMA9000 Micro Array device suitable for universal logic replacement capable of fully integrating TTL logic. Whether</p>		<p>designing new ASICs or converting existing designs, an extensive library of SSI/MSI cells and LSI/VLSI megafunctions as well as RAM and ROM blocks are available. Packaging options include a variety of plastic and ceramic pin-grid arrays, dual in-line, leadless and leaded chip carriers.</p> <p>VLSI applications for the larger Micro Array devices include intelligent special purpose processors, multi-function controllers and other high performance subsystem architectures. Smaller LMA9000 devices make suitable replacements for high-speed Schottky TTL or 10K ECL logic. Mid-range Micro Array ASICs are ideal for high performance dedicated peripheral controllers and intelligent support functions.</p>
<b>Features</b>	<ul style="list-style-type: none"> <li>■ Silicon gate 0.9-micron channel length (1.5-micron drawn gate length), 2-layer metal HCMOS technology</li> <li>■ Gate speed equivalent to 10K ECL; faster than 74S TTL; 0.57 ns through 2-input NAND gate, standard load = 2, VDD = 5 V, TA = 25°C</li> <li>■ Up to 172 signal I/O capability</li> <li>■ Extensive macrocell, macrofunction, megafunction, metal-megacell and memory library</li> <li>■ Ten array sizes from 1,968 to 34,944 gates</li> <li>■ Fully supported by Modular Design Environment™ (MDE™) software for verification, simulation and layout</li> <li>■ Channel-Free architecture for maximum layout flexibility</li> </ul>		<ul style="list-style-type: none"> <li>■ Random routing with hierarchical function placement</li> <li>■ Configurable output drive up to 12 mA with slew rate control</li> <li>■ Over voltage and latch-up protection for inputs and outputs</li> <li>■ TTL/CMOS I/O compatibility</li> <li>■ Efficient implementation of large logic blocks</li> <li>■ Extensive selection of ceramic and plastic packages</li> <li>■ ESD protection greater than 2001 V</li> <li>■ Functionally compatible with LL7000 and LL9000 macrocell and macrofunction libraries</li> <li>■ Full Military capability</li> <li>■ LMA9072Q Evaluation Device</li> </ul>
<b>Benefits</b>	<ul style="list-style-type: none"> <li>■ Higher system performance achievable with greater integration and fewer I/O boundary crossings</li> <li>■ Fast prototype and production unit delivery with masterslice technology</li> <li>■ Increases system reliability with greater device integration and smaller chip sizes</li> <li>■ Complete library compatibility with existing LL7000/LL9000 designs provides performance improvements</li> </ul>		<ul style="list-style-type: none"> <li>■ Full range of popular SSI to VLSI library elements allows efficient and rapid implementation of customer logic</li> <li>■ Reduces board space and system size due to maximum integration capability</li> <li>■ Complete design and applications support from worldwide LSI Logic design centers</li> </ul>

### Product Offerings

Device Number	Estimated Usable Gates <sup>1</sup>	Gate Complexity	Total Pads	Min Power Pads <sup>2</sup>		Max I/O Pads <sup>3</sup>
				VDD	VSS	
LMA9020	700	1,968	44	1	2	41
LMA9033	1,200	3,286	58	1	2	55
LMA9050	1,750	4,992	70	1	2	67
LMA9072	2,500	7,238	86	2	4	80
LMA9095	3,300	9,504	98	2	4	92
LMA9141	5,000	14,124	118	2	6	110
LMA9190	6,700	19,000	138	2	6	130
LMA9239	8,400	23,908	154	4	6	144
LMA9284	10,000	28,388	168	4	6	158
LMA9350	12,500	34,944	186	4	10	172

#### Notes:

1. Gates used will vary by design.
2. Minimum power pads required to be bonded to package pins.
3. I/O pads may be configured as VDD/VSS, subject to number and drive of output buffers.

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## LCA10000 Compacted Array™ Series

### Description

The LCA10000 Compacted Array series is an HCMOS semicustom technology offering from 10K to 50K usable gates and speed performance equivalent to 10K ECL. Processed using 0.9-micron channel length (1.5-micron drawn gate length) 2-layer HCMOS technology, the LCA10000 series features LSI Logic's Channel-Free™ architecture. Without predetermined metal routing channels, Channel-Free arrays allow flexible placement and routing of macrofunctions, macrocells, megafunctions and memories of any configuration. This maximizes design flexibility and enhances propagation speeds. An extensive design library contains hundreds of basic SSI/MSI cells and LSI/VLSI megafunctions including a wide selection of industry standard microprocessors, peripherals, multipliers and ALUs. Up to 32K ROM and 8K static RAM blocks plus logic can be implemented on a single chip.

The LCA10000 accommodates a maximum 256 I/O signals. A family of ceramic PGA chip packages for up to 299 pins is available.

Speed (2-input NAND delay = 0.57 ns—FO = 2) and extremely high density make the LCA10000 series ideally suited for achieving system-to-silicon integration. Sophisticated algorithms incorporated in LSI Logic's Modular Design Environment™ development software allow designers to take their design from schematics to silicon with the certainty that the result will be functionally correct and meet design performance specifications.

Fully configurable output buffers are available with drive strengths of 1, 2, 4, 6, 8 and 12 mA. A slew rate control circuit allows each output dV/dt to be tailored to individual load conditions.

### Features

- Silicon-gate 0.9-micron channel length (1.5-micron drawn gate length), 2-layer metal HCMOS technology
- Speeds equivalent to 10K ECL — 0.57 ns through 2-input NAND gate, standard load = 2, VDD = 5 V, TA = 25°C
- Up to 256 signal I/O capability
- Extensive macrocell, macrofunction and megafunction library elements
- Six array sizes from 25,740 to 129,042 gates
- Fully supported by MDE™ software for verification, simulation and layout
- Channel-Free architecture for maximum layout flexibility
- Random routing with hierarchical functional placement
- Configurable output drive up to 12 mA with slew rate control capability
- Inputs and outputs protected from over-voltage and latchup
- TTL/CMOS I/O compatibility
- Efficient implementation of large logic blocks
- Clock driver distribution methodology
- Advanced packaging techniques
- ESD protection: 2001 V

### Product Benefits

- Higher system performance achievable with greater integration and fewer I/O boundary crossings
- Fast prototype and production unit delivery with masterslice technology
- Increases system reliability with greater device integration
- Complete Library compatibility with existing LL7000/LL9000/LMA9000 Micro Array™ designs provides upward density migration
- Full range of popular SSI to VLSI library elements allows efficient and rapid design of advanced system architectures
- Reduces board space and system size due to maximum integration capability
- Complete design and applications support from worldwide LSI Logic design centers

### Product Outline

Device Number	Gate Complexity	Estimated <sup>(1)</sup> Usable Gates	Total Device Pads <sup>(2, 4)</sup>	Minimum Power Pads <sup>(2, 5)</sup>		Maximum I/O Pads <sup>(2, 3)</sup>
				VDD	VSS	
LCA10026	25,740	10,000	168	4	6	154
LCA10038	37,932	15,000	204	8	12	184
LCA10051	50,904	20,000	234	8	12	214
LCA10075	74,970	30,000	282	8	12	256
LCA10100	100,182	40,000	326	8	12	256
LCA10129	129,042	50,000	368	8	12	256

#### Notes:

1. Usable gates will vary, depending on design.
2. I/O pads may be configured as VDD/VSS, subject to number and drive of output buffers.
3. I/O signals presently limited to 256 by tester capability.

4. Includes eight dedicated VDD pads.
5. Minimum power pads required to be bonded to package pins.

LSI Logic and design, Compacted Array, Channel-Free, Micro Array, Modular Design Environment and MDE are trademarks of LSI Logic Corporation.



## LSC15 Series 1.5-Micron HCMOS Cell-Based ASICs

### Description

The LSC15 Series is a family of standard cell format ASICs for creating high-density cost-effective semi-custom devices. Implemented in 0.9-micron channel length (1.5-micron drawn gate length) 2-layer metal HCMOS technology, LSI Logic Corporation cell-based ASICs combine ECL speeds with the lower power consumption and higher noise margin characteristics of CMOS technology. The LSC15 Series offers extensive design libraries and the added capability to incorporate high-density memory blocks using LSI Logic Modular Design Environment™ (MDE™) tools such as memory and logic compilers. Custom and fixed-die sizes are available.

LSC15 Cell-Based ASICs begin with a classic standard cell architecture of fixed-height variable-length cells and then incorporate hard-coded, hand-packed or compiled logic elements in large VLSI building block formats for complex design requirements. The gate-level blocks are arranged in rows separated by routing

channels for metal interconnects. A variable-width routing channel that expands only for required metal interconnects optimizes silicon usage.

Design libraries contain comprehensive collections of gate-level SSI, MSI, LSI and VLSI building blocks (macrocells, macrofunctions, megafunctions and megacells) in both hard-coded and soft-coded versions, as well as memory blocks. Choose from behavioral and gate-level models of industry standard devices such as AMD's 2900, Motorola's 6800 and Intel's 8200 microprocessor families or from LSI building blocks including high-speed adders, ALUs, barrel shifters, comparators, as well as large multiplier blocks. Custom compilation of RAM and ROM blocks meets a wide range of application requirements. Compile up to 72 K bits of static RAM or up to 512 K bits of ROM to any depth or width, with one through five ports. Memory options include First-In First-Out (FIFOs), Last-In First-Out (LIFOs) and Content Addressable Memories (CAMs).

### Features

- 0.9-micron channel length (1.5-micron drawn gate length), 2-layer metal, silicon gate HCMOS technology
- Up to 60,000 equivalent gate complexity
- Typical gate delays of 570 picoseconds (ND2C 2-input NAND gate with 8 standard loads, VDD = 5V, TA = 25°C)
- Latchup immunity over 200 mA
- Electrostatic discharge (ESD) protection of over 2000 V
- High density memory blocks
  - High-speed static RAM compilable up to 72 K bits
  - Up to 5 ports available
  - Metal-layer programmable ROM compilable up to 512 K bits
  - Specialized memories including FIFOs, LIFOs, and CAMs
  - Memory blocks compiled to any user-specified widths and depths
- Full military capability
- Up to 348 pads (328 signal I/Os, 256 testable) with choice of
  - Input, output or bidirectional buffer
  - HCMOS or TTL input levels
  - Different output drive capability and slew rate
- All LSI and VLSI megafunctions either available as, or can be converted into, megacells
- Built-in scan circuitry on all memories and megacells
- Choice of system-level test structures for logic elements
- Full netlist compatibility with all other LSI ASIC Products
- Fully supported by LSI's Modular Design Environment software
- Extensive macro libraries
  - Gate-level, SSI, MSI, LSI, and VLSI building blocks
  - Over 400 LSI and VLSI elements
  - Each macrocell available in three versions varying in drive strengths

### Design Flexibility

LSI Logic Cell-Based ASICs represent a high-density, yet flexible, approach to semicustom design. Using MDE design tools and compilers, ASIC designers can select from a variety of cell versions to meet drive-strength, space and other requirements. Figure 1 shows three versions of a 4-input NOR gate. Each version varies in drive strength and silicon space required

for layout. For example, NR4B has a higher drive capability than NR4A and thus requires more silicon (8 cell units for NR4B vs 6 cell units for NR4A). LSI Logic's cell-based ASIC flexibility means designers can optimize their designs by using cell versions that best match requirements.

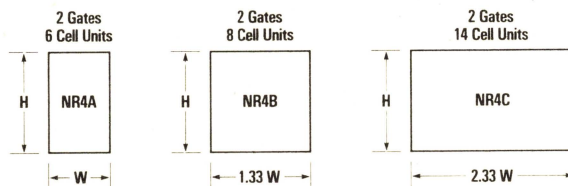


Figure 1. Example of Area Occupied by Various Versions of a 4-Input NOR Gate Cell

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## HCMOS Libraries

<b>Overview</b>	<p>LSI Logic HCMOS design libraries support all ASIC product offerings. The design libraries contain the logic elements and timing and functional data that designers need to develop and characterize their ASICs.</p> <p>One or more libraries are available for each ASIC family. Library contents depend on the logic complexity and gate count of the technology. The more complex the ASIC technology, the more varied and sophisticated the available libraries. Add-on libraries, such as megafunctions, are optional for many ASIC families.</p>	<p>LSI Logic design libraries contain hundreds of basic SSI, MSI, and TTL-type cells. The libraries also have more than 400 LSI and VLSI blocks including a wide selection of industry-standard microprocessors, peripherals, multipliers and megacells describe the categories of available logic elements. Macrocells and megacells are hard-coded; macrofunctions and megafunctions are soft-coded.</p>
<b>Macrocells</b>	Macrocells are the basic building blocks available to ASIC designers. Macrocells—ORs, NANDs, flip-flops—	are comprised of logic gates, each of which is configured using two n and p-channel transistor pairs.
<b>Macrofunctions</b>	Macrofunctions are combinations of macrocells that form logic blocks of greater complexity. LSI Logic's wide selection of macrofunctions includes SSI/MSI	functions such as adders, counters, registers, etc. (see Table 1).
<b>Megafunctions</b>	Combinations of macrocells and macrofunctions that implement a complex yet common logic element are called megafunctions. Megafunctions include CAMs (Content Addressable Memories), barrel shifters, multipliers and ALUs (see Table 2). LSI Logic offers a large and growing set of standard-product megafunctions	that are functionally compatible with processors, peripherals and other devices from Intel, AMD and Motorola, including the Intel 8254 programmable timer/counter, the AMD29203 registered ALU and Motorola 6845 CRT controller.
<b>Megacells</b>	LSI Logic offers both logic and memory megacells for cell-based ASICs and for gate arrays. Megacells are specialized fixed metallization patterns which use a combination of cells to implement hard-coded functions including standard and custom memory blocks tailored to their design requirements. For cell-based de-	sign, customers can compile up to 72K-bits of static RAM or up to 512K-bits of ROM to any depth or width, with one through five ports. Standard memory options include First-In First-Out (FIFOs) and Last-In First-Out (LIFOs).

**Table 1. Representative Macrofunctions**

<b>Adders</b> Up to 16 bits	<b>Parity Generators</b> 8-bit odd parity detector
<b>Comparators</b> Magnitude Equality 4 and 8 bits	<b>Decoders</b> 2-to-4 decoders 3-to-8 decoders 4-to-10 decoders
<b>Registers</b> 8-bit data latch 8-bit data register, clear direct 4-bit shift register, sync parallel load and clear 4-bit shift register, async parallel load	<b>Counters</b> Binary, BCD, Gray and Johnson counters in a variety of configurations Large modulo counters

**Table 2. Representative Megafunctions**

<b>ALUs</b> 4-bit 181 type 16-bit 181 type 32-bit 181 type	<b>Barrel Shifter</b> 8-bit 16-bit 32-bit
<b>Clock Generators</b> Two phase clock generator, buffered	<b>2900 Family</b> 2901 2909 2910
<b>LIFO</b> 5 × 12	<b>FIFO</b> 16 × 4
<b>Multipliers</b> 8 × 8 12 × 12 16 × 16	<b>CAMs</b> 32 × 4 16 × 4 8 × 4 4 × 4



## Overview

### Description

LSI Logic, the pioneer in semicustom IC design and fabrication, offers the most advanced HCMOS gate array and cell-based application-specific integrated circuits (ASICs) in the industry. Comprehensive and flexible design packages such as LSI Logic's Modular Design Environment™ (MDE)™ development system and third-party CAD Connection Program are fully integrated with LSI Logic's advanced wafer fabrication and assembly facilities to provide ASICs that work the first time and that are guaranteed to meet customer specifications. Whether customers use LSI Logic's MDE software design system, in-house third party CAE tools, or an LSI Logic Design Resource Center, LSI Logic's proven track record of over 4,000 successful designs assures right-the-first-time ASIC solutions.

The LSI Logic Design Flow (see next page) is an integrated ASIC solution that includes advanced software design tools, technology libraries, logic compilers and hardware accelerators to provide everything required to characterize complex single-chip and multi-chip mixed-mode ASIC designs in almost any environment and on all popular workstations and mainframes. These development tools are available through LSI Logic Design Resource Centers and in a variety of configurations as MDE product offerings or via LSI Logic certified CAE vendors.

LSI Logic's ASIC methodology forms the most advanced system available for describing, simulating, verifying, manufacturing and testing 0.7-micron channel length (1-micron drawn gate length) and 0.9-micron channel length (1.5-micron drawn gate length) HCMOS 2-layer and 3-layer metal interconnect ASIC products. LSI Logic's extensive gate-array, cell-based and standard product ASICs feature low, intermediate and high logic complexities ranging from 880 to over 100K usable gates. All of the gate array products employ LSI Logic's Channel-Free™ architecture. Channel-Free array cores are filled with potentially active transistors without any predetermined metal routing channels. This allows flexible and efficient placement and routing of logic cells and memories in any configuration for a maximum of design flexibility as well as enhanced propagation speeds.

Advanced wafer fabrication, assembly, testing and packaging technology also makes LSI Logic the leader in ASIC manufacturing. With worldwide production facilities extending from the USA to Great Britain, Germany and Japan, LSI Logic's manufacturing operations are geared to handle the special needs of the ASIC market: large high-density chips, a wide variety of packages, short manufacturing runs and complex test patterns. Though customer requirements vary, the end

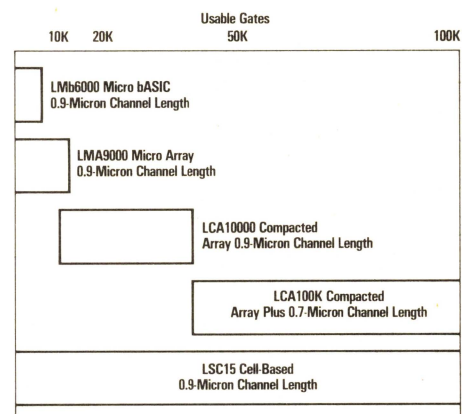
result is always the same: tested and working array prototypes are delivered in only 2-3 weeks—or just 7 days if the customer requires faster turnaround. Tested and working cell-based prototypes are delivered in 6 weeks.

The LMA9000 Micro Array™ series is a 0.9-micron channel length (1.5-micron drawn gate length) 2-layer HCMOS product family offering 10K ECL speeds and intermediate logic complexities up to 10K usable gates in a Channel-Free architecture. LMA9000 devices incorporate SSI/MSI, as well as LSI/VLSI logic and memory building blocks.

The LCA10000 Compacted Array™ offers from 10K to 50K usable gates using 0.9-micron channel length (1.5-micron drawn gate length) 2-layer HCMOS technology and Channel-Free architecture. The LCA100K Compacted Array Plus™, available in 1988, is a 0.7-micron channel length (1-micron drawn gate length) 2-layer metal HCMOS leading-edge array family providing a usable gate range from 50K to 100K.

The LMB6000 Micro bASIC™ series is an economical gate array technology with usable gate counts up to 6700. This entry-level ASIC technology combines high-end features such as 0.9-micron channel length (1.5-micron drawn gate length) 2-layer metal HCMOS with the design-flexibility and enhanced speed of Channel-Free array cores.

The LSC15 Cell-Based ASICs come in 0.9-micron channel length (1.5-micron drawn gate length) 2-layer metal HCMOS and support any combination of RAM, ROM, standard cells, VLSI building blocks and compiled cells in a classic variable-height, variable-width layout format.



LSI Logic's family of products covers the entire ASIC spectrum.

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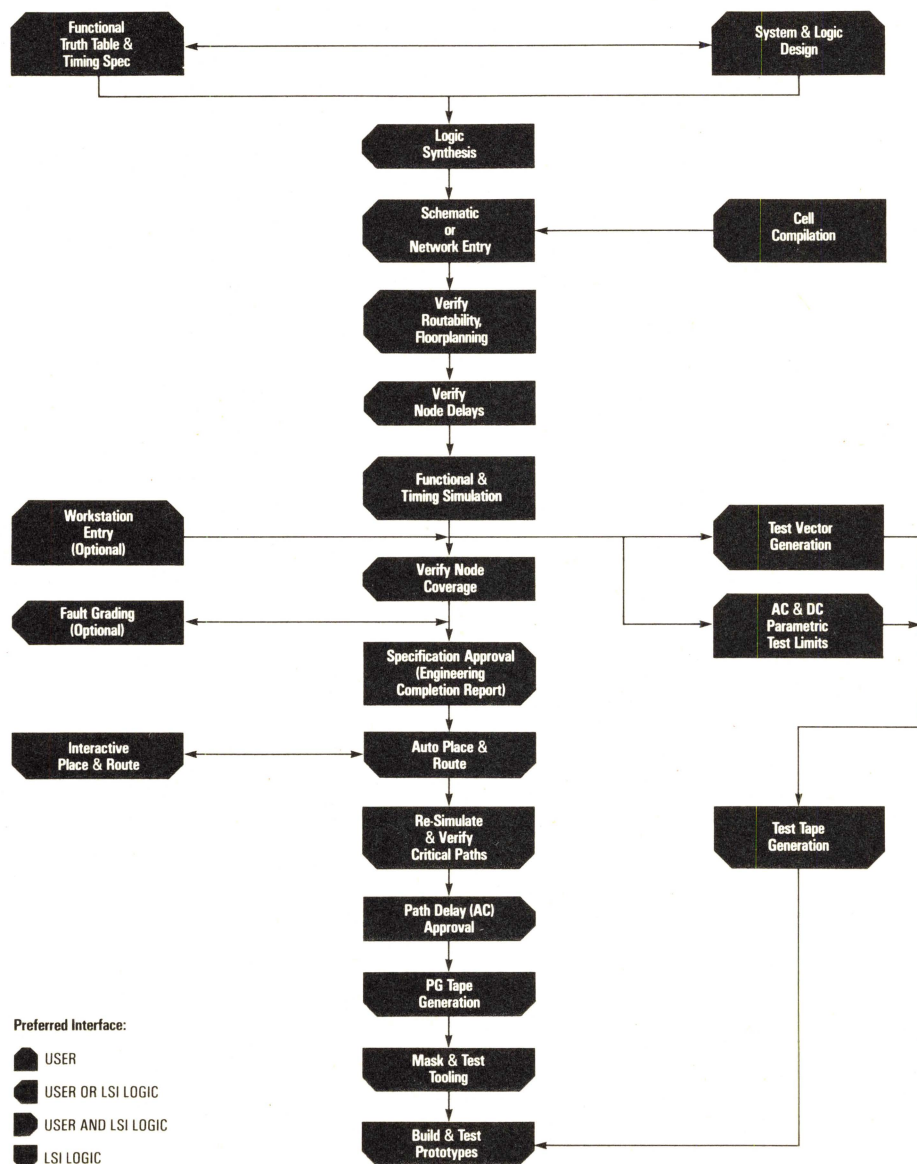
## Overview

LSI Logic standard products, including DSP and Image processors, military microprocessors, and fixed- and floating-point 16- and 32-bit multiplier-accumulators, are also manufactured using industry-leading 0.9-micron channel length (1.5-micron drawn gate length) HCMOS technology. Available also as cells on ASIC chips, these standard products find applications in high-end digital computer systems in the military/aerospace, data processing and telecommunications industries.

LSI Logic's extensive set of design libraries contains all the popular SSI and MSI functions and more than

400 industry-standard LSI and VLSI logic and memory building blocks for channeled and Channel-Free arrays and Cell-Based designs.

LSI Logic maintains the industry's largest ASIC design support network and a full range of hardware and software design tools. At over two dozen Design Resource Centers worldwide, experienced application engineers offer expert training and design assistance, providing customers with the design expertise, hardware platforms and software tools required to integrate systems in silicon.



LSI Logic Design Flow



## Global Design Resource Centers

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### Comprehensive Design Support

LSI Logic Corporation maintains the world's largest ASIC design support network. Over two dozen Design Resource Centers provide access to qualified LSI Logic application engineers and a full range of hardware and software design tools. Whether customer engineers elect to work at or through a design center,

experienced application engineers offer expert training and design assistance. Comprehensive support includes design training, access to extensive technology libraries, use of CAD equipment and tools and distribution of design literature, databooks and technical information.

### Features

- Full support for all LSI logic channelled and Channel-Free™ array and cell-based ASIC designs
- Experienced LSI Logic application engineers offer detailed and comprehensive design assistance
- Access to major software and hardware tools and environments:
  - Mainframes
  - Workstations
  - Silicon compilers
  - PAL converters and logic synthesizers
  - Hardware accelerators
  - SSI, MSI, LSI and VLSI technology libraries
- Demonstration facilities to introduce customers to the latest tools and technologies
- Full customer facilities for on-site or remote design entry and simulation
- Design courses offered on-site
- Worldwide design tool network for fast and comprehensive service and support
- Full marketing and sales support

### LSI Logic Sales Offices and Design Resource Centers

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- Sales Offices with Design Resource Centers

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# MICREL

## MPD8020

### CMOS/DMOS SEMICUSTOM HIGH VOLTAGE ARRAY

PRELIMINARY

#### CONCEPT

The MPD8020 is a monolithic I.C. semiconductor array of low voltage CMOS analog and digital circuits on the same chip with high voltage DMOS power transistors. For quick turnaround time, wafers are held at the last step (metallization) where the customer's specific metal interconnect pattern makes each wafer run into thousands of custom I.C.'s. These smart power ASIC's (Application Specific I.C.'s) cast in silicon the proprietary advantages of the customer's design even for moderate volume applications, and give the customer a size, reliability and performance advantage over the competition!

#### GENERAL DESCRIPTION

The MPD8020 CMOS/DMOS Semicustom High Voltage Array uses **Micrel's** proprietary process to combine TTL/CMOS compatible high speed CMOS logic, CMOS analog, and high voltage DMOS power drive circuits on the same monolithic I.C. A single +5 Volt to +15 Volt supply powers the logic and analog circuitry while the high voltage portion functions at voltages of from +20 Volts to +100 Volts. An optional internal voltage pump with the help of two external components generates an extra voltage such that the high side gates of the power N-channel DMOS FET's are driven approximately 15 Volts above the +100 Volt supply allowing rail-to-rail high voltage switching.

The MPD8020 in combination with **Micrel's** CAD systems, CAE simulations (SPICE, Hi-Low, TIMVER, etc.) and an experienced fab and test group give a design engineer a highly versatile means of taking a circuit idea from concept to packaged silicon.

#### AVAILABLE IN:

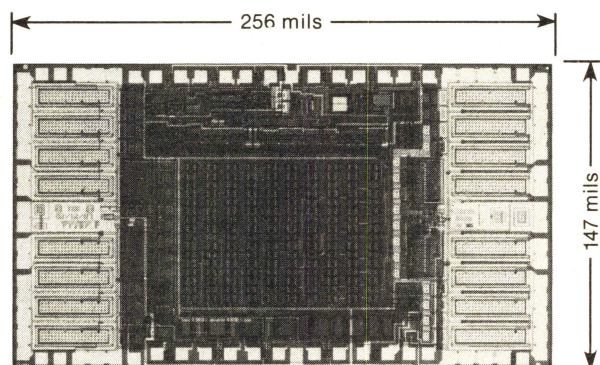
- Chip Form
- 16 to 48 pin plastic DIP's
- 16 to 48 pin ceramic DIP's
- Ceramic LCC's
- Surface mount packages
- PLCC
- Fused lead PLCC and DIP's
- Custom packages

#### FEATURES

- 16 N-Channel DMOS power FET's (fully floating sources, gates and drains), each 100 V, 200 mA, and 10 ohms.
- DMOS can be paralleled for 100 V, 3.2 Amp, 0.625 ohm single, half bridge, full bridge or bilateral switches.
- 200 CMOS gates in an uncommitted gate array.
- 12 TTL/CMOS I/O buffers.
- 3 op amp / comparator / Schmitt Triggers.
- 1 unity gain analog buffer.
- Bandgap reference (1.25 V / 2.5 V).
- Overtemperature sensor.
- Voltage pump (drives high side gates above  $V_{DD}$ ).
- 16 medium current sink pre-drivers.
- 16 high voltage level-shifting high side pre-drivers.
- Separate analog and digital ground ( $V_{SS}$ ) pads.
- Numerous logic I/O, high voltage I/O,  $V_{CC}$  and  $V_{DD}$  pads.
- Miscellaneous resistors, capacitors, and a zener.
- Available to military temperature range specifications.
- Selection of military, commercial, and power packages.

#### APPLICATIONS

- Switching regulators
- Motor control
- Bilateral analog switching
- High voltage switching
- Relay and solenoid driver
- Smart switch with bus decode
- Half or full bridge driver
- 3 phase driver
- Lamp driver
- Differential line driver
- Automotive switching
- Printer solenoid driver
- High voltage display driver



MPD8020 CMOS/DMOS/Bipolar Semicustom Array

**MICREL INC. 1235 Midas Way Sunnyvale, California 94086**

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## MPD8020 MACRO CELL MENU

- 16 fully floating 100 V, 200 mA, 10 ohm Vertical-DMOS FET's
- 16 high voltage 100 V P and N channel level shifters (made up of 32 cross coupled 20 to 50 mA P & N channel pairs)
- 200 CMOS gates in an uncommitted gate array
  - over 30 pre-designed logic "templates" of shift registers, decoders, flip-flops, NAND gates, NOR gates, etc.
  - general purpose op amps, comparators and Schmitt Triggers, implemented in the gate array
- 12 TTL/CMOS I/O buffers
- 16 logic predrivers (with logic enable) for bottom side DMOS drive
- 3 configurable op amp / comparator / Schmitt Trigger cells which can be hooked-up as:
  - ground sensing or  $V_{CC}$  sensing amplifiers or comparators
  - folded cascode high performance amplifiers
  - NPN input amplifiers
  - programmable bandwidth / power consumption amplifiers
- A unity gain buffer with adaptive bias (to drive large loads with minimum quiescent current)
- A bandgap reference with a 1.25 V output plus multiple programmable outputs up to  $V_{CC}$
- An over-temperature protection circuit with programmable temperature trip points and hysteresis
- A master bias programming circuit for all the linears
- A high voltage  $V_{++}$  "doubler" for N-channel gate drive above the +100 V  $V_{DD}$  rail
- A low voltage ( $V_{CC}$ ) pass regulator to drive a local low voltage analog and digital power supply from the high voltage supply
- Multiple current mirrors both at high (100 V) and low (15 V) levels
- Floating zener clamps, avalanche zeners, references and Schottky diodes
- Diffusion, diffusion P-well, pinched and poly resistors
- 40 picofarads of on-chip capacitance
- Isolated PNP and NPN transistors

## What MICREL Supplies with the MPD8020

- MPD8020 CMOS/DMOS Semicustom High Voltage Array Data Sheet
- MPD8020 Kit Part #1, Analog SSI and MSI Circuits
  - Kit parts in a 40 pin DIP with eleven commonly used analog circuits
  - Kit Part #1 data sheet with specifications and application hints
- MPD8020 Kit Part #2, Digital SSI and MSI Circuits
  - Kit parts in a 40 pin DIP with eight revealing digital circuits for checking speed and digital timing characteristics (also some analog circuits implemented in the gate array)
  - Kit Part #2 data sheet with specifications and application hints
- Highly experienced design and applications engineers on call to discuss how to optimize putting a complex analog, digital, and power circuit on one I.C.

## What MICREL Needs from You — the Designer

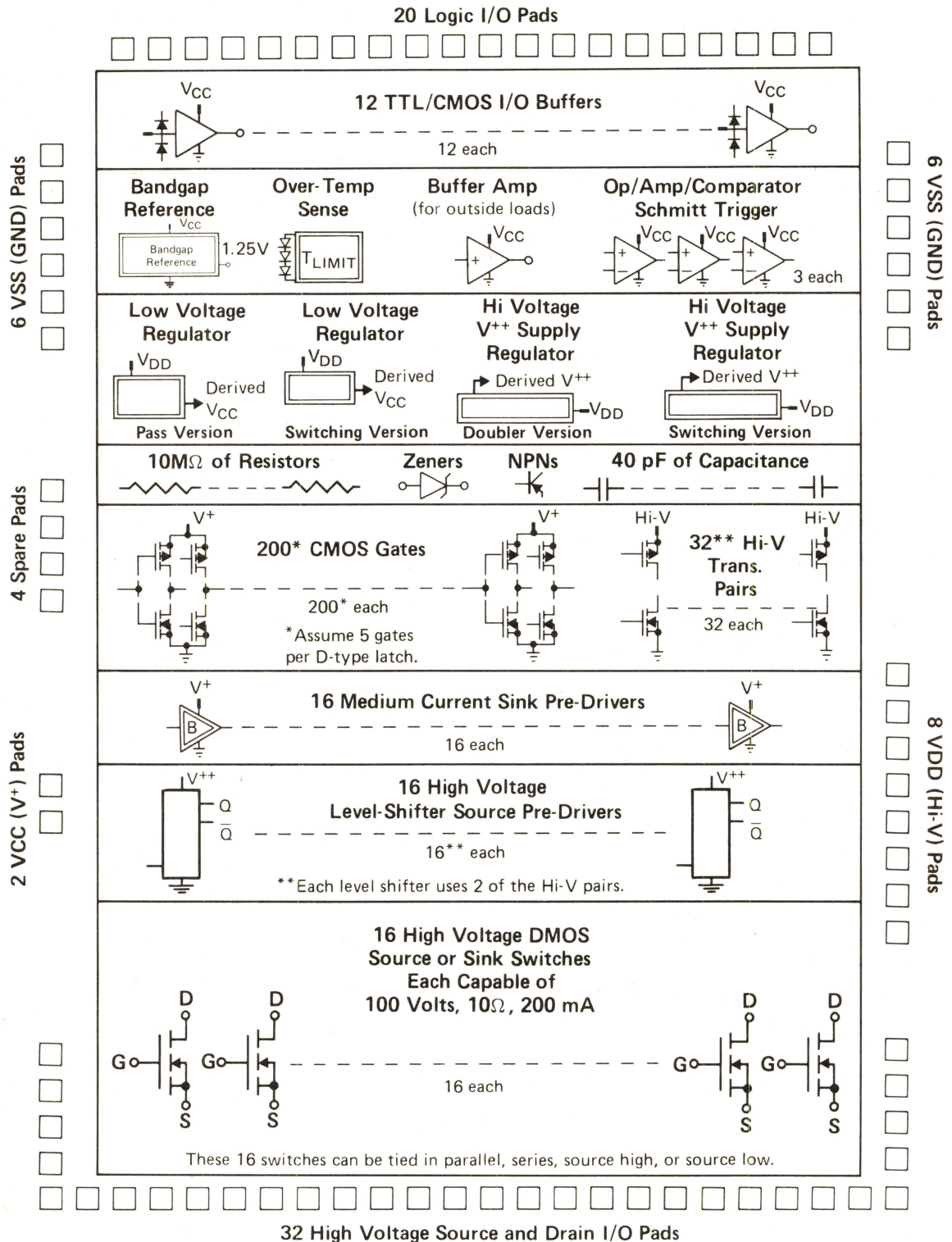
- System block diagram with basic I/O specifications, or
- Schematic of circuit implemented with analog, digital and discrete power transistors plus the I/O specifications, or
- Breadboard using our kit parts plus "glue" logic and I/O specifications, or
- Spice and Hi-Low netlists or any other compatible computer generated description and I/O specifications.

## Typical Semicustom Design Cycle Following Exploratory Discussions and Contract Initiation

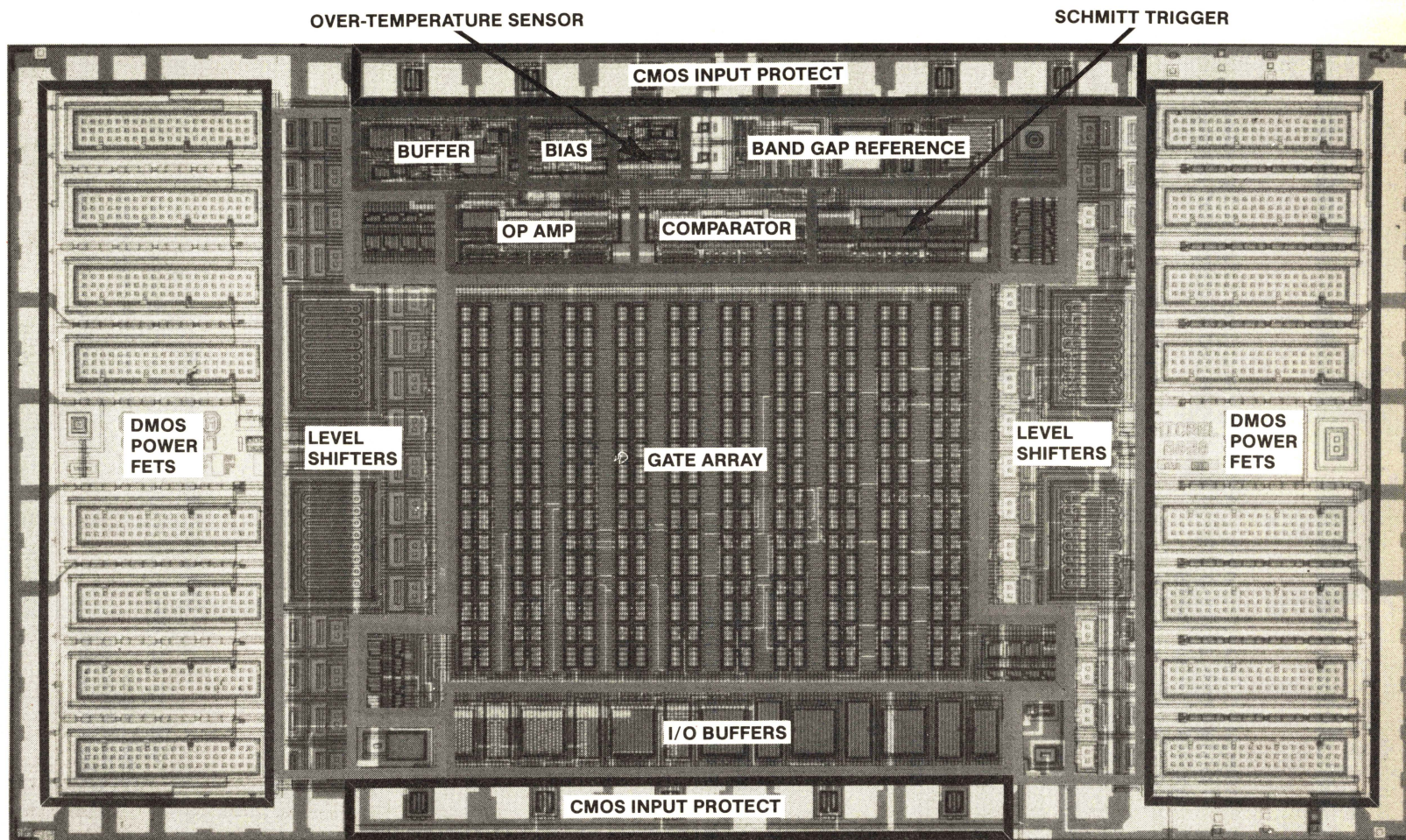
Week	Action
1	Design & Customer Interface
2	Design & Customer Interface
3	Electrical & Layout Computerized Checks
4	Mask Generation
5	Mask Generation
6	Apply ASIC Masks to Preprocessed Wafers
7	Wafer Test
8	Package Test Units
9	Final Test, QA & Ship 25 Units

## DETAILED COMPONENT

**AND PAD LISTING:** This diagram lists the components available to the designer for laying out an MPD8020 semicustom circuit. The I/O pads shown around the periphery represent the total number available; all pads are not normally used in a given circuit/package combination.







**MICREL \*MPD8020 CMOS/DMOS SEMICUSTOM HIGH VOLTAGE ARRAY**

(PATENT PENDING)

Micrel Inc. • 1235 Midas Way • Sunnyvale, California 94086  
 TEL: (408) 245-2500 • TWX: (910) 379-0007 • FAX: (408) 245-4175



**GENERAL**

Micro-Rel's CMOS Integrated Circuit technology includes 3 micron and 5 micron processes. Each process has linear and digital standard cells available. Micro-Rel's experienced IC design staff assures optimal performance for customer application requirements.

The wafer processing within Micro-Rel consists of ten thousand square feet of Class 100 Clean Room. These committed facilities insure high quality processing and quick turn around. Comprehensive manufacturing capability is available by having design, process, and test development at one site.

**CMOS IC Manufacturing Technologies:**

- |   |   |
|---|---|
| <input type="checkbox"/> Silicon Gate CMOS                        | <input type="checkbox"/> Rad-Hard Processing (Epitaxial Wafers) |
| <input type="checkbox"/> Linear CMOS                              | <input type="checkbox"/> Wafer Foundry Services                 |
| <input type="checkbox"/> Full Custom and Cell Based Custom Design | <input type="checkbox"/> Mil-Std-883C                           |

<b>3 MICRON CMOS</b> <div><input type="checkbox"/> P Well <input type="checkbox"/> Double Layer Metal <input type="checkbox"/> Single Layer Poly <input type="checkbox"/> Buried P<sup>+</sup> Capacitor</div> <div><input type="checkbox"/> Standard Digital Cells 25 MHz 8 Volt Maximum Supply Voltage -55°C to 125°C Operation <input type="checkbox"/> Standard Analog Cells <input type="checkbox"/> 1.3k ohms/sq., 200 ppm/°C Cr/Si Resistors</div>								<b>5 MICRON CMOS</b> <div><input type="checkbox"/> P Well <input type="checkbox"/> Double Layer Metal <input type="checkbox"/> Single Layer Poly <input type="checkbox"/> Buried P<sup>+</sup> Capacitor</div> <div><input type="checkbox"/> Standard Digital Cells 10 MHz 15 Volt Maximum Supply Voltage -55°C to 125°C Operation <input type="checkbox"/> Standard Analog Cells <input type="checkbox"/> 1.3k ohms/sq., 200 ppm/°C Cr/Si Resistors</div>							
<b>3 MICRON DEVICE CHARACTERISTICS</b>								<b>5 MICRON DEVICE CHARACTERISTICS</b>							
	N-CHANNEL			P-CHANNEL					N-CHANNEL			P-CHANNEL			
PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
V <sub>T</sub>	0.60	—	1.0	-0.60	—	-1.0	Volts	V <sub>T</sub>	0.60	—	1.0	-0.60	—	-1.0	Volts
BV <sub>ds</sub>	15	—	—	15	—	—	Volts	BV <sub>ds</sub>	21	23	—	18	—	—	Volts
Gamma	—	1.3	—	—	0.70	—	V <sup>1/2</sup>	Gamma	—	1.2	—	—	0.55	—	V <sup>1/2</sup>
X <sub>i</sub> S/D	—	0.5	—	—	0.5	—	Microns	X <sub>i</sub> S/D	—	1.1	—	—	0.90	—	Microns
X <sub>i</sub> P <sup>-</sup> Well	—	3.0	—	—	—	—	Microns	X <sub>i</sub> P <sup>-</sup> Well	—	5.0	—	—	5.0	—	Microns
T <sub>ox</sub>	475	—	575	475	—	575	Angstroms	T <sub>ox</sub>	730	—	800	730	—	800	Angstroms
N <sup>+</sup> Sheet Rho	—	23	—	—	—	—	Ohms/Square	N <sup>+</sup> Sheet Rho	—	20	—	—	—	—	Ohms/Square
P <sup>+</sup> Sheet Rho	—	—	—	—	65	—	Ohms/Square	P <sup>+</sup> Sheet Rho	—	—	—	—	50	—	Ohms/Square
P <sup>-</sup> Well Sheet Rho	—	2.2	—	—	—	—	k Ohms/ Square	P <sup>-</sup> Well Sheet Rho	—	2.5	—	—	—	—	k Ohms/ Square
Delta L	0.30	—	1.30	0.30	—	1.30	Microns	Delta L	1.0	—	2.5	0.80	—	2.30	Microns
Delta W	0	—	1.0	0	—	1.0	Microns	Delta W	1.0	—	3.0	1.0	—	3.0	Microns
K'	31	—	47	11	—	17	Microamps/V <sup>2</sup>	K'	28	—	38	8	—	14	Microamps/V <sup>2</sup>
Subthreshold Slope Factor	—	2.0	—	—	1.7	—		Subthreshold Slope Factor	—	2.0	—	—	1.9	—	

**DEVELOPMENT SEQUENCE**

Customer may initiate custom development at any of these stages.

- |   |   |
|---|---|
| <input type="checkbox"/> Circuit Diagram    | <input type="checkbox"/> Circuit, Logic & Timing Simulation |
| <input type="checkbox"/> Circuit Conversion | <input type="checkbox"/> IC Layout                          |
| <input type="checkbox"/> Schematic Capture  | <input type="checkbox"/> Design Verification† Database Tape |

**†DESIGN VERIFICATION SOFTWARE**

**Circuit Simulations:** SPICE 2G.6 + 3A.5, SPLICE, and SWITCHCAP  
**Logic Simulation:** DAISY Logician;™ MENTOR, and ASP  
**Mask and Layout Verification:** ECAD's DRACULA™ Software; DRC, ERC, LVS; & LPE

Micro-Rel™ 2343 West Tenth Place • Tempe, Arizona 85281 • TEL: 602-968-6411; TWX: 910-950-1941; FAX: 602-968-9691



**GENERAL**

Micro-Rel's Bipolar Integrated Circuit technology is comprised of 20, 40, and 100 volt processes. Each of these processes can utilize dielectrically isolated wafers. Dielectrically isolated wafers eliminate parasitic interaction between devices therefore improving radiation hardness and voltage handling capability. Speed and temperature characteristics are also enhanced.

Cr/Si resistors are also available in either process. Two ranges of resistance are available; 100k ohms/sq. and 1.3k ohms/sq. The high value resistors allow design at very low bias current which is important in battery powered applications.

**Bipolar IC Manufacturing Technologies:**

- |  |   |
|--|---|
| <input type="checkbox"/> Linear Bipolar                  | <input type="checkbox"/> Wafer Foundry Services |
| <input type="checkbox"/> Full Custom                     | <input type="checkbox"/> Mil-Std-883C           |
| <input type="checkbox"/> Rad-Hard Processing (DI Wafers) |   |

20 VOLT PROCESS				40 VOLT PROCESS			100 VOLT PROCESS			
8 Micron — feature size 20 Volt Maximum Supply Voltage MOS Capacitor 100k ohms/sq., – 5500 ppm/°C Cr/Si & 1.3k ohms/sq., 200 ppm/°C Cr/Si Resistors				8 Micron — feature size 40 Volt Maximum Supply Voltage MOS Capacitor 100k ohms/sq., – 5500 ppm/°C Cr/Si & 1.3k ohms/sq., 200 ppm/°C Cr/Si Resistors			8 Micron — feature size 100 Volt Maximum Supply Voltage **MOS Capacitor 100k ohms/sq., – 5500 ppm/°C Cr/Si & 1.3k ohms/sq., 200 ppm/°C Cr/Si Resistors			
BIPOLAR PROCESS CHARACTERISTICS										
	20 VOLT PROCESS			40 VOLT PROCESS			100 VOLT PROCESS			
	MIN.	TYPE.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Buried Layer (Arsenic)	18 5.0	— —	25 6.0	15 6.0	— —	35 8.0	— —	25 7	— —	Ohms/sq. Microns
EPI	2.0 8	— —	6.0 10	4.0 16	— —	7.0 20	7.0 20	— —	9.0 30	Ohm-cm Microns
Isolation	2.7 11	— —	6.6 —	5.0 20	— —	9.0 —	— —	DI* —	— —	Ohms/sq. Microns
Base	135 2.6	— —	165 3.3	180 2.6	— —	220 3.3	160 —	— 3.8	200 —	Ohms/sq. Microns
Emitter	3.5	—	5.0	3.5	—	5.0	3.5	—	5.0	Ohms/sq.
Capacitor Oxide	1300	—	1700	1300	—	1700	—	—	—	Angstroms
Thin Film Resistors 1.3k is low TC	80k 1.0k	100k 1.3k	120k 1.6k	80k 1.0k	100k 1.3k	120k 1.6k	80k 1.0k	100k 1.3k	120k 1.6k	Ohms/sq.
Metalization	— —	11k 1.0%	— —	— —	11k 1.0%	— —	— —	11k 1.0%	— —	Angstroms SiAl
Passivation (Si <sub>3</sub> N <sub>4</sub> )	—	7.5k	—	—	7.5k	—	—	7.5k	—	Anastroms

\*Dielectric Isolation: 1.5 Micron SiO<sub>2</sub>, 10 micron spacing. DI is also available in 20 and 40 volt processes. Consult factory for Dielectrically Isolated Process Information

\*\*Maximum voltage across MOS Capacitor, 50V.

**DEVELOPMENT SEQUENCE**

Customer may initiate custom development at any of these stages.

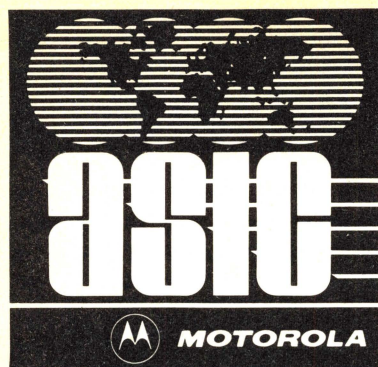
- |   |   |
|---|---|
| <input type="checkbox"/> Circuit Diagram    | <input type="checkbox"/> Circuit, Logic & Timing Simulation |
| <input type="checkbox"/> Circuit Conversion | <input type="checkbox"/> IC Layout                          |
| <input type="checkbox"/> Schematic Capture  | <input type="checkbox"/> Design Verification† Database Tape |

**†DESIGN VERIFICATION SOFTWARE**

- |                                      |  |
|--------------------------------------|--|
| <b>Circuit Simulations:</b>          | SPIICE 2G.6 +3A.5, SPLICE, and SWITCHCAP       |
| <b>Logic Simulation:</b>             | DAISY Logician,™ MENTOR, and ASP               |
| <b>Mask and Layout Verification:</b> | ECAD's DRACULA™ Software; DRC, ERC, LVS; & LPE |

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## Bipolar Macrocell Arrays

The Ideal Process for the Application . . .  
The Right Size for Efficient Utilization

**Motorola Semicustom** gives the designer the same process-technology choices available for discrete-logic designs, and the option of Macrocell array or cell-based functions for commercial and military applications.

- For very high speeds — state-of-the-art ECL arrays.
- For high-end TTL applications — ALS-TTL arrays have higher speed and lower power consumption at conventional TTL prices.
- For applications demanding low cost and/or very low power consumption — advanced 2-micron silicon-gate CMOS arrays.
- For both high drive and low power at high frequencies, BiMOS is the best of bipolar and CMOS blended on one chip.
- Finally, for the added capability of analog and complex megafunctions — a comprehensive library of cell-based functions.

Count on Motorola to help you select the right products for your application.

MCA I and MCA II Macrocell Arrays

Features	MCA 600ECL	MCA 800ECL	MCA 1200ECL	MCA 1500M	MCA 2500ECL	MCA 500ALS	MCA 1300ALS	MCA 2800ALS	MCA 2800RAM
Max Gate Equivalent	652	902	1192	1708 + RAM	2760	533	1280	2860	1800 + RAM
Major Macrocells	24	36	48	64	110	24	60	130	74
I/O Ports	46	54	60	120	120	57	75	120	120
Input/Interface Cells	25	—	32	—	—	26	40	120	120
Output Macrocells	18	22	26	60	68	27	40	120	120
Max Gate Delay (ns)	1.2	0.5	1.2	0.5	0.5	4.0	4.0	1.1	1.1
Max Toggle Freq. (MHz)	250	770	250	770	770	80	80	250	250
Power Dissipation (W)	2.5	2.5	4.0	8.0	8.0	1.0	1.4	3.5	3.0

## CMOS Macrocell Arrays

The Motorola HCA62A00 Series Macrocell Arrays consists of 2-micron gate length devices fabricated using a CMOS silicon-gate 2-layer metal technology. This technology pro-

vides high speed performance while maintaining the high noise immunity and low power consumption advantages of CMOS.

HCA62A00 Series CMOS Macrocell Arrays

Features	2-Micron HCA62A00 Series							
	HCA62A85	HCA62A67	HCA62A50	HCA62A36	HCA62A25	HCA62A17	HCA62A10	HCA62A06
Primary Cells	2856	2236	1656	1200	816	546	319	216
Equivalent Gates	8568	6708	4860	3600	2448	1638	957	648
Bidirectional Pads	168	146	124	100	84	68	52	44
VDD Pads	Power and ground pins are programmable to any package pin. Number of pins varies with array utilization and output loading.							
VSS Pads								
Typical Gate Delay (ns)	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1
Typical Freq. (MHz)	85	85	85	85	85	85	85	85
Total Pads	168	146	124	100	84	68	52	44



**MOTOROLA**

MOTOROLA APPLICATION SPECIFIC INTEGRATED CIRCUITS



# CMOS Standard Cells

- 3 Micron Single Layer Metal Technology
- 2 Micron Double Layer Metal Technology

Cell based design offers you the same high performance, design flexibility and breadth of functions as a fully-customized integrated circuit, while simultaneously minimizing development time and cost. Key elements of the Motorola system include computer-aided design (CAD) tools, advanced process technologies, total technical support and a wide selection of cell functions in a state-of-the-art CMOS standard cell library. Unique complex digital functions such as a 68HC05 core, CRT Controller, memory and timers reside in the library. A deep selection of analog cells simplify interface tasks. Cell generators allow many functions to be tailored during the design cycle to meet specific configuration requirements.

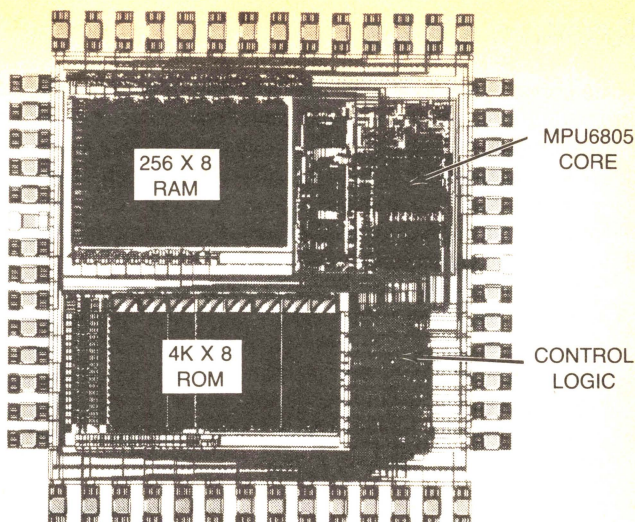
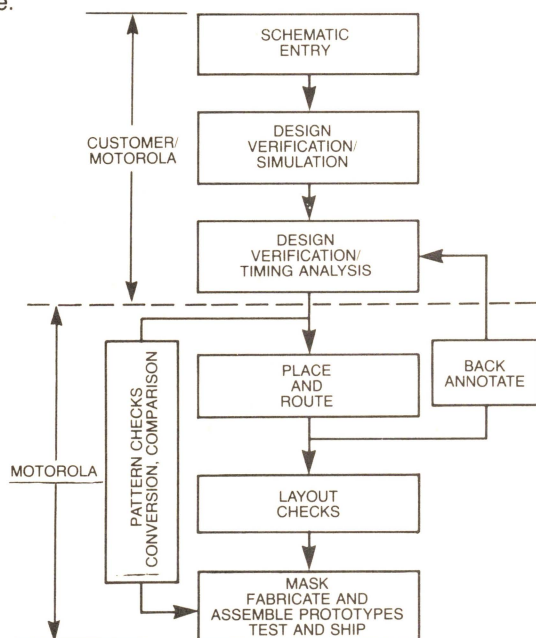
## Benefits

- Die size no larger than necessary; i.e., gate count no more than customer requirement.
- Implementation of application specific functions such as microprocessor core, memory, analog, and functional blocks.
- More flexibility to vary the performance of specific functions to optimize chip size.
- Ability to generate new cells on-the-spot using design automation tools, such as silicon generator/compilers.

## Development Tools

Design automation tools available to customers encompass Silicon Generation/Compilation, Timing Analysis and Design Verification, Layout Analysis and Test Generation.

Motorola provides for turnkey as well as interactive development procedures. For interactive designs the customer enters logic schematic and simulates the design on engineering workstations. Daisy, Mentor Graphics and Valid are fully supported. Motorola then commences with place and route.



Customized controller chip with memory and  $\mu$ p core (240 mils x 245 mils)

## 2 Micron Standard Cell Features

- Up to 20,000 equivalent gates
- Double layer metal 2-micron HCMOS technology
- Extensive analog offering
- 68HC05 core microprocessor
- CRTC-cathode ray tube controller
- Cell types optimized for speed and density
- Select Motorola standard products available as functional block "Generators":
  - UART, I/O Port, timer, prescaler
- Parameterized Memory
  - RAM (16 x 1 to 1K x 32)
  - ROM (128 x 1 to 8K x 16)
- Parameterized data path elements:
  - registers, adders, multiplexers, ALU, digital comparators, barrel shifters, counters, latches
- Second sourcing by NCR

## 3 Micron Standard Cell Features

- Up to 10,000 equivalent gates
- Single layer metal 3-micron HCMOS technology
- Extensive analog offering
- Comprehensive SSI/MSI Digital Cell Library
- Variety of packages — DIP, LCC, PLCC, PGA, SOIC, QUAD FLAT
- Parameterizable Memory
  - RAM (16 x 1 to 512 x 8)
  - ROM (128 x 1 to 2K x 8)
- Second sourcing by NCR

Design Features	3 $\mu$ SLM	2 $\mu$ DLM
Max Gate Equivalent	10000	20000
Max I/O and Power Pins	156	158
Max Gate Delay (ns)	3.3	2.4
Max Toggle Freq. (MHz)	20	50
Operating Voltage (Vdc)	+3 to +6*	+3 to +6*

\*Analog cells are specified at 3 or 5 volts.



MOTOROLA APPLICATION SPECIFIC INTEGRATED CIRCUITS



## Analog Cells

The comprehensive analog standard cells in the Motorola library can be combined with the digital cells to develop an application specific implementation suited to virtually any 8-bit (or less) application. The "soft macro" approach allows quick modification of existing analog designs; and, new designs can be tailored to meet circuit-unique requirements of proprietary data acquisition systems.

As part of Motorola's ASIC analog design strategy, many conventional circuit blocks are omitted since they are easily configured with our comprehensive primitives leaving the design flexibility and control in the hands of the designer.

Another special feature of these analog cells is the ability to run in low voltage mode (3 Volts) and they can also be put into a power down (sleep) mode.

## Analog Functions & Devices

### Functions:

- Analog Switch
- Band Gap Reference
- A/D Converter, 6-bit SAR
- A/D Converter, 6-bit Flash\*
- A/D Converter, 8/10-bit SAR\*
- D/A Converter, 8-bit\*
- DC-DC Converter\*
- Differential Line Driver\*
- Differential Line Receiver\*
- Comparator, P-Channel
- Comparator, N-Channel
- Comparator, low power
- Comparator, clocked
- Op Amp, general purpose (3)
- Op Amp, low power

- Oscillator\*
- PLL/VCO\*
- Phase Shifter\*
- RS232 Interface\*
- Switched Capacitive Filter
- Voltage/Current Converter

### Devices:

- Capacitor, general purpose
- Pad, analog input
- Pad, analog output
- Resistor, general purpose
- Resistor Divider, general purpose

\*Preliminary information

## Compiler Cells

Compilers are the group of parameterized functions that can be immediately customized to specific applications. The result is a reduced design time and die size with maximum chip performance and design accuracy. Most of Motorola's compiler cells have been produced through silicon compilation techniques to make efficient use of die area. The circuit designers that use these functions, however, do not have to become familiar with silicon compiler software. Motorola has incorporated the means to use these functions on supported CAE workstations, so the designer needs only to call up the appropriate symbol, specify the necessary parameters and "connect the wiring" of the schematic as with SSI or MSI functions.

The compiler functions are designed to be compatible with other digital, analog and special functions in the Motorola Standard Cell library. These cells are usable in both standard (5 Volt) and low voltage (3 Volt) modes.

### Datapath Elements:

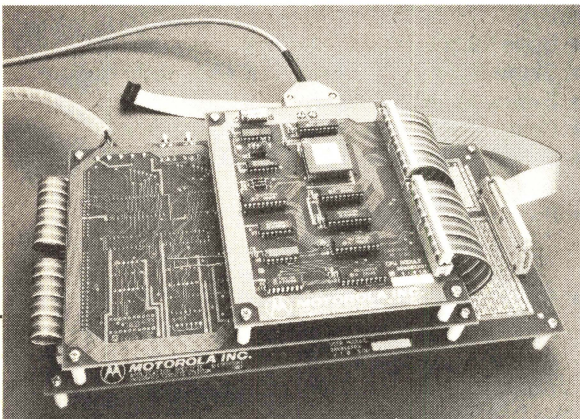
- Latch
- D-Register
- Comparator
- 3-State Buffer
- Counter
- Adder
- Multiplexer
- Register File 1R/1W
- Register File 2R/1W
- ALU
- Barrel Shifter
- Incrementer/Decrementer
- Parity Gen/Checker
- Inverter
- Serial Interface (SPI function)

### Peripherals:

- I/O Port
- PLA
- Prescaler
- RAM
- ROM
- Status/Control Register
- Timer
- UART (SCI function)

## System Emulation

### MPU6805 Evaluation Board (EVB)



### Features

- Economical Means of Evaluating Target Systems Incorporating the MPU6805 Core
- Includes Monitor/Debugging Firmware Program

The MPU6805 Evaluation Board (EVB) is designed to be a basic hardware and software development tool. The EVB enables the ASIC device designer to actually construct and debug a hardware model of a proposed device that incorporates the MPU6805 standard cell microprocessor core.

The hardware model "behaves" like (emulates) the proposed standard cell chip. This model can be used to interact with the real system for which it is designed. The emulator can run in real-time even though its internal timing may not be exactly like the final ASIC device.

In general, emulation is ideally suited for design tasks involving interaction with the devices outside of the ASIC device. It is therefore suited for both interactive controllers and complex combinational logic or state machines.

- Integral RS-232C Terminal I/O Port for User Interface to Terminals or Host Computers
- Contains Separate User Definable Wirewrap Board
- Provides Design Development Tools Including:
  - Start and Stop of the User Program
  - Examine or Change User Memory
  - Examine or Change Registers Within the Core Cell
  - Set Breakpoints in the User Program
  - Download Programs from Host Computer to User RAM



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MOTOROLA APPLICATION SPECIFIC INTEGRATED CIRCUITS



# BiMOS Macrocell Arrays

BiMOS merges the major technologies required to fabricate VLSI MOS and bipolar transistors on the same integrated circuit.

Combining high performance bipolar and MOS transistors on the same integrated circuit is extremely attractive to the VLSI system engineer. MOS transistors maintain an edge in packing density and ability to integrate large complex functions with high yields. In addition, CMOS circuits have inherent low power dissipation and large noise margins. The bipolar transistor has an advantage in switching speed, better

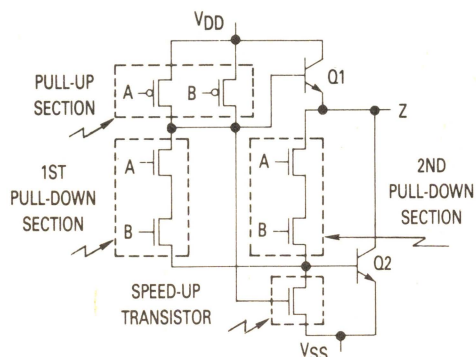
noise performance, superior analog performance, and greater current drive per unit area than a MOS transistor.

Motorola's BiMOS arrays combine these advantages within each I/O and internal cell.

When your semicustom array requires a different combination of performance characteristics than CMOS or bipolar can provide, Motorola BiMOS is the solution.

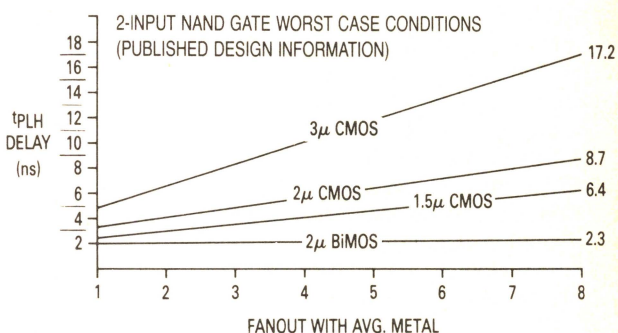
Unique I/O flexibility, high density, more speed and drive than CMOS, lower power than bipolar, and on-chip memory make innovative designs possible.

## BiMOS 2-INPUT NAND



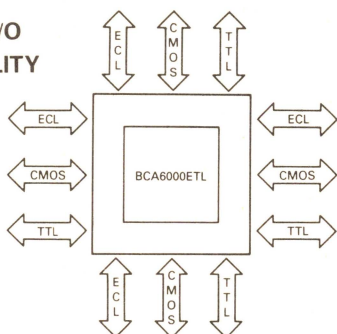
BIMOS BLENDS BIPOLAR WITH CMOS

## PERFORMANCE COMPARISON



BIMOS MAINTAINS PERFORMANCE BETTER THAN CMOS AS FANOUT INCREASES

## BiMOS I/O FLEXIBILITY



Each I/O cell may be personalized into a CMOS input or output or bidirectional, ECL input or output, or TTL input or output or bidirectional port.

### • CMOS I/O Compatibility

All inputs can be interfaced to CMOS logic levels with true CMOS 2.4 V thresholds.

### • High Drive TTL Outputs

TTL outputs are available in output only, bidirectional, or tri-statable, open collector and active pull-up configurations. The normal sink current in these configurations is 8 mA or 24 mA. Higher drives of 48 mA or 72 mA are obtained by paralleling output cells internal to the array.

### • ECL Options

Most BiMOS arrays are offered with an ECL 100K option that features approximately constant output levels over temperature. All ECL I/O may be chosen as 50 ohm 10KH or 100K.

## BiMOS (BCA) Macrocell Array Family

Features	BCA 700ETL	BCA 1800ETL	BCA 4000ETL	BCA 6000ETL	BCA 8000RAM	BCA 10000TTL
Max Gate Equivalent	704	1792	4032	6144	7500 + RAM	10080
Internal Cells	352	896	2016	3072	3960 + RAM	5040
I/O Ports*	44	92	136	202	228	228
Max Gate Delay (ns)	1.7	1.7	1.7	1.7	1.7	1.7
Max Toggle Freq. (MHz)	135	135	135	135	135	135
Output Drive (mA)	8 to 72	8 to 72	8 to 72	8 to 72	8 to 72	8 to 72
I/O Compatibility	TTL-CMOS-ECL				TTL/CMOS	TTL/CMOS
Power Dissipation (W)	Low power — varies with array utilization and output loading.					

\*Specific Input/Output configurations vary greatly based on package selection.



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# High Density CMOS Macrocell Arrays

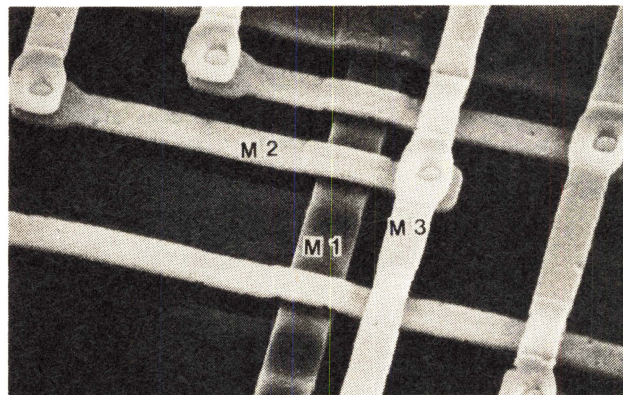
## The "MAX"

Built on a 1.0 micron, triple layer metal CMOS process (TRIM) the "MAX" family of arrays represents a significant advancement in microchip technology. By utilizing three layers of metal for routing in addition to power distribution, designers can achieve over 70,000 usable gates on a channelless architecture of minimum dimensions. The result is very high performance (subnanosecond loaded gates) combined with unprecedented I/O flexibility and density.

### Features

- 5,000 to 100,000 available gates
- Over 70% utilization
- Channelless sea of cells architecture
- 1.0 micron drawn gate length CMOS process
- Triple layer metal routing and power distribution
- 8 transistor fully utilizable primary cell
- 250 picosecond typical gate delay (F.O. = 1)
- Up to 48 mA drive
- Efficient memory implementation
  - RAM cells — 12 x 9 to 1K x 32
  - ROM cells — 12 x 9 to 1K x 32
- CMOS/TTL input compatible
- Comprehensive CAD support
- Up to 512 I/O cells available

The "MAX" redefines high density to be 1097 square microns per gate. Minimum dimensions are achieved while still allowing high speed cells to drive 1.0 pF loads (100 mils of metal and F.O. = 6) in 0.9 ns typical.

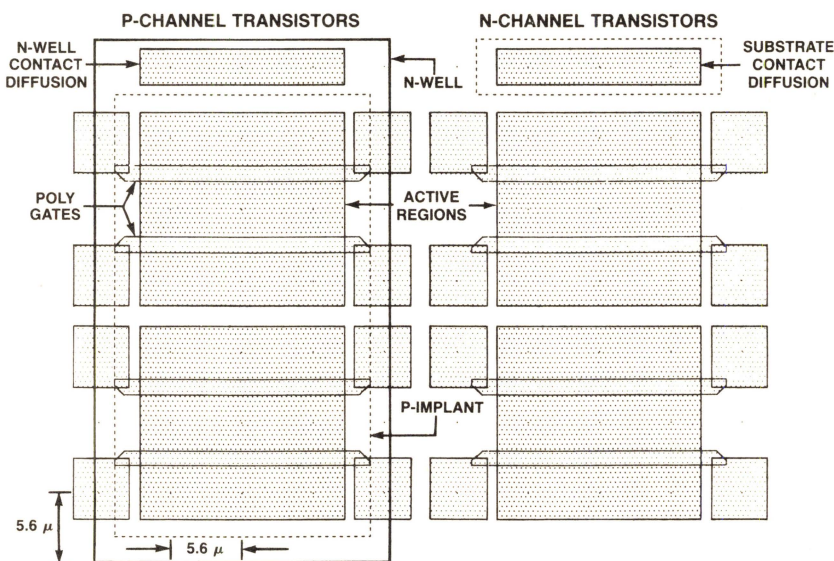


Triple layer metal routing improves utilization to record 75% on sea of cells architecture.

The "MAX" High Density Array Series

Array	# of Gates	# of I/O Pads	
		Wire Bond	TAB
HDC005	5,670	96	100
HDC008	8,208	108	130
HDC012	11,208	120	160
HDC016	16,416	136	204
HDC025	26,112	168	256
HDC031	31,290	180	280
HDC045	47,214	212	350
HDC062	63,900	240	410
HDC080	80,304	264	450
HDC100	104,832	300	512

### Primary Cell Layout



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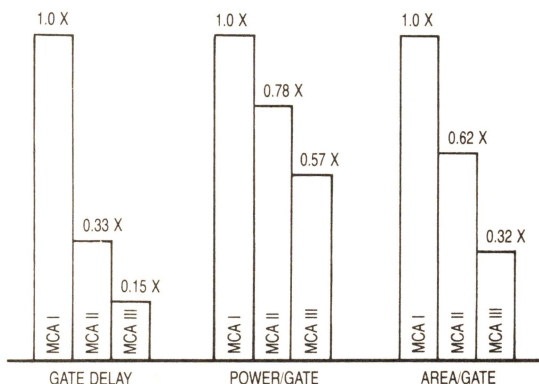


# MCA III — Third Generation ECL Arrays

Densities up to 10,000 equivalent gates combined with 100 picosecond typical gate delays make the MCA III family your logical choice in applications requiring the highest performance arrays.

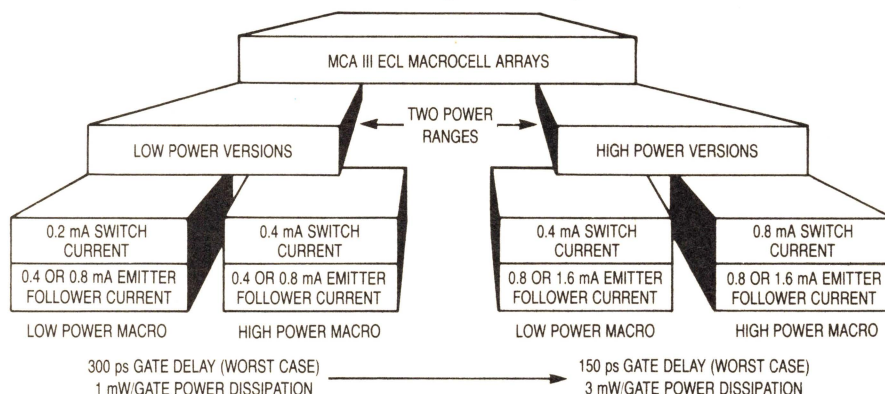
Third generation ECL arrays from Motorola offer twice the speed at less power per gate than previously available products. Initially offered in 10,000 gate density the family will expand to include smaller arrays as well as on-board memory.

**Performance Progression — 1st through 3rd Generation**



Features	MCA 1500ECL	MCA 3000ECL	MCA 7000ECL	MCA 7500RAM	MCA 10000ECL
Max Gate Equivalent	1500	3000	7000	7500 + RAM	10332
Major Macrocells	66	132	300	310 + RAM	414
I/O Ports	106	120	180	256	256
Input Cells	96	—	176	224	224
Output Cells	96	80	176	200	200
Max Gate Delay (ns) (high power)	0.15	0.15	0.15	0.15	0.15
Max Toggle Freq. (GHz)	1.2	1.2	1.2	1.2	1.2
Power Dissipation (W) programmable	3-6	8-15	10-20	10-30	10-30
Package Pin Count	132	149	235	289	289
Power Pins	26	28	48	33	33

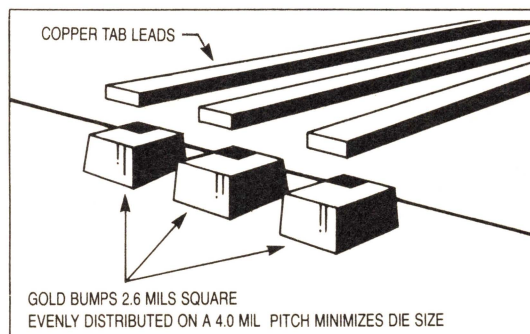
## Power Programmability



**Speed/Power Programmability** — allows the designer to choose from a range of four performance levels. CAD tools provide for selectable resistor implant options, current source values and output emitter follower currents. These features let each design operate at maximum performance and minimum power.

**Tape-Automated Bond (TAB)** — minimizes chip size while providing up to 256 signal lines and 33 power pins on higher density arrays. The TAB process allows the MCA10000ECL array to fit on a die measuring only 385 mils square.

## Tape Automated Bond Process



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# Modular Design System —

## Technology Independent Software guides design from schematics through testability.

### Modular CAE for Silicon Design

Motorola introduces ASIC design software for engineering workstations called the Modular Design System (MDS). The first two modules introduced are the *Design Verification Module* and the *Design Capture Module*. These CAD software modules support the Daisy and Mentor graphics engineering workstations. The Modular Design System provides engineers with a technology independent tool box that will handle today's gate array or cell-based designs and tomorrow's technologies as they become available. The MDS software allows capturing of a design using Motorola's symbol libraries to simulate the behavior of the design over commercial, industrial, automotive, and military temperature ranges, resimulate the actual performance of the design after physical layout, and perform rigorous timing checks and testability analysis prior to releasing the design.



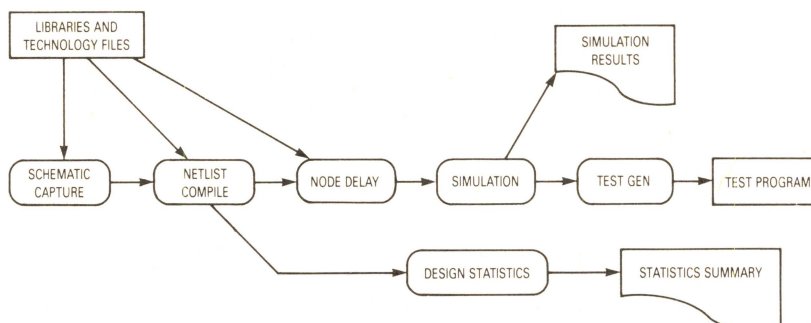
The *Design Verification Module (DVM)* is available on 1/4" cartridge tape, 8" and 5.25" floppy disc, or 1/2" reel tape and includes:

- 62A00 Series and standard cell libraries
- Netlist with electrical rules checking
- Design statistics package
- Selectable simulation delays
- Post simulation timing analysis tools
- Installation and verification utilities

Plus: RAM/ROM custom cell generator

The *Design Capture Module (DCM)* is available on 1/4" cartridge tape, 8" and 5.25" floppy disc, or 1/2" reel tape and includes:

- Above libraries, netlist, cell count and communications only



#### LIBRARIES AND TECHNOLOGY FILES

#### Includes CMOS Array and Standard Cell Libraries

- Compatible with Daisy, Mentor, and Valid Workstations
- Typical/Best/Worst Case Technology Models

#### NETLIST COMPILE

#### Netlist Compiler and Diagnostics

- Electrical Rules and Syntax Checks
- Produces TDL, Logcap, and EDIF 2.0 Netlist

#### NODE DELAY

#### Node Delay Calculation and Back Annotation

- Sophisticated Node Delay Calculation Equation
  - a. Selected Temperature, Voltage, and Process Variation
  - b. Estimated or Actual Wirelength Capacitance
  - c. RC Tree Analysis
  - d. Delay = Intrinsic + Rise/Fall Effects + Output Load
  - e. User Specified Output Loading
- Accurate Pin-to-Pin Multipath Delay Modeling (Mentor)

#### DESIGN STATISTICS

#### Design Statistics Package

- Gate and I/O Pad Utilization
- Design Rules Check
- Interconnect Analysis

#### TEST GEN

#### Test Generation and Timing Analysis

- Extracts and Verifies Tester Input Stimulus
- Checks for Bus Contention (Mentor) and Consistent Timing
- Generates Composite Best/Worst Case Simulation File
- Checks Output Timing Response for Testability
- Extensive Stimulus Diagnostics

Daisy is a trademark of Daisy Systems Corporation.

Mentor Graphics is a trademark of Mentor Graphics Corporation.



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# MOTOROLA SEMICONDUCTORS

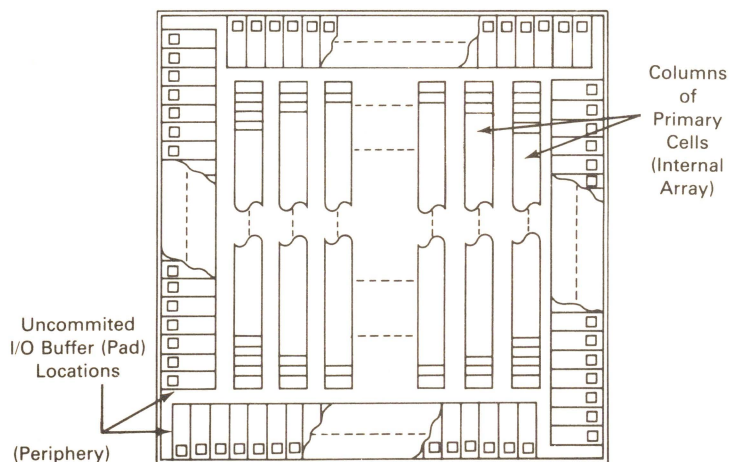
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

## HCA62A00 SERIES CMOS MACROCELL ARRAYS

The HCA62A00 series macrocell arrays are implemented in silicon gate, 2-micron drawn gate length, dual-layer metal interconnection and HCMOS technology. With equivalent gate counts of 600 to 8500, there is an HCA62A00 series array to meet nearly every commercial or military application. Full I/O flexibility, as well as completely flexible power, ground, and oscillator inputs make Motorola's HCA62A00 series a leader in the macrocell array field. Built with HCMOS technology, the HCA62A00 series arrays provide high-speed performance with low-power consumption. The extensive macrocell library and flexible I/O structure are designed to meet the market needs for both military and commercial high technology systems.

- Equivalent Gate Count Ranging from 600 to 8500 Gates
- 100% Programmable I/O Simplifies Board Layout
- Fully Programmable Power and Ground Pins
- Packaging from 16 DIP to 180 PGA in Plastic and Ceramic
- Outputs Can Be Paralleled Internally For Up to 24 mA Drive Without Disabling Input Pins
- 2-Micron Double Layer Metal HCMOS Technology
- 3KV ESD Protection
- CMOS/TTL Compatible I/O
- Separate I/O and Internal Power Buses
- Mil-Std-883C Class B Processing for Military Applications
- Supported by Complete CAD Development System
- Comprehensive Macro Library Including Oscillator with Clock Buffer
- Alternate Sourced

FIGURE 1 — TYPICAL LAYOUT OF AN HCA62A00 SERIES MACROCELL ARRAY



## HCA62A00 Series

HIGH PERFORMANCE  
TTL AND CMOS COMPATIBLE

MACROCELL ARRAYS

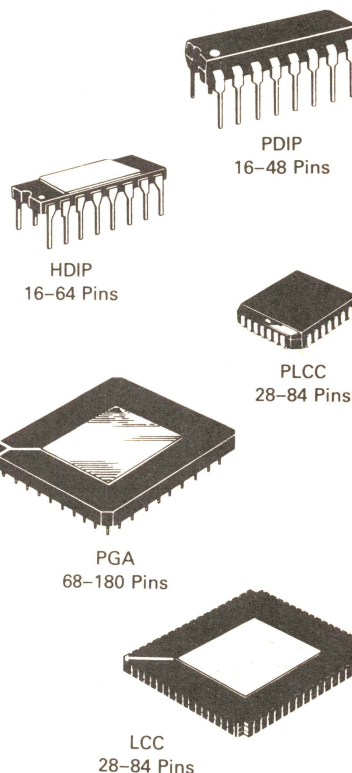


TABLE 1 — ARRAY FEATURES

Array	Primary Cells	Gate Equivalent	Available I/O Pads
HCA62A06	216	648	44
HCA62A10	319	957	52
HCA62A17	546	1638	68
HCA62A25	816	2448	84
HCA62A36	1200	3600	100
HCA62A50	1656	4968	124
HCA62A67	2236	6708	146
HCA62A85	2856	8568	168



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**Advance Information****MCA10000ECL MACROCELL ARRAY**

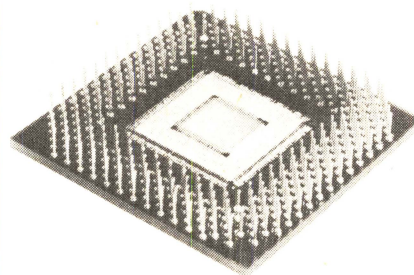
This specification establishes design and performance requirements for the MCA10000ECL, the first in a new series of third-generation, high performance bipolar arrays. Motorola's new MOSAIC III process provides the MCA10000ECL with the logic power of over 10,000 equivalent 100 picosecond gates on one integrated circuit chip. This advanced process technology, combined with innovative design, gives the array the performance and flexibility to meet the high-performance system needs of the future.

- Logic Function Fully Specified by User
- Metal Mask Programmable (Three Unique Masks)
- Over 10000 Equivalent Logic Gates
- Internal Gate Delays — 100 ps Typical
- Input Interface Cell Delays — 100 ps Typical
- Output Cell Delays — 200 ps Typical
- Flexible I/O Structure with up to 256 Signal Lines
- Programmable Speed/Power Levels (1 mW to 3 mW per gate)
- Series-Terminated ECL Outputs for Multichip Applications
- Three-Level Series Gated Macros
- Interfaces with MECL 10K/10KH or ECL 100K Logic Families
- Supported By Complete CAD Development System

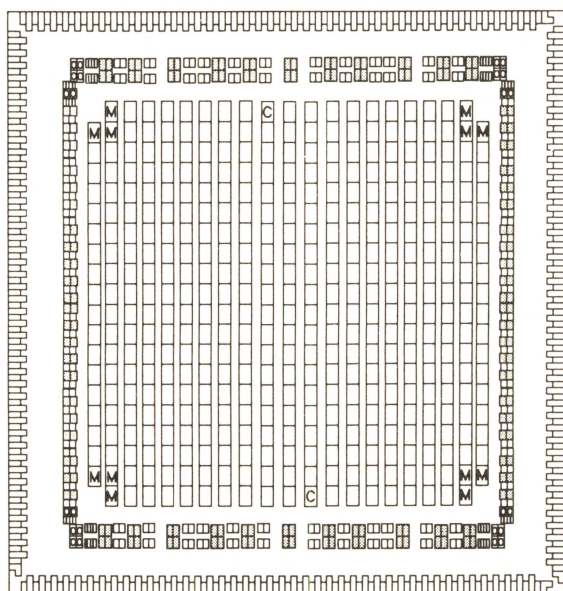
**MCA10000ECL**

**HIGH PERFORMANCE  
HIGH DENSITY  
MOSAIC III**

**ECL  
MACROCELL ARRAY**



**Multi-Layer PC Board Technology  
Pin-Grid-Array  
w/T.A.B. Assembly**

**FIGURE 1 — MACROCELL ARRAY LAYOUT**

M—Major (Internal) Cells  
Divisible into Four 1/4 C  
414 Total  
I—Input Interface Cells  
224 Total

O—Output Cells  
200 Total

C—Clock Generators  
2 Total

Over 1400 Routing Channels

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# SEMICONDUCTORS

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## Advance Information

### BCA6000ETL BiMOS ARRAY

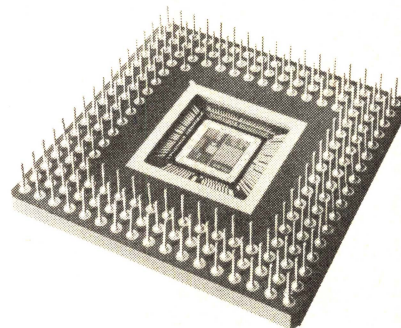
This specification defines design and performance requirements for the BCA6000ETL, first in a new generation of high performance TTL, ECL, and CMOS-compatible BiMOS semicustom arrays. The BCA6000ETL is built with epitaxial NPN transistors using polysilicon, oxide walled emitters for the switching and current drive of bipolar combined with the use of silicon-gate CMOS having silicided source, drain and gate for characteristic MOSFET power dissipation and enhanced speed characteristics. The logic power of over 6000 equivalent 2-input NAND gates is available for VLSI applications.

- Logic Function Specified by User (Three Unique Masks)
- Interfaces CMOS, TTL, MECL 10K/10KH and ECL 100K
- Input Receiver Delays: — 1.0 ns Typ CMOS  
— 1.3 ns Typ TTL  
— 3.0 ns Typ ECL
- Output Driver Delays: — 3.0 ns Typ CMOS (@ 50 pF)  
— 3.5 ns Typ TTL (8.0 mA @ 50 pF)  
— 1.1 ns Typ ECL (50  $\Omega$ )
- Internal Gate Delay: — 0.8 ns Typ (2-input NAND)
- Flexible I/O Structure: ECL, TTL or CMOS  
Receivers, Drivers or Bidirectional
- Supported by Complete CAD Development System

## BCA6000ETL

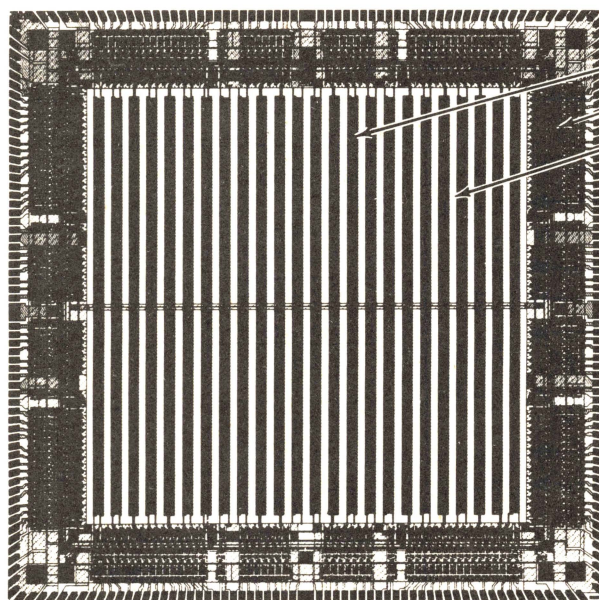
HIGH PERFORMANCE BiMOS  
TTL-ECL-CMOS  
COMPATIBLE

### MACROCELL ARRAY



169-Pin  
Pin Grid Array Package

FIGURE 1 — BCA6000ETL MACROCELL ARRAY LAYOUT



- 3072 Internal Cells
- 202 I/O Cells (periphery)
- Over 1400 Routing Channels
- 252 Pads (wire bond option)
- 322 Pads (TAB bond option)

Package Options	I/O Pins
254 PGA	202*
224 PGA	178
193 PGA	148
169 PGA	130
132 PGA	102

\*TAB bonding

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# MOTOROLA SEMICONDUCTORS

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## Advance Information

### MPU6805 CORE STANDARD CELL

This MPU6805 Cell is the microprocessor core extracted from the MC68HC05C4 microcomputer. The core consists of the CPU, ALU, clock logic, and the necessary registers. All other peripheral blocks can be implemented with standard cell logic blocks or as functional blocks.

#### HARDWARE FEATURES:

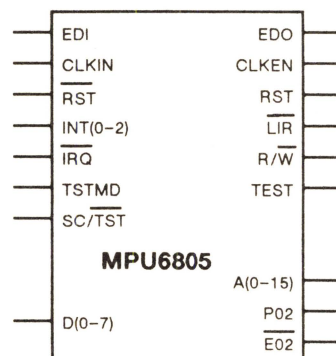
- HCMOS Technology
- Instruction Set Identical to the MC68HC05C4
- 64 Kb Addressing Capability
- 8-bit Architecture
- Up to 4 MHz Internal Bus, Operating Frequency @ 5V
- Supported with Hardware Evaluation Board
- Power Saving Stop and Wait Modes
- Fully Static Operation
- Self-Check Mode
- Master Reset and Power-on Reset
- Behavioral Level Simulation Model Available

#### SOFTWARE FEATURES:

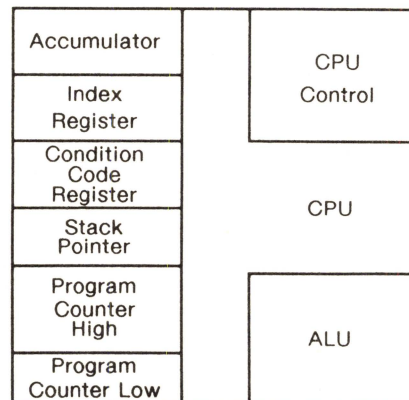
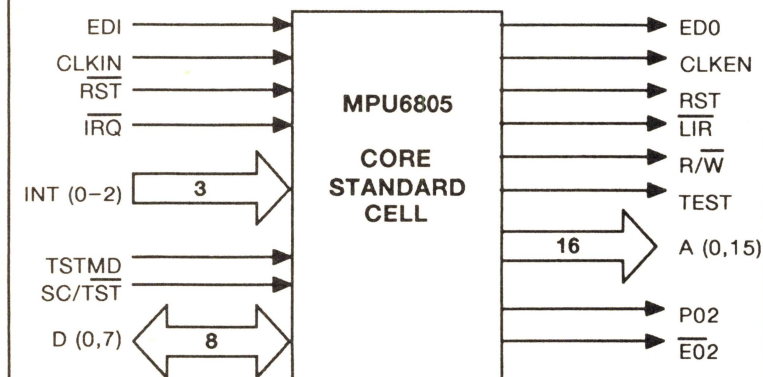
- Similar to MC6800
- 8 x 8 Unsigned Multiply Instruction
- Efficient Use of Program Space
- Versatile Interrupt Handling
- True Bit Manipulation
- Addressing Modes with Indexed Addressing for Tables
- Efficient Instruction Set
- Two Power-Saving Standby Modes
- Upward Software Compatible with M146805 CMOS Family

## MPU6805

### MPU6805 CORE STANDARD CELL



Standard Cell Symbol



Block Diagram



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# Future Directions

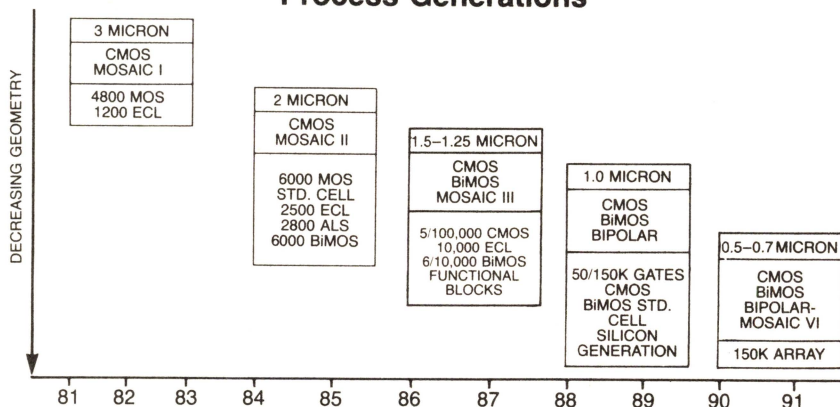
Motorola is dedicated to servicing the application specific market with CMOS, bipolar and merged technology products. Our leadership is based on superior customer service, fast cycle time and a balanced portfolio of defect free, cost effective products delivered on time and supported by state-of-the-art development tools.

1988 will be an exciting period as many new products and services become available.

- 1.0 micron, 100,000 gate density CMOS arrays with triple layer metal for high utilization.
- 1.5 micron standard cell with 8-bit and 16-bit microprocessor core cells.

- High density BiMOS arrays with CMOS power/density at bipolar speeds and on-board RAM.
- 30,000 equivalent gate ECL arrays with less than 100 picosecond speeds and imbedded 1.5 ns RAM.
- Technology independent EWS design software allowing simulations on either gate array or cell based designs.
- 512 I/O arrays in printed circuit board type PGA packages and on tape with T.A.B., for multichip applications.
- Achieve best in class for service with focused factory, quick turn around areas and captive fab/assembly/test.

## Process Generations



# Why Buy Motorola ASIC?

## Leading Global Based Manufacturer

- **Manufacturing** — In-house wafer fab through test  
— Dedicated quick turn facilities  
— Regional metallization and test  
—  $\pm 6$ -Sigma (3.4 PPM defects) Quality goal
- **Technology** — High density 1.0 micron CMOS  
— Submicron bipolar  
— 1.5 micron BiMOS  
— 3 layer metallization  
— Tape Automated Bonding
- **Experience** — Semicustom array business since 1972  
— Thousands of successful designs

## Comprehensive Design Automation Tools

- Technology Independent libraries for popular engineering workstations
- Cell generators/compiler for memory, data path elements and complex functional blocks

- Microprocessor core behavioral level simulation models combined with hardware emulation boards
- Dedicated mainframe for physical layout and DRC to assure first-pass working silicon

## Customer Design Support

- **Factory Engineering Services**  
— Technology and library development
- **Regional Design Centers**  
— Consultation; training; turnkey design
- **Local Application Engineering Assistance**
- As little or as much support as you need from passive monitor to 100% turnkey

## Alternate Sourcing

- CMOS arrays and Cell based semicustom
- Transparent libraries with analog and functional blocks
- Commercial and Military specifications

## Regional ASIC Design Support Centers

### U.S.A.

Los Angeles, California . . . (714)634-2844  
San Jose, California . . . . (408)985-0510  
Denver, Colorado . . . . . (303)337-3434  
Washington, DC/Maryland . . (301)577-2600  
Maitland, Florida . . . . . (305)628-2636  
Chicago, Illinois . . . . . (312)576-7800  
Burlington, Massachusetts . . (617)932-9700  
Detroit/Westland, Michigan . . (313)261-6200  
Minneapolis, Minnesota . . . (612)941-6800

Raleigh, North Carolina . . . (919)876-6025  
Philadelphia, Pennsylvania . . (215)443-9400  
Dallas/Ft. Worth, Texas . . . (214)699-3900

### International

Melbourne, Australia . . . . (03)566-7558  
Downsview/Toronto, Canada . . (416)497-8181  
Aylesbury/Bucks, England . . . (0296)395252  
Munich, Germany . . . . . (089)92720  
Vanves, France . . . . . (01)47360199

Kwai Chung, Hong Kong . . . . (0)223111  
Tel Aviv, Israel . . . . . 3-388-388  
Milan, Italy . . . . . (02)82201  
Tokyo, Japan . . . . . (03)440-3311  
Seoul, Korea . . . . . (02)554-5118  
Singapore . . . . . 65-294-5438  
Sweden, Solna . . . . . (08)830200  
Geneva, Switzerland . . . . . (022)991-111  
Taipei, Taiwan . . . . . (02)752-8944



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# When George Tobias and his design team needed every ASIC solution—from PLDs to gate arrays to standard cells—they called every ASIC company they needed: National.

It's the pressure every design engineer is familiar with. The pressure to squeeze more functionality into a smaller space.

That's why today's designs are requiring more ASIC solutions — and more than one type of ASIC solution in the same system.

And that's why more designers, like George Tobias and his team, are calling the one company that can meet all their needs in every ASIC category and can provide the full range of design tools, technical support, manufacturing capacity, and long-term commitment to ensure that those needs will be met on time, on budget, and in spec.

That one company is National Semiconductor.

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## NO ONE OFFERS YOU MORE DESIGN FLEXIBILITY

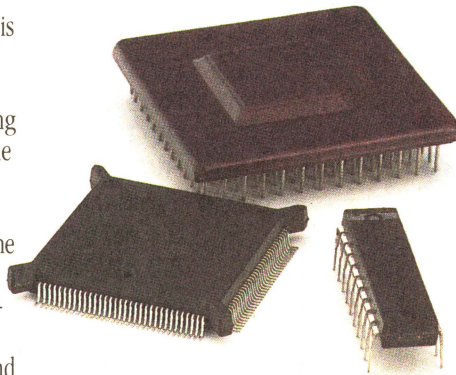
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National is the only company in the industry that can offer you a clear-cut upward-integration path from programmable logic devices to gate arrays to standard cells.

And we're the only company that can offer you a full range of capabilities *within* each of those categories.

**Programmable logic.** National has one of the most complete PLD listings available. We offer a variety of circuit types in a variety of process technologies, including bipolar, CMOS, and ECL.

**Gate arrays.** National has one of the most complete gate-array listings available. We offer a variety of densities, from 600 to



8700 equivalent gates, with higher densities in development, all with sub-nanosecond speeds.

**Standard cells.** National has one of the most complete standard-cell listings available. We offer a variety of functional blocks in a comprehensive and continually expanding cell library that will include logic, linear, memory, interface, microprocessor, and peripheral elements.

And you're not "stuck" at any level. Once you're comfortable with your programmable-logic design, for example, you can integrate the PLDs and glue logic into a gate array.

Or you can prototype your design as a gate array and then migrate it directly — with no re-engineering — to the full integration of a standard cell.

Or you can simply stay with your gate-array solution indefinitely, knowing that you can "tweak" your design relatively easily to maintain your competitive edge.

---

## NO ONE OFFERS YOU MORE DESIGN SUPPORT

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National is the only company in the industry that has committed the full magnitude of its semiconductor technology to the development of a complete cell library.

With a standard-product list that includes over 9,000 proven devices, we not only have more circuit-design experience, but we also have a broader base of circuit-design *resources* to help you implement your specific application.

And you can tap into those resources on all the leading workstations, including Daisy, Mentor, Valid, and Futurenet (IBM® PC).

---

## NO ONE OFFERS YOU MORE MANUFACTURING CAPACITY

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National is the only company in the industry that can offer you a complete, comprehensive, dedicated ASIC manufacturing capability.

In Santa Clara, California, we have a dedicated 4-inch quick-turn line that can give you rapid prototyping and small production runs.

And in Arlington, Texas, we have a world-class, 6-inch wafer-fab operation that meets Class-10 standards to give you high volume with high reliability.

So whether you're an experienced ASIC designer or you're just now ready to take that first big step toward higher integration, whether you're working with a single design or dozens, whether you need one device or millions, there's only one company that is as committed to your ASIC needs as you are.

National.

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ASIC Solutions  
P.O. Box 58090  
Santa Clara, CA 95052-8090



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# RAY1.25VG

## Ultra Low Power, Very High Speed, High Density HCMOS Gate Array Family

### Description

Raytheon's 1.25VG Series of silicon-gate HCMOS arrays combines exceptional performance with design flexibility using Raytheon's comprehensive CAD system.

Array complexities from 5670 to 20440 2-input gates are offered. I/O complexities range from 90 to 160 fully configurable pads. Raytheon's dual height row topology allows performance driven macrofunction compaction which exceeds VHSIC phase 1 clock speeds.

Raytheon's proven and fully integrated set of CAD design tools produce error-free designs while minimizing circuit turnaround time. Raytheon engineering workstations and remote access to the CGA design system provide complete verification and flexibility for customer design development.

### Features

- Production proven process
- VHSIC — Phase 1 compatibility including radiation hardening
- Symmetrical switching, edge delays
- Densities
  - RVG5 — 5670 gates, 90 I/Os
  - RVG10 — 10360 gates, 118 I/Os
  - RVG15 — 14640 gates, 142 I/Os
  - RVG20 — 20440 gates, 160 I/Os
- Typical array performance
  - 0.4 nS unloaded inverter delay
  - 8.0  $\mu$ W/MHz typical (45% of comparable devices)
- 250 MHz flip-flop frequency
- Latch-up free operation
- Extensive macrocell and macrofunction library
- TTL/CMOS I/O compatibility
- High output drive capability — 12 mA
- Electrostatic discharge protection
- Military and commercial operating temperatures
- Multiple packaging options — pin grid arrays, DIPs, flatpacks, leaded and leadless chip carriers
- Programmable macrocell drive

### Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VI	-0.3 to VDD +0.3	V
DC input current	II	$\pm 10$	mA
Storage temperature range	TSTG	-65 to +125	$^{\circ}$ C

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# RL7000 Series Silicon-Gate HCMOS Logic Arrays

## Features

- Silicon-gate  $2.0\mu$  (drawn) HCMOS technology
- Speeds higher than 74S TTL —  $1.4\text{nS}$  for a 2-input NAND gate with interconnection,  $T_A = 25^\circ\text{C}$ , fanout = 2,  $V_{DD} = 5\text{V}$
- Optimal block structure of 2N and 2P transistors
- Choice of eight array sizes ranging from 880 to 10,013 blocks
- Pad counts ranging up to 232
- Fully supported by LDS™ (LSI Design System), Daisy LOGICIAN\*, Mentor Graphics IDEA 1000\*, Valid Logic SCALDSsystem\* and FutureNet Dash-1 Schematic Designer\* systems
- Extensive macrocell and macrofunction libraries
- All non-power pads configurable as inputs, outputs or bidirectional I/O
- TTL/CMOS I/O compatibility
- High output drive capability — 12mA under worst case commercial conditions
- All inputs and outputs protected from over-voltage and latch-up
- RL7320Q evaluation device available
- Commercial and military operating temperature ranges
- Full military capability
- Multiple package options — LCCs, PGAs, leaded CCs, flatpacks, DIPs and custom packages

- Fully compatible with LSI Logic Corporation's LL7000 Series on an alternate source basis

## General Description

Raytheon's RL7000 Series of Silicon-Gate HCMOS Logic Arrays exhibits bipolar speeds, while at the same time, offers low power consumption, high noise margins, and ease of design of HCMOS. The RL7000 series is implemented in silicon-gate  $2\mu$  drawn gate length, dual-layer metal interconnection technology. A range of complexities from 880 to 10,013 blocks is offered; each block is equivalent to a 2-input NAND or NOR gate. Maximum pad counts range up to 232 with a maximum of 216 I/O pads.

The speed and range of block counts available in the RL7000 series make it ideal for LSI and VLSI implementation of a variety of high-performance functions. The high-density members of the series can be used for VLSI implementation of complete high-performance subsystem architectures such as intelligent special-purpose processors or multi-function controllers. The low block count members can be used for the replacement of high-speed logic such as Schottky TTL or even 10K ECL. The intermediate members can be used for high-performance dedicated peripheral controllers, intelligent support functions, etc.

## Product Description

The RL7000 series of arrays is manufactured using an advanced  $2\mu$ , oxide-isolated silicon-gate HCMOS fabrication process. The use of short channel lengths, thin gate oxides and two levels of metal interconnection provides bipolar speeds.



# CGA40E12, CGA70E18 High Density Low Power ECL Gate Array Family

## Features

- Superior performance, lower power, and higher density than existing ECL arrays
- Bipolar Integrated Technology (BIT1) process
- Densities  
CGA70E18 — 12540 equivalent gates  
CGA40E12 — 8001 equivalent gates
- Array performance  
300 pS (typical gate)  
300  $\mu$ W (typical gate)  
Speed-power product < 0.1 pJ  
Toggle frequency: 1.2 GHz (typical)  
Typical chip power dissipation: 3 to 5W
- Programmable internal drives
- Interface: TTL, ECL (10K, 10KH, 100K), ETL
- I/O counts  
CGA70E18 — 176  
CGA40E12 — 120
- Comprehensive, proven, fully integrated CAD system
- Commercial and military operating temperature ranges
- Mil-Std-883, classes B and S screening and qualification available

## Description

Raytheon's ECL gate array family combines exceptional performance with design flexibility using Raytheon's comprehensive CAD system. The high speed, low power performance is derived from the efficient design and unique BIT1 ECL process developed by Bipolar Integrated Technology, Inc. The BIT1 process, based on 2-micron lithography and polysilicon self-aligning techniques, produces a transistor

size that results in power dissipation one-tenth those of conventional ECL gates at comparable propagation delays.

Raytheon's contiguous row topology allows the greatest possible compaction of macrocells and macrofunctions. The very high density of the array is the result of the utilization of ultrasmall 14  $\mu$ m<sup>2</sup> bipolar transistors and 4  $\mu$ m metal pitch interconnects. Full utilization of the array is achieved through the ability to route over unused component sites and the placement flexibility afforded by the contiguous row topology. Implementation of the customer design requires four personalization masks: contact, first metal, via, and second metal.

Customers can choose from ECL (10KH, 100K, 10K military), TTL and ETL interface options. A 229 PGA with cavity down construction is offered for the 70E18 which reduces the junction to case thermal resistance to less than 0.5 °C/W. A similar 149 PGA is offered for the 40E12 array. An extensive library of array core macrocells is available with low, medium, high, and wire-OR drive options.

Raytheon's proven and fully integrated set of CAD design tools produce error-free designs while minimizing circuit turnaround time. Raytheon engineering workstations and remote access to the CGA design system provide complete verification and flexibility for customer design development.

## Absolute Maximum Ratings

Storage Temperature	..... -55°C to +150°C
Maximum Junction Temperature	..... 150°C
ECL Continuous Supply	
Voltage	..... -7.0 to +0.5V
ECL Input Voltage	..... Gnd to V <sub>EE</sub>
ECL Output Current	
(Continuous)	..... -50 mA
(Surge)	..... -100 mA
ECL Input Current	..... +2 mA



# RLA Linear Macrocell Array

## Device Features

### General

- Dual-layer metal for ease of interconnect routing and maximum array utilization
- Binarily weighted thin-film resistors having superior performance and ease of use
- Bipolar transistors arranged as:
  - User-configurable gain cells of 10 transistors each
  - Small NPN transistors
  - Small PNP transistors
  - 200mA NPN transistors
- Wide supply voltage range — 2V to 32V ( $\pm 1V$  to  $\pm 16V$ )
- Available in LCC, PLCC and other packages
- Die size —
  - 135 mils  $\times$  95 mils (RLA80)
  - 148 mils  $\times$  119 mils (RLA120)
  - 189 mils  $\times$  123 mils (RLA160)

### Component

- Resistors:
  - $\pm 10\%$  absolute resistor tolerance (max)
  - $\pm 1\%$  resistor matching (identical values)
  - $\pm 100$  ppm per  $^{\circ}C$  absolute resistor tempco
  - $\pm 5$  ppm per  $^{\circ}C$  resistor tempco tracking
- With macro gain cell in op amp configuration:
  - Slew rates to 5 V/ $\mu$ S (2 V/ $\mu$ S in unity gain)
  - Unity gain bandwidth to 20 MHz
  - 1 mV input offset voltage (5 mV max)
  - 30 nA input bias current
  - 1 nA input offset current
  - 80 dB dc voltage gain into 10 k $\Omega$  load
- With macro gain cell in comparator configuration:
  - Propagation delay to 300 nS
  - 1 mV input offset voltage (5 mV max)
  - 1 mA output sink current (min)
- Transistors:
  - Breakdown voltage: 32V
  - 500 MHz NPN  $F_T$
  - 4 MHz PNP  $F_T$
  - NPN  $H_{FE} = 100$  (min)
  - PNP  $H_{FE} = 30$  (min)

## Device Description

RLA ICs are primarily made up of op amp/comparator cells and thin-film resistors. Other components are included to help support these cells and resistors in creating a wide variety of application circuits. The user integrates op amps, comparators, precision resistors, and NPN/PNP transistors into a specific design. The final result is a monolithic IC containing feed-back amplifiers, filters, one shots, and other circuits, combined together to attain high-level functions.

### IC Processing

Wafers are manufactured using Raytheon's standard bipolar planar process at Raytheon's own Mountain View, California site. This process, which has been well characterized, is used to make many military and commercial IC products. The use of this process has two advantages: it allows building military grade parts and it allows any semicustom design to be easily converted to a full custom design. This provides a trouble-free transition from low volume to high volume production, with semicustom devices turned around quickly and low-cost, full custom devices arriving later.

The process uses bipolar transistors to form op amps capable of withstanding  $\pm 16V$  supply voltages.

### RLA Series Comparison Chart

	RLA80	RLA120	RLA160
Gain Cells	8	12	15
Large NPN	3	4	4
Small NPN	46	39	43
Small PNP	19	16	10
Resistors	95	196	240
Bonding Pads	24	24	44
Voltage Reference	No*	No*	Yes

\*May easily be configured.

## Gate Array Product Listing

MAXIMUM <sup>1*</sup> CLOCK FREQUENCY	RAM/ ROM BITS	SUPPLY VOLTAGE RANGE	TECH- NOLOGY	PROCESS GEOMETRY	LAYERS OF INTER- CONNECT	INTERNAL STRUCTURE	AVAILABLE PACKAGES	TEMPERATURE RANGES
67 MHz	0	5 V $\pm$ 10%	EPL Med. Power	5 $\mu$	2 + VIA	80 Pre-Characterized Cells	14, 16, 18, 24, 28, 40, 48, 50 DIP 68, 84 LCC	- 55°C to + 125°C
50 MHz	0	5 V $\pm$ 10%	EPL Low Power	5 $\mu$	2 + VIA	80 Pre-Characterized Cells	14, 16, 18, 24, 28, 40, 48, 50 DIP 68, 84 LCC	- 55°C to + 125°C

RAM BITS	RAM ACCESS TIME (MAX.)	SUPPLY VOLTAGE RANGE	TECHNOLOGY	INTERNAL STRUCTURE	AVAILABLE PACKAGES	JUNCTION TEMPERATURE RANGE
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	28, 44 PLCC/24 DIP	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	28, 44 PLCC/24 DIP	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	64 PGA/68 QFP 28, 44, 68 PLCC 24 DIP	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	64 PGA/68 QFP	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	64 PGA/68 QFP 28, 44, 68 PLCC	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	64 PGA/68, 84 QFP	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	144 PGA/84 QFP 84 PLCC	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	144 PGA/84 QFP	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	144 PGA/68, 84, 148 QFP/84 PLCC	30°C to 125°C
0		10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	144 PGA/84, 148 QFP	30°C to 125°C
320 User- Configurable	5 ns	10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	144 PGA/84, 148 QFP	30°C to 125°C
1280 (16 Blocks of 5 $\times$ 16)	6 ns	10KH: - 5.2 V ( $\pm$ 5%) 100K: - 4.5 V ( $\pm$ 5%)	CML/ECL	Pre-Characterized Cell	144 PGA/84, 148 QFP 84 PLCC	30°C to 125°C



## Gate Array Product Listing

PART NUMBER	NUMBER OF GATES	NUMBER OF I/Os	FIXED INPUTS	OUTPUT CURRENT (mA)	PROPAGATION DELAY TYP	MAX	GATE POWER TYP	MAX	MAXIMUM POWER DISSIPATION
<b>COMPOSITE CELL LOGIC (CCL)</b>									
CCL	Up to 450	Variable	O	8, 24, 80mA	$2_{FO=1}$	4.5	3.3mW	5.6mW	1.7W @ 300 Gates
CCL	Up to 650	Variable	O	8, 24, 80mA	$3_{FO=1}$	5.5	1.5mW	2.6mW	0.8W @ 300 Gates

PART NUMBER	NUMBER OF GATES	NUMBER OF I/Os	I/Os COMPATIBILITY		PROPAGATION DELAY TYP	MAX	GATE POWER TYP	MAX	MAXIMUM CLOCK FREQUENCY
<b>ADVANCED CUSTOMIZED ECL (ACE)</b>									
ACE2T00	250	32	10KH TTL	100 K	250 ps	350 ps			
ACE2100	250	32	10KH TTL	100 K	325 ps	450 ps			
ACE6T00	660	58 (30 inputs) (28 I/Os)	10KH TTL	100 K	250 ps	350 ps	2.3mW	2.8mW	600 MHz
ACE6LP00	660	58 (30 inputs) (28 I/Os)	10KH TTL	100 K	325 ps	450 ps	1.4mW	1.7mW	450 MHz
ACE9T00	910	58 (30 inputs) (28 I/Os)	10KH TTL	100 K	250 ps	350 ps	2.3mW	2.8mW	600 MHz
ACE9LP00	910	58 (30 inputs) (28 I/Os)	10KH TTL	100 K	325 ps	450 ps	1.6mW	1.7mW	450 MHz
ACE14T00	1750	96	10KH TTL	100 K	250 ps	350 ps	2.3mW	2.8mW	600 MHz
ACE14LP00	1750	96	10KH TTL	100 K	325 ps	450 ps	1.4mW	1.7mW	450 MHz
ACE22T00	2700	128	10KH TTL	100 K	250 ps	350 ps	2.3mW	2.8mW	600 MHz
ACE22LP00	2700	128	10KH TTL	100 K	325 ps	450 ps	1.4mW	1.7mW	450 MHz
ACE1320	1650	112	10KH TTL	100 K	350 ps	500 ps	2.3mW	2.8mW	450 MHz
ACE30T00	1450	128	10KH TTL	100 K	250 ps	350 ps	2.3mW	2.8mW	600 MHz

\*At room temperature.

\*\*LCC = Leadless Chip Carrier.

**NOTE:**

1. Typical frequency for toggle flip-flop without set and reset (all limits based on 5V supply except ACE).

# Signetics

## SemiCustom Products

# ACE 200/600/900/1400/ 2200

## Advanced Customized ECL (ACE) Master Slice Logic Arrays

### Product Specification

### DESCRIPTION

The Signetics Advanced Customized ECL (ACE) family of products provides the user with a cost-effective technology, futuristic speeds, and other high-performance alternatives for the design of LSI-based systems. Basic cell designs are implemented with Emitter Coupled and Current Mode Logic (ECL/CML) to guarantee the very best compromise between speed, power, and interface capabilities (see Figure 1 and the Technical Summary that follows).

The ACE Family offers five logic arrays with densities of 250/660/910/1750 and 2700 equivalent gates, which are available in either high-speed (Turbo ACE) or reduced power (Low-Power ACE) versions.

### FEATURES

	<u>Turbo</u>	<u>Low Power</u>
Geometry	2 micron	2 micron
Equivalent gate delay	250ps	350ps
Flip-flop toggle frequency	600MHz	400MHz
Power per gate	2.5mW	1.6mW

- Expandable macro library
- Mask-selectable rise and fall time for output interface cells
- 10KH, 100K ECL and TTL compatible
- 25 $\Omega$  and 50 $\Omega$  drive capability
- Pin grid and quad Cerpack packages

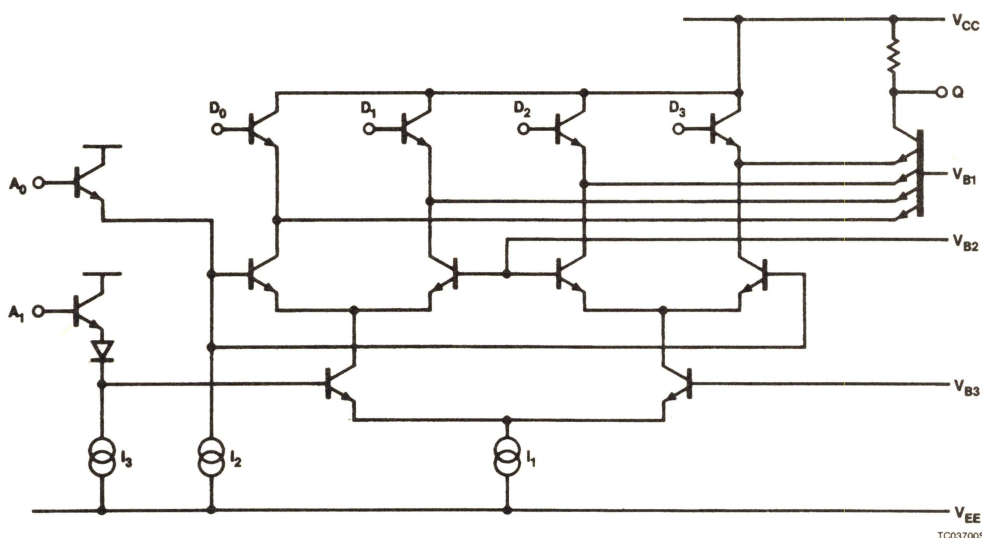


Figure 1. Typical ACE Cell Using Three-Level Series Gating (4-to-1 Multiplexer)



### DESCRIPTION

The Signetics Advanced Customized ECL (ACE) family of products provides the user with a cost-effective technology, futuristic speeds, and other high-performance alternatives for the design of LSI-based systems. Basic cell designs are implemented with Emitter Coupled and Current Mode Logic (ECL/CML) to guarantee the very best compromise between speed, power, and interface capabilities (see Figure 1 and the Technical Summary that follow).

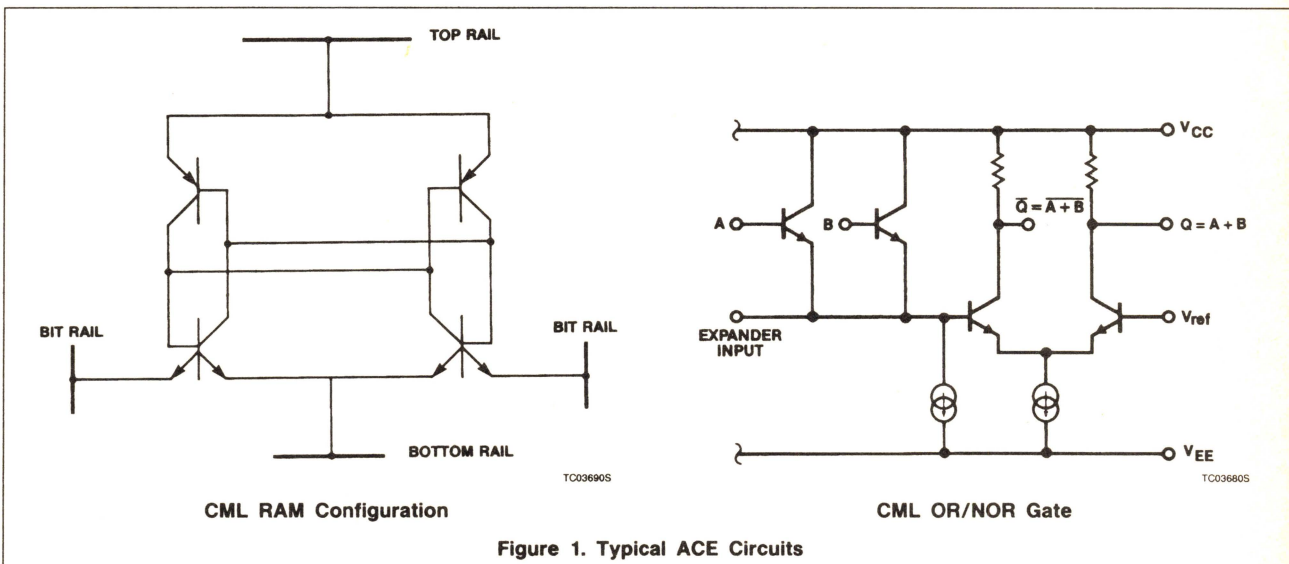
The ACE Family offers five logic arrays with densities of 250/660/910/1750 and 2700 equivalent gates, which are available in either high-speed (Turbo ACE) or reduced power (Low Power ACE) versions.

The two arrays with RAM-on-chip are described in this specification. The speed power product for all arrays range from 0.6 to 3 picojoules allowing for heatsink cooling.

### FEATURES

	30T00	30T20
Geometry	2 micron	2 micron
Equivalent gate delay	250ps	250ps
RAM	1280-bits	320-bits
Logic density	1450 gates	2410 gates
RAM access time (typ.)	2.8ns	2.8ns
Flip-flop toggle frequency	600MHz	600MHz

- Expandable macro library
- Mask-selectable rise and fall time for output interface cells
- 10KH, 100K ECL and TTL compatible
- Unrestricted bidirectional I/O's
- 25Ω and 50Ω drive capability
- Pin grid or quad Cerpack packages



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### Application Specific Products (IC's)

S-MOS Systems and our affiliate, Seiko Epson, form a team that is one of the world's technology leaders in Application Specific Integrated Circuits. Advanced design and manufacturing capabilities enable us to provide fast turn-around on prototypes and quickly ramp to volume production with high-performance, high-reliability products. We currently offer:

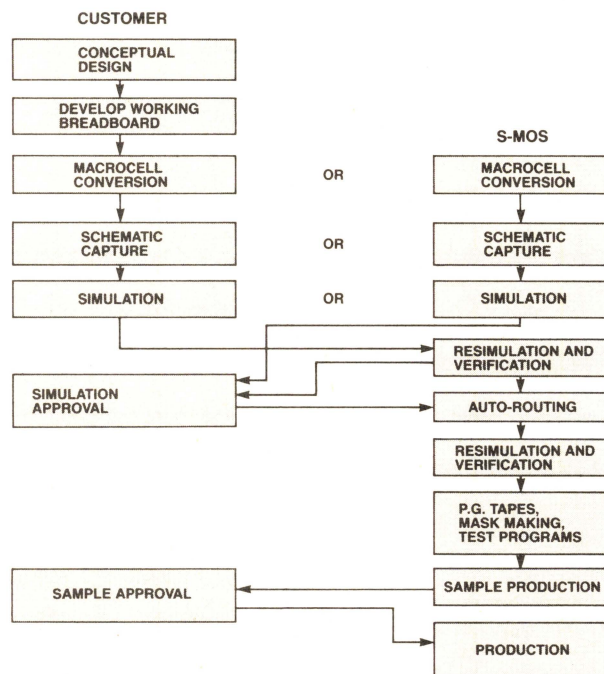
- SLA Series Gate Arrays:
  - SLA 5000—3 micron dual-layer metal (2.15 ns delay), 413 to 3082 gates (not recommended for new designs)
  - SLA 6000—2 micron dual-layer metal (1.3 ns delay)
  - SLA 7000—1.5 micron dual-layer metal (0.65 ns delay), 2232 to 16250 gates
  - SLA 8000—1.2 micron dual-layer metal (0.52 ns delay), 5904 to 38500 gates
  - SLA 700B—derivative of SLA 7000 with 24 mA drivers
  - SLA 100L—derivative of SLA 7000 with 1.0 to 6.0 volt operation
- SSC Series Standard Cells: SSC 1000—1.8 micron dual-layer metal (0.72 ns delay), up to 14,000 gates

In the near future\*, we will also provide:

- SLA Series Gate Arrays:
  - SLA 9000—0.8 micron dual-layer metal
  - SLA 800B—1.2 micron derivative of SLA 8000 with BiCMOS output drivers
  - SLA 2000—1.2 micron with BiCMOS internal cells and I/O
  - SLA 800E—SLA 8000 derivative  
Up to 130,000 gates
- SSC Series Standard Cell:
  - SSC 2000—1.8 micron low voltage, low power
  - SSC 3000—1.2 micron dual layer metal

\*Consult S-MOS for availability.

### ASIC Design Implementation





### Gate Arrays

S-MOS Systems presently offers 4 families of CMOS Gate Arrays and two special purpose derivative families to satisfy virtually any design needs.

All series are made up of cells that functionally emulate the familiar 74LS and HCMOS families of SSI/MSI integrated circuits. This makes it easy to convert existing discrete designs and breadboards to gate array designs using the S-MOS Systems cell libraries.

#### Features

- "Hard" MSI Macrocells for fully characterized AC performance
- High speed silicon gate CMOS technology
- TTL and CMOS I/O compatible
- High output drive capability (up to 24mA/pad in SLA 700B)
- Gate densities from 413 to 38500 gates
- I/O ports from 46 to 218
- Large package selection, including DIP, Flat Pack, PLCC, PGA
- Variety of design systems, including Daisy, Mentor and PC Based Systems using FutureNet, OrCAD and ViewLogic

### SLA 5000 Series (Not recommended for new designs)

Parameter	Series				
	SLA 5040	SLA 5080	SLA 5120	SLA 5210	SLA 5300
Gates (2-input Nand)	413	790	1264	2140	3082
Technology	Si-CMOS 2 layer metallization				
I/O level	TTL, CMOS				
Delay time (Internal gate)*	2.15 ns				
Total ports for I/O (Terminals only for input port)	46 (8)	60 (8)	72 (8)	90 (6)	108 (8)
Output mode	Normal, open-drain, 3-state, bi-directional				
Operating temperature	0°C to +70°C				

\*Typical 2-input Nand 1mm interconnect

### SLA 6000 Series

Parameter	Series							
	SLA 6050	SLA 6080	SLA 6140	SLA 6170	SLA 6270	SLA 6330	SLA 6430	SLA 6620
Gates (2-input Nand)	513	820	1394	1746	2667	3312	4342	6206
Technology	Si-CMOS 2 layer metallization							
I/O level	TTL, CMOS							
Delay time (Internal gate)*	1.3 ns							
Total ports for I/O (Input only port)	48 (6)	60 (6)	74 (6)	82 (6)	100 (6)	110 (6)	126 (6)	154 (8)
Output mode	Normal, open-drain, 3-state, bi-directional							
Operating temperature	0°C to +70°C							

\*Typical, 1 unit load + 100 mils of aluminum interconnect.

### SLA 7000 Series

Parameter	Series					
	SLA 7220	SLA 7340	SLA 7490	SLA 7620	SLA 7800	SLA 790S
Gates (2-input Nand)	2232	3432	4900	6210	8000	16250 <sup>2</sup>
Technology	Si-CMOS 2 layer metallization					
I/O level	TTL, CMOS					
Delay time (Internal gate) <sup>1</sup>	t <sub>PLH</sub> 0.60ns, t <sub>PHL</sub> 0.65ns					
Total ports for I/O (Terminals for power only)	82 (8)	104 (8)	128 (8)	150 (8)	170 (8)	188 (8)
Output mode	Normal, open-drain, 3-state, bi-directional					
Operating temperature	0°C to +70°C					

<sup>1</sup>Typical 2-input Nand with fan out of 1 and 1mm of interconnect

<sup>2</sup>Sea of gates used for SLA 790S only

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### SLA 8000 Series

Parameter	Series					
	SLA 827S	SLA 847S	SLA 872S	SLA 8B3S	SLA 8F0S	SLA 8J3S
Gates (2-input Nand)	5304	9416	14336	22680	30000	38550
Technology	Si-CMOS 2 layer metallization, sea of gates					
I/O level	TTL, CMOS					
Delay time (Internal gate) <sup>1</sup>	$t_{PLH}$ 0.46ns, $t_{PHL}$ 0.50ns					
Total ports for I/O (Terminals for power only)	78 (8)	104 (8)	132 (8)	164 (8)	190 (8)	218 (8)
Output mode	Normal, open-drain, 3-state, bi-directional					
Operating temperature	0°C to +70°C					

<sup>1</sup>Typical 2-input Nand with fan out of 1 and 1mm of interconnect

### Standard Cell

S-MOS Systems presently offers the SSC 1000 family of 1.8 micron dual layer metal standard cells. This family is intended primarily for direct conversion from SLA 7000 gate arrays, and therefore, shares most of the SLA 7000 cell library. Designs with up to 14,000 gates and 188 I/O pads are attainable with this family, but while new designs are certainly possible using the SSC 1000, most customers will prefer the flexibility of C.C. Custom for that purpose.

### Compiled Cell Custom

CC Custom is S-MOS' proprietary cell-based custom design process that is faster and more cost-effective than full custom. With this system, S-MOS engineers can develop large, functional custom blocks for customers, then implement them, along with logic, on a single chip.

The logic can be captured and simulated at your own site with S-MOS' LADS software. The logic is then combined with the custom blocks and routed using our timing-driven place-and-router. This software simulates the entire circuit, place-and-routes it, resimulates, and re-place-and-routes. This process continues until all paths meet the original pre-route timing.

The entire process through PG-tape is complete at our facility in San Jose, California. Process technology includes our 1.8, 1.5 and 1.2 micron drawn CMOS processes.

The S-MOS CC Custom Cell library is constantly expanding and currently includes microprocessor core cells, peripheral cells, and RAM and ROM blocks. For current availability of a particular macro cell, contact your local S-MOS representative or the S-MOS ASIC (Marketing) department.

### Electrical Characteristics (All ASIC Families)

( $V_{DD} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )<sup>\*</sup>

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{OH}$	High level output voltage	$V_{DD} = 4.75V$ $I_{OH} = -6mA$	2.4	—	—	V
$V_{OL}$	Low level output voltage	$V_{DD} = 4.75V$ $I_{OL} = 6mA$	—	—	0.4	V
$V_{IH}$	High level input voltage	$V_{DD} = 5.25V$	2.0	—	—	V
$V_{IL}$	Low level input voltage	$V_{DD} = 4.75V$	—	—	0.8	V
$I_L$	Input leakage current	—	-1	—	1	$\mu A$

<sup>\*</sup>Wider power supply tolerance and wider temperature range available. Consult S-MOS Systems for more information.



### S-MOS Logic Array Design System (LADS)

LADS is S-MOS' proprietary ASIC design software for use on an IBM PC or compatible. The software is free of charge to S-MOS customers. LADS requires the use of FutureNet or OrCAD schematic capture software.

LADS includes the S-MOS symbol libraries, netlist translator, design rule verification and test vector generation support software. LADS also includes the S-MOS proprietary DCS simulator, which performs full logic and timing verification. DCS can simulate tens-of-thousands of gates on an IBM PC compatible and is one of the fastest simulators available anywhere.

### Workstation Simulator Speed Comparison

Simulator	Simulation Time
Typical CAE workstation	1.5 hours
Typical PC-based simulator on PC-AT	2.5 hours
DCS from S-MOS on PC-AT	14 minutes
DCS from S-MOS on 386-based PC	5 minutes

Simulation time of 4000 gates and 4000 vectors

### S-MOS Workstation Design System for Daisy, Mentor and Intergraph

#### ■ Support Library

Macrocell symbol library  
Macrocell functional model library

#### ■ Software

Design rule checker (DRC)  
Netlist extractor  
Back annotation  
Test vector generation support  
Simulation post processor  
Gate array physical layout on Daisy

### ASIC Package Availability

Many other custom packages are available. Ask your S-MOS representative for further details.

Package Type	Pin Counts Available
Plastic dip	14 16 18 24 28 40 42 48 64
SOP	24 48
Plastic flat pack	44 46 60 80 100 128 144 160 196
PLCC	28 44 68 84
Low-cost PGA	64 72 132 176 208
Ceramic flat pack	148
PGA	64 72 132 176 208

### Quality Assurance

S-MOS, with our affiliate Seiko Epson, is totally committed to the realization of zero defects through a comprehensive quality assurance program.

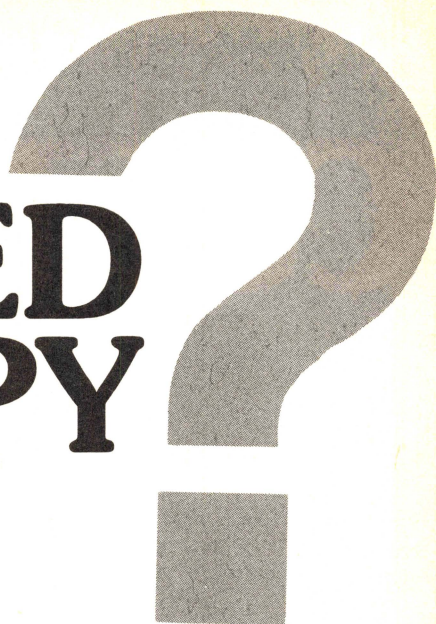
This program begins with new production definition and continues through design, product development and into production. Prior to first production, prototype samples are subjected to thorough reliability inspection. Before we officially release a new product or Macrocell, full characterization, environmental and life tests are performed on multiple lots to assure reliable and consistent products.

In addition to environmental tests, production parts receive 100% functional tests at customer's clock speed to 40 MHz (soon to be increased to 80 MHz). Memory products also receive 100% burn-in. Lot tests are performed on each production lot, including burn-in, temperature cycle, pressure cooker (plastic only) and electro-static discharge testing. Life tests are performed quarterly.

Full qualification tests are performed on each device/package combination and are redone any time there is a change in design, process or material.



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# THE CUSTOMATION DESIGN SYSTEM.

**SMC®'s leading-edge ASIC technology and microperipheral SuperCells™ combine to make your competitive-edge circuits.**

With CUSTOMATION™, you can invent the semicustom circuits you need without reinventing the wheel. Everything Standard Microsystems has learned in over a decade of developing innovative standard products and high-performance ASICs is at your disposal.

## **YOUR PLACE OR OURS.**

The real beauty of our system is that it puts you in total control of your design. You work at your own pace—at your own facility, if you wish—verifying logic through simulation every step of the way.

This hands-on involvement can help reduce production costs, speed up turnaround and virtually guarantee that first silicon is working silicon.

Standard Microsystems will provide everything you need to perform the entire design function, including a turnkey workstation complete with our cell library and "industry-standard" software, formal classroom training on how to use the CUSTOMATION™ design system and ongoing technical support.

Once you are totally satisfied with your design, we will then use your netlist database for automatic

placement and routing, carrying the process through masks, wafers and prototypes.

Or, if you prefer, we can do the full job, handling everything for you from start to finish. At your request, we can do the job at Standard Microsystems' Hauppauge design and manufacturing facility or at any of our worldwide network of design centers.

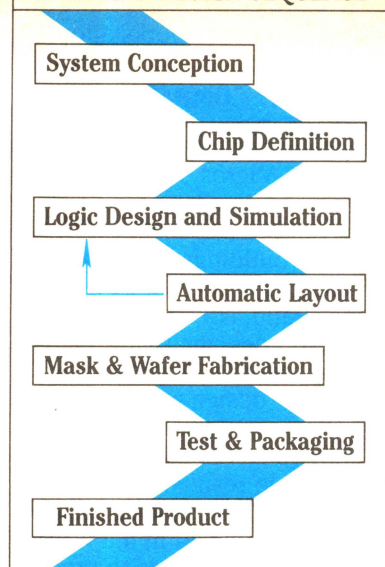
## **A TYPICAL DESIGN SEQUENCE.**

A CUSTOMATION™ design sequence typically involves the use of a progression of software design tools, with the output of one serving as the input for the next. (See flow chart.)

Although the designer is constantly monitoring this process, he is not actually "in line." Therefore, problems due to human error are almost completely eliminated, virtually assuring first-time success.



## A TYPICAL DESIGN SEQUENCE



## PROCESS TECHNOLOGY YOU CAN COUNT ON.

The cornerstones of the CUSTOMATION™ technologies are our production-proven 1.5, 2 and 3 micron, silicon-gate CMOS processes that are compatible with the design rules of several other major semiconductor manufacturers.

## A LIBRARY OF BEST-SELLERS.

There are hundreds of cells in the CUSTOMATION™ cell library, including a complete array of 74LS SSI and MSI logic functions, and a large and growing number of analog cells, macrocells and supercells. The design system stores the cell layouts, logical models and performance characteristics of each cell in its database.

Because most of our standard cells emulate 74LS logic functions, many of your design engineers should already be familiar with them.

We are always prepared to develop new cells to meet your specific requirements. For digital applications this might include special counter cells or special I/O buffers. Analog applications often require customized cells for your particular requirements.

You can feel totally confident about the performance of the CUSTOMATION™ cells, too. They are thoroughly characterized and have been used successfully in numerous

applications. Before a cell can be added to our library, it is completely modeled, characterized, tested and "certified."

Standard Microsystems is also dedicated to incorporating more microprocessor peripheral SuperCells™ into the library. These currently encompass such functions as ROMs, RAMs, UART "Tool-Set," 8250, 8259 BRG, Manchester Encoder/Decoder, 555 RC Oscillators, Real time clock DTMF encoder, RLL decoder, SCSI interface, floppy disk digital data separator, counter/timer and A to D converter.

### SuperCells™

**UART Tool-Kit**  
UART Building Cell-Set

**Manchester SuperCell™**  
Encoder/Decoder

**RTC SuperCell™**  
Real Time Clock

**PC-KBRD SuperCell™**  
PC Keyboard Interface Controller

**SCSI SuperCell™**  
SCSI Interface Controller

**TWINAX SuperCell™**  
5250 Interface Controller

**8250 SuperCell™**  
UART

**8259 SuperCell™**  
Prog. Interrupt Controller

**8254 SuperCell™**  
Programmable Interval Timer

**6845 SuperCell™**  
CRT Controller

**8237 SuperCell™**  
DMA Controller

**TIMER SuperCell™**  
Master Timer

**FDDS SuperCell™**  
Data Separator

**65CX02 SuperCell™**  
65C02 Core Microprocessor

**RAM SuperCell™**  
Modular RAM (512 bits/block)

**ROM SuperCell™**  
Modular ROM (512 bits/block)

**VCO SuperCell™**  
Voltage Controlled Oscillator

**555 SuperCell™**  
555 Timer

**DTMF SuperCell™**  
DTMF Tone Generator

**ATOD SuperCell™**  
8-Bit Analog to Digital Converter

## CUSTOMATION CELL LIBRARY PERFORMANCE

**Voltage:** 3V to 10V

**Temperature:** -55°C to +125°C

**Speed:** DC to 50 MHz

**Process:** 2μ DLM & 3μ SLM  
CMOS  
SIGATE

**I/O:** TTL & CMOS Compatible

**Fanout:** Capacitive Loading  
Restricted Only

**Delay:** <1.5 NSEC Typical

In addition to the customized layout of cells, we've also helped pioneer the use of "soft macrocells," which are the implementation of large logic blocks through the stored interconnection of more basic "core cells."

By using standardized core cells and "soft macrocells," digital designs presently fabricated in one technology are easily portable to next-generation processes. This means your design will never become dated or obsolete.

## INDUSTRY-STANDARD SOFTWARE.

CUSTOMATION™ utilizes software that provides a well-proven package of design aids which your engineers will be comfortable using. If you wish, the entire package can be licensed through Standard Microsystems.

We think you'll find our software to be comprehensive, easy to use and incredibly powerful. Netlists developed on any workstations supported by Standard Microsystems can be transported quickly and easily to any other. Logic can also be simulated on any workstation.

Our software is designed to virtually guarantee that your chip will work the first time, every time. We not only provide schematic capture, but logic simulation, timing analysis and automatic test program generation as well.



## OUTSTANDING CHECKS AND BALANCES.

The heart of the CUSTOMATION™ design system, STANSURE™, is a system of interrelated procedures, programs and data files that convert your input data into a working integrated circuit. The STANSURE™ system is designed to maximize the probability that all circuits designed using the CUSTOMATION™ cell library will be "first time" successes.

**STANSURE™** provides not only schematic capture, but logic simulation, timing analysis, fault coverage, automatic test program generation and automated breadboarding.

The **STANSURE™** system of procedures consists of the following elements:

**STANNET™**: the STANNET™ family of programs works with the workstation based schematic capture tools to convert the resulting netlists into a common database format and verifies the results. Also included in the STANNET™ family are the STANROM™ and STANRAM™ ROM and RAM memory generators.

**STANSIM™**: provides logic simulation, interfaces between the workstations and back annotation.

**STANTIME™**: timing verification programs calculate and display the propagation delays (rise and fall times) of each circuit element. The STANTIME™ programs may be run before and after layout. They will also calculate the cumulative propagation delays of each path on the design.

**STANCOMP™**: provides the chip layout and design rule checking functions. Further, it provides the capability of checking the netlist extracted from the layout with the logical netlist to assure the correctness of the layout data.

**STANWIRE™**: produces a wirewrap breadboard from the logical netlist of any circuit designed using the 74LS family of CUSTOMATION™ cells.

**STANTEST™**: produces Sentry® or GenRad™ compatible test files from the simulation vectors.

The **STANFAULT™** system of fault grading ensures that your

simulation will completely check the logic. The test program is then automatically generated from the proven simulation files. This ensures that your custom design will be adequate for tomorrow's demanding quality standards.

## A COMPLETE TURNKEY WORKSTATION.

Standard Microsystems offers a complete set of design tools, everything you need to develop your circuit from start to finish without ever leaving your facility. Our tools combine high performance and user-friendly operation. What's more, our standard cell library and circuit development tools are currently compatible with virtually all industry-standard workstations, including the IBM® PC (no hardware modification required with the VIEWlogic® Workview™ software), Daisy,™ Mentor Graphics, Valid Logic, and VAX. (Note: VAX® hardware is supported through the use of IBM® PC/compatible-based VIEWlogic™ graphic front-end systems.)

If one of these workstations is not your preferred model, check with Standard Microsystems. We are constantly enhancing our software to support other workstations and mainframes.

Each CUSTOMATION™ design system includes:

- ▶ **Symbols and Schematics**  
For Standard Microsystems' advanced standard cell library.
- ▶ **Circuit Simulation**  
Detailed and proven simulation models for each supported workstation.
- ▶ **Timing Analysis Package**  
A Supplement to workstation capabilities which performs detailed analysis of propagation delays for each circuit path and node throughout the design.
- ▶ **Automated Test Program Extraction**  
Standard Microsystems' software rapidly compiles IC test program files based on simulation data.
- ▶ **Complete "How To" Documentation**  
Design and Simulation Instruction Manual dedicated to your specific workstation.

If you like, we'll even install the CUSTOMATION™ cell library and software on your workstation, at your facility.

## THE RIGHT COMPANY FOR THE JOB.

Standard Microsystems is the right sized company for all of your ASIC needs. With five modern buildings housing 250,000 sq. ft. on our 30-acre Long Island, N.Y. site, we have the resources, including state-of-the-art wafer fabrication, assembly, design and test, to bring your program in on time, within budget and with remarkable results.

Yet we aren't too large. We can work with you in the way that *you* desire, to provide the results that you need.

Our 15 years of ASIC experience has taught us that service, support and communications are the keys to successful ASIC development. So, we open a direct pipeline to you and keep it open throughout the entire development and production program.

We've established an environment that stimulates creativity while encouraging adherence to pragmatic objectives. Our intensive Research and Development efforts have resulted in over 30 patents, and a list of licensees that is virtually a "who's who" of the semiconductor industry.

We monitor each project very carefully. Strict scheduling via program management and frequent customer contact has become the hallmark of our CUSTOMATION™ program.

Just as important, we have a track record of success. Numerous testimonials from satisfied customers are proof of our ability to perform. Quite simply, we make no promises we can't keep.

For more information or to get started with CUSTOMATION™, call your nearest Standard Microsystems regional office. Or contact Standard Microsystems Corporation, Custom Marketing Department, 35 Marcus Boulevard, Hauppauge, NY 11788. (516) 273-3100.



# SMC® CUSTOMATION™ STANDARD CELL LIBRARY

## CELL NAME DESCRIPTION

### LOGIC GATE CELLS

LS00	2-Input NAND Gate
LS02	2-Input NOR Gate
LS04	Inverter
LS08	2-Input AND Gate
LS10	3-Input NAND Gate
LS11	3-Input AND Gate
LS20	4-Input NAND Gate
LS21	4-Input AND Gate
LS25	4-Input NOR Gate with Strobe
LS27	3-Input NOR Gate
LS28	2-Input NOR Gate with Buffer
LS30	8-Input NAND Gate
LS32	2-Input OR Gate
LS37	2-Input NAND Gate with Buffer
LS40	4-Input NAND Gate with Buffer
LS51A	2-Wide, 2-Input AND-OR-Invert Gate
LS51B	2-Wide, 3-Input AND-OR-Invert Gate
LS54	4-Wide, 2-Input & 3-Input AND-OR-Invert Gate
LS55	2-Wide, 4-Input AND-OR-Invert Gate
LS64	4-2-3-2 Input AND-OR-Invert Gate
LS86	2-Input Exclusive OR (XOR) Gate
LS133	13-Input NAND Gate
LS134	12-Input NAND Gate with 3-State Output
LS260	5-Input NOR Gate
LS266	2-Input Exclusive NOR (XNOR) Gate

### BUFFER CELLS

LS125	Non-Inverting 3-State Buffer
LS126	Non-Inverting 3-State Buffer
LS240	Inverting 3-State Buffer
LS242	Inverting Transceiver
LS243	Non-Inverting Transceiver
LS244	Non-Inverting 3-State Buffer
LS245	Octal Non-Inverting Transceiver
LS265A	1-Input, Dual Complimentary Output Gate
LS265B	2-Input AND Gate w/Complimentary Dual Output
LS365	Hex Non-Inverting 3-State Buffer
LS366	Hex Inverting 3-State Buffer
LS367	Quad Non-Inverting 3-State Buffer
LS368	Quad Inverting 3-State Buffer

### SHIFT REGISTER CELLS

LS95	4-Bit Parallel I/O, Serial Input Left/Right SR
LS164	8-Bit Parallel Output, Serial Input SR w/Clear
LS166	8-Bit Parallel/Serial Input, Serial Output SR Clear
LS178	4-Bit Universal Shift Register
LS179	4-Bit Universal SR with Async. Clear
LS194	4-Bit Bidirectional Universal SR w/Clear
LS195	4-Bit Parallel Input/Output SR w/Clear
LS198	8-Bit Bidirectional Universal SR w/Clear
LS295	4-Bit Universal Shift Register
LS395	4-Bit Universal SR w/Async. Clear, 3-State Outputs

### FLIP-FLOP CELLS

LS73	J-K Flip Flop with Clear
LS74A	D Flip Flop with Set & Reset
LS76A	J-K Flip Flop
LS174	Hex D Flip-Flop with Direct Clear
LS175	Quad D Flip-Flop with Direct Clear
LS374	Octal D Flip-Flop with 3-State Output
LS377	Octal D Flip-Flop

## CELL NAME DESCRIPTION

### LATCH CELLS

LS75	Dual Transparent Latch
LS77	Dual Transparent Latch
LS100	Quad Transparent Latch
LS116	Quad Transparent Latch with Clear
LS375	Dual Transparent Latch

### MULTIPLEXER/SELECTOR CELLS

LS151	8:1 Multiplexer with Strobe
LS152	8:1 Multiplexer, Inverting
LS153	4:1 Multiplexer
LS157	Quad 2:1 Multiplexer
LS158	Quad 2:1 Multiplexer, Inverting
LS253	4:1 Multiplexer, 3-State Output
LS352	4:1 Multiplexer, Inverting
LS353	4:1 Multiplexer, 3-State, Inverting
MUX2TO1	2:1 Multiplexer Cell

### COUNTER CELLS

LS163	4-Bit Synchronous Binary Counter
LS169	4-Bit Synchronous Binary Up/Down Counter

### DECODER/ENCODER CELLS

LS138	3:8 Decoder with Enable
LS139	2:4 Decoder with Enable
LS148	8:3 Priority Encoder

### COMPARATOR CELL

LS85	4-Bit Magnitude Comparator
------	----------------------------

### ARITHMETIC OPERATOR CELL

LS83	4-Bit Full Adder
LS283	4-Bit Full Adder
LS183	Full Adder

### PARITY GENERATOR CELL

LS180	9-Bit Odd/Even Parity Checker
-------	-------------------------------

### GATE CELLS

AND8	8 Input AND Gate
AOI211	2-1-1 AND-OR-Invert
AOI22	2-2 AND-OR-Invert
AOI31	3-1 AND-OR-Invert
EXNOR	Exclusive NOR Gate
EXOR	Exclusive OR Gate
HBUF	High Drive Buffer
HBUFL	Large High Drive Buffer
MBUF	Medium Drive Buffer
INBUF	Input Buffer
INV	Inverter
INV3/OUTINV	High Drive INV/Output Buffer
OUTINV	Large Inverting High Drive Output Buffer
IOBUF	Input/Output Buffer
IOBUFL	Large I/O Buffer
DLYCEL	Delay Cell
NAN2	2 Input NAND Gate
NAN3	3 Input NAND Gate
NAN4	4 Input NAND Gate
NAN5	5 Input NAND Gate
NOR2	2 Input NOR Gate
NOR3	3 Input NOR Gate
NOR4	4 Input NOR Gate
OR8	8 Input OR Gate
OAI22	2-2 OR-AND-Invert
OAI31	3-1 OR-AND-Invert
INVT	Inverting 3-State Driver
TBUF	Non-Inverting 3-State Driver

### LATCH & FLIP-FLOP CELLS

CCND	Cross Coupled NAND Latch
CCNR	Cross Coupled NOR Latch
DFF	D Flip Flop
DFFR	D Flip Flop with Reset
DFFRS	D Flip Flop w/Set & Reset
JKFF	J-K Flip Flop
LAT	Transparent Latch
LATBUF	3-Stateable Transparent Latch
LATR	Transparent Latch with Reset
SRBN	Shift Register
UDC	Up/Down Counter
PCL2	Two Phase Clock

## CELL NAME DESCRIPTION

### ANALOG CELLS

ANSW	Analog Switch
CBGX	Current Bias Generators
DS1216	Schmitt Trigger (1.2-1.6V)
DS1218	Schmitt Trigger (1.2-1.8V)
DS1238	Schmitt Trigger (1.2-3.8V)
DS1323	Schmitt Trigger (1.3-2.3V)
DS1527	Schmitt Trigger (1.5-2.7V)
DS1728	Schmitt Trigger (1.7-2.8V)
DS2028	Schmitt Trigger (2.0-2.8V)
DS2232	Schmitt Trigger (2.2-3.2V)
OSCP	General Purpose Oscillator
POR	Power On Reset
PORLC	Low Current Power On Reset
VCM1	Voltage Reference (50uA)
VCM2	Voltage Reference (100uA)
VCM3	Voltage Reference (200uA)
OPAMP	General Purpose Operational Amplifier
COMP05	High Speed Low Power Comparator
COMP06	General Purpose Comparator

### PAD CELLS

INPD	Input PAD
IODPD48	48mA Input/Open-Drain Output Pad
IOPD25	2mA Split P-Channel I/O PAD
IOPD4	4mA Input/Output PAD
IOPD4S	4mA Split P-Channel I/O PAD
IOPD8	8mA Input/Output PAD
IOPD16	16mA I/O Pad
IOPD24	24mA I/O Pad
IPPD4	Input PAD with 400uA Pullup
IPPD8	Input PAD with 800uA Pullup
ODPD4	4mA 5V Open-Drain Output PAD
ODPD8	8mA 5V Open-Drain Output PAD
ODPD16	16mA 5V Open-Drain Output Pad
ODPD48	48mA 5V Open-Drain Output Pad
ONPD4	4mA 7V Open-Drain Output PAD
ONPD8	8mA 7V Open-Drain Output PAD
OPD4	4mA Output PAD
OPD8	8mA Output PAD
OPD16	16mA Output Pad
OPD24	24mA Output Pad
OPPD4	4mA 3-State Output PAD
OPPD8	8mA 3-State Output PAD
PUD30	P-Channel Pullup
PD30	N-Channel Pulldown

### SUPERCCELLS™:

UART Tool-Kit	UART Building Cell-Set
Manchester	Encoder/Decoder
SuperCell™	
RTC SuperCell™	Real Time Clock
PC-KBRD	PC Keyboard Interface
SuperCell™	Controller
SCSI SuperCell™	SCSI Interface Controller
TWINAX	5250 Interface Controller
SuperCell™	
8250 SuperCell™	UART
8259 SuperCell™	Prog. Interrupt Controller
8254 SuperCell™	Programmable Interval Timer
6845 SuperCell™	CRT Controller
8237 SuperCell™	DMA Controller
TIMER SuperCell™	Master Timer
FDDS SuperCell™	Data Separator
65C02	Core
SuperCell™	Microprocessor
RAM SuperCell™	Modular RAM (512 bits/block)
ROM SuperCell™	Modular ROM (512 bits/block)
VCO SuperCell™	Voltage Controlled Oscillator
555 SuperCell™	555 Timer
DTMF SuperCell™	DTMF Tone Generator
ATOD SuperCell™	8-Bit Analog to Digital Converter

**STANDARD MICROSYSTEMS CORPORATION**

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# TGC100 SERIES

## 1- $\mu$ m CMOS GATE ARRAYS

TEXAS  
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### features

- Fast Prototype Turnaround Time
- Extensive Design Support
  - Design Libraries Compatible with Daisy and Mentor CAE Systems
  - TI Regional ASIC Design Centers
  - TI ASIC Distributor Design Centers
- High Performance 1.0- $\mu$ m EPIC™ CMOS Technology
  - Typical Gate Delay 500ps (FO = 3)
  - Flip-Flop Toggle Rates to 208 MHz
- Three Arrays with Maximum Basic Cell Utilization to 8006 Equivalent Gates
- Integral ESD- and Latch-Up-Protection Circuitry
- Low-Cost, Industry-Standard Packages
- Integral AC Performance Test Structure

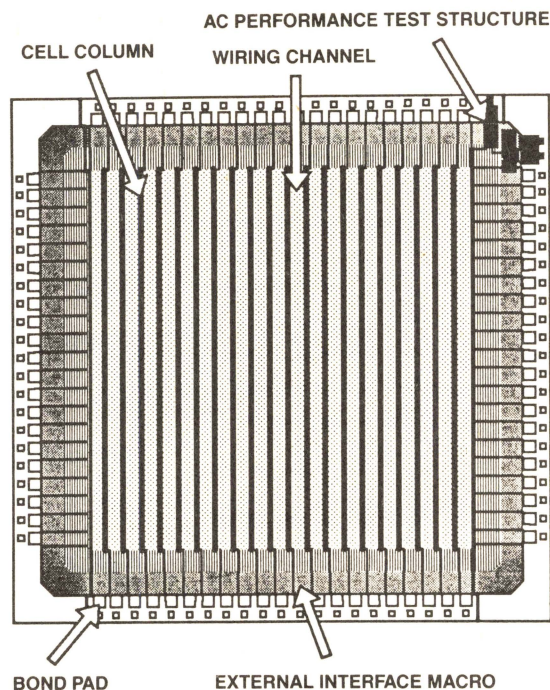


Figure 1. TGC103 CMOS GATE ARRAY

### description

The Texas Instruments TGC100 Series comprises three gate arrays, each fabricated using TI's 1-micrometer advanced silicon-gate CMOS EPIC™ process. The process features two levels of copper-doped-aluminum metalization for interconnect. Silicided polysilicon gate, source, and drain elements further reduce internal resistance and enhance performance. N-channel and P-channel gate lengths are patterned at 1.0 micrometer.

The basic structure of the TGC100 Series 1-micrometer CMOS gate arrays consists of basic-cell columns separated by wiring channels with a perimeter of external interface macros configurable as inputs, outputs, bidirectional I/Os, or power pins. Each 4-transistor internal basic cell is equivalent to a 2-input NAND gate. The three base gate arrays are shown below, along with their basic-cell and bond-pad configurations and standard production package options.

GATE ARRAY TYPE	BASIC CELLS		TOTAL BOND PADS	STANDARD PRODUCTION PACKAGE OPTIONS					
	TOTAL AVAILABLE	MAXIMUM USABLE		28-PIN PLCC	28-PIN DIP	40-PIN DIP	44-PIN PLCC	68-PIN PLCC	84-PIN PLCC
TGC103*	3200	2880	84	✓	✓	✓	✓	✓	✓
TGC105	5376	4838	118		✓	✓	✓	✓	✓
TGC108	8896	8006	142		✓	✓	✓	✓	✓

\* See Figure 1.



Each base array in the TGC100 Series incorporates an AC-performance test structure embedded in an otherwise unused corner of the array. Although not user-accessible from the I/O bond pads, this test structure is activated by TI during the wafer-probe stage of device fabrication when measurements are made to verify that the AC performance of the finished gate array falls within the normal production range. For most applications, this AC performance verification, in conjunction with the standard 1-MHz functional testing, is sufficient to ensure correct device operation and performance.

## library functions

The TGC100 Series gate array library includes basic gate and buffer macros and MSI-level macros. Of the 174 macros offered, 147 are hardwired and 27 are software macros. The hardwired macros provide a broad selection of predesigned, fully characterized functions. The software macros provide popular TTL/CMOS-type MSI functions that can be used as designed or modified at your workstation to suit your design requirements. Additional user-defined software macros can be created using the TGC100 library macros. Library release 1.0 contains the following classes of macros:

- 27 MSI Internal Software Macros
- 68 External Input, Output, and Bidirectional Buffer Macros
- 24 Internal Register, Flip-Flop, and Latch Macros
- 55 SSI Internal Gate and Bus Macros

A complete TGC100 Series Design Kit, supplied for the Daisy or Mentor CAE Systems, includes the following:

- TGC100 Series Data Manual
- 1- $\mu$ m CMOS Gate Array Design Manual
- Design Support Software User's Manual
- TGC100 Series Design Library

The Design Kit is arranged to accommodate new material as it is issued.

## recommended operating conditions

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage†	TTL-compatible inputs	2			V
		CMOS-compatible inputs	0.7V <sub>CC</sub>			V
V <sub>IL</sub>	Low-level input voltage†	TTL-compatible inputs			0.8	V
		CMOS-compatible inputs			0.2V <sub>CC</sub>	V
V <sub>I</sub>	Input voltage†		0		V <sub>CC</sub>	V
t <sub>t</sub>	Input transition (rise and fall times)†		0		100	ns
V <sub>O</sub>	Output voltage‡		0		V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current‡	As specified on data sheets				mA
I <sub>OL</sub>	Low-level output current‡					
T <sub>A</sub>	Operating temperature range		0		70	°C

† Applies for external input and bidirectional input buffers.

‡ Applies for external bidirectional and output buffers.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I <sub>CC</sub> Supply Current	TGC103	V <sub>I</sub> = V <sub>CC</sub> or 0 (See Note below)		350	μA
	TGC105			550	
	TGC108			850	

Note: For external inputs and bidirectional I/O buffers with pullup source V<sub>I</sub> = V<sub>CC</sub> and for external inputs and bidirectional I/O buffers with pulldown source V<sub>I</sub> = 0.

The remaining electrical and switching characteristics are specified on the individual macro data sheets.

## mechanical data

Production quantities of the TGC100 family of fast prototype gate-array designs are available in the industry-standard plastic packages shown below. Primary power-pin assignments utilize low-inductance locations and are implemented at offset positions, ensuring that improper insertion will not damage the device electrically. The minimum number of GND pins and the number of signal pins available are summarized in the following table.

## ARRAY ORGANIZATIONS AND PACKAGES

GATE ARRAY TYPE	BASIC CELLS		TOTAL BOND PADS	PLASTIC PACKAGE SELECTION ♦ (MIN V <sub>CC</sub> , MIN GND, MAX SIGNAL PINS)					
	TOTAL AVAILABLE	MAXIMUM USABLE		28-PIN PLCC	28-PIN DIP	40-PIN DIP	44-PIN PLCC	68-PIN PLCC	84-PIN PLCC
TGC103	3200	2880	84	1,2,25	1,2,25	1,2,37	1,2,41	2,4,62	2,4,78
TGC105	5376	4838	118	- - - -	1,2,25	1,2,37	1,2,41	2,4,62	2,4,78
TGC108	8896	8006	142	- - - -	1,2,25	1,2,37	1,2,41	2,4,62	2,4,78

♦ Prototypes are supplied in a socket/footprint-compatible ceramic package.

## military applications

TI also offers gate-array designs processed in compliance with MIL-STD-883, Method 5004/5005 or Method 5010. Production facilities are fully DESC and JAN certified. Please refer to the Military Products section of the IC Master for more information regarding TI Military ASICs.

FOR MORE INFORMATION ON THE TGC100 SERIES,  
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Department SRY5083IZ800  
Dallas, Texas 75380-9066

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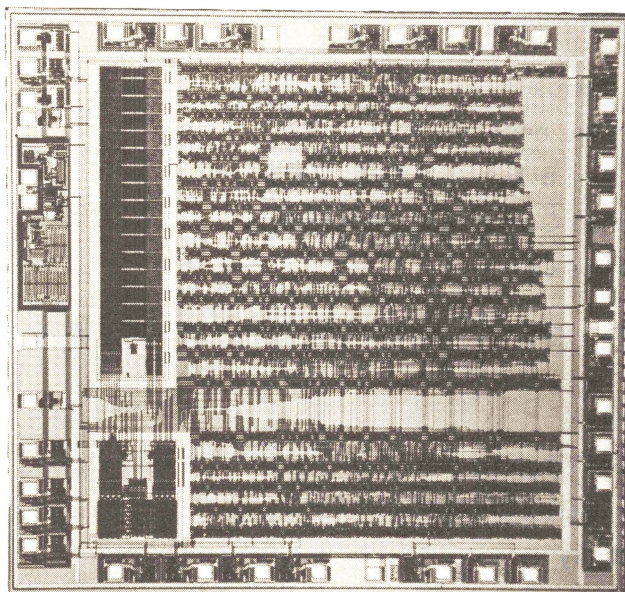


PHOTO COURTESY OF CHRYSLER

#### features

- **High-Performance 1.0- $\mu$ m EPIC™ CMOS Technology**
  - Typical Gate Delay 490ps (FO = 3)
  - Flip-Flop Toggle Rates to 170 MHz
- **Extensive Design Library (>350 Elements)**
  - SSI, MSI, and I/O Functions
  - LSI/VLSI MegaModule™ Building Blocks
- **Through-Hole/Surface-Mount Packaging Offering (DIP/SOIC/PLCC/PGA/QFP)**
- **User-Configurable High-Density SRAM**
- **Extensive Design Support**
  - Design Libraries Compatible with Daisy and Mentor CAE Systems
  - TI Regional ASIC Design Centers
  - Comprehensive Design Kit Support
- **Specified Over Full Commercial and Military Temperature Range**

#### description

The Texas Instruments TSC500 Series comprises an extensive offering of SSI, MSI, and I/O functions and a growing library of LSI/VLSI building blocks, each fabricated using TI's 1-micrometer advanced silicon-gate CMOS EPIC™ process. The process features two levels of copper-doped-aluminum metalization for interconnect. Silicided polysilicon gate, source, and drain elements further reduce internal resistance and enhance performance. N-channel and P-channel gate lengths are patterned at 1.0 micrometer.

## library functions

The TSC500 Series cell library includes basic gate, buffer, and MSI-level macros. Of the 352 cells offered, 302 are hardwired and 50 are software macros. The hardwired macros provide a broad selection of predesigned, fully characterized functions. The software macros provide popular TTL/CMOS-type MSI functions that can be used as designed or modified at your workstation to suit your design requirements. Additional user-defined software macros can be created using the TSC500 Series library. Library release 1.0 contains the following classes of macros:

- 50 MSI Internal Software Macros
- 15 MSI Internal Hardwired Macros
- 79 External Input, Output, and Bidirectional Buffer Cells
- 27 Internal Register, Flip-Flop, Counter, and Latch Macros
- 181 SSI Internal Gate and Bus Cells

A complete TSC500 Series Design Kit, supplied for the Daisy and Mentor CAE Systems, includes the following:

- TSC500 Series Data Manual
- 1- $\mu$ m CMOS Standard Cell Design Manual
- Design Support Software User's Manual
- TSC500 Series Design Library

The Design Kit is arranged to accommodate new material as it is issued.

### STANDARD-CELL PACKAGE OPTIONS

Type	Number of Pins																	
	8	16	20	24	28	40	44	48	64	68	84	100	120	132	144	164	180	208
DIP	✓	✓	✓	✓	✓	✓		✓										
SOIC		✓	✓		✓													
LCC					✓		✓			✓	✓							
QFP											✓	✓		✓				
PGA												✓	✓	✓	✓		✓	✓



## military applications

TI also offers standard-cell designs processed in compliance with MIL-STD-883, Method 5004/5005 or Method 5010. Production facilities are fully DESC and JAN certified. Please refer to the Military Products section of the IC Master for more information regarding TI Military ASICs.

## recommended operating conditions

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$V_{IH}$	High-level input voltage†	TTL-compatible inputs	2			V
		CMOS-compatible inputs	$0.7V_{CC}$			V
$V_{IL}$	Low-level input voltage†	TTL-compatible inputs			0.8	V
		CMOS-compatible inputs			$0.2V_{CC}$	V
$V_I$	Input voltage†		0		$V_{CC}$	V
$t_t$	Input transition (rise and fall times)†		0		100	ns
$V_O$	Output voltage‡		0		$V_{CC}$	V
$I_{OH}$	High-level output current‡		As specified on data sheets			mA
$I_{OL}$	Low-level output current‡					
$T_A$	Operating temperature range	Military	– 55		125	°C
		Extended	– 40		85	°C

† Applies for external input and bidirectional input buffers.

‡ Applies for external bidirectional and output buffers.

**FOR MORE INFORMATION ON THE TSC500 SERIES,  
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**TEXAS  
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# TEXAS INSTRUMENTS PROGRAMMABLE LOGIC CROSS REFERENCE

## IMPACT™ PAL® DEVICES

NOVEMBER 1987

TEXAS INSTRUMENTS RELEASED PRODUCTS				AMD		MMI		NATIONAL	
PINS	DEVICE TYPE	WORST CASE		TYPE	T <sub>pd</sub> /cc	TYPE	T <sub>pd</sub> /cc	TYPE	T <sub>pd</sub> /cc
		T <sub>pd</sub> (ns)	I <sub>cc</sub> (ma)						
20	TIBPAL16L8-10	10	180	AmPAL16L8D	10/180	PAL16L8D	10/180	----	----
20	TIBPAL16R8-10	10	180	AmPAL16R8D	10/180	PAL16R8D	10/180	----	----
20	TIBPAL16R6-10	10	180	AmPAL16R6D	10/180	PAL16R6D	10/180	----	----
20	TIBPAL16R4-10	10	180	AmPAL16R4D	10/180	PAL16R4D	10/180	----	----
20	TIBPAL16L8-12	12	210	----	----	----	----	----	----
20	TIBPAL16R8-12	12	210	----	----	----	----	----	----
20	TIBPAL16R6-12	12	210	----	----	----	----	----	----
20	TIBPAL16R4-12	12	210	----	----	----	----	----	----
20	TIBPAL16L8-15	15	180	AmPAL16L8B	15/180	PAL16L8B	15/180	DMPAL16L8B	15/180
20	TIBPAL16R8-15	15	180	AmPAL16R8B	15/180	PAL16R8B	15/180	DMPAL16R8B	15/180
20	TIBPAL16R6-15	15	180	AmPAL16R6B	15/180	PAL16R6B	15/180	DMPAL16R6B	15/180
20	TIBPAL16R4-15	15	180	AmPAL16R4B	15/180	PAL16R4B	15/180	DMPAL16R4B	15/180
20	TIBPAL16L8-25	25	100	AmPAL16L8A	25/180	PAL16L8B-2	25/90	DMPAL16L8B-2	25/90
20	TIBPAL16R8-25	25	100	AmPAL16R8A	25/180	PAL16R8B-2	25/90	DMPAL16R8B-2	25/90
20	TIBPAL16R6-25	25	100	AmPAL16R6A	25/180	PAL16R6B-2	25/90	DMPAL16R6B-2	25/90
20	TIBPAL16R4-25	25	100	AmPAL16R4A	25/180	PAL16R4B-2	25/90	DMPAL16R4B-2	25/90
24	TIBPAL20L8-15	15	180	AmPAL20L8B	15/210	PAL20L8B	15/210	DMPAL20L8B	15/210
24	TIBPAL20R8-15	15	180	AmPAL20R8B	15/210	PAL20R8B	15/210	DMPAL20R8B	15/210
24	TIBPAL20R6-15	15	180	AmPAL20R6B	15/210	PAL20R6B	15/210	DMPAL20R6B	15/210
24	TIBPAL20R4-15	15	180	AmPAL20R4B	15/210	PAL20R4B	15/210	DMPAL20R4B	15/210
24	TIBPAL20L8-25	25	105	AmPAL20L8A	25/210	PAL20L8A	25/210	DMPAL20L8A	25/210
24	TIBPAL20R8-25	25	105	AmPAL20R8A	25/210	PAL20R8A	25/210	DMPAL20R8A	25/210
20	TIBPAL20R6-25	25	105	AmPAL20R6A	25/210	PAL20R6A	25/210	DMPAL20R6A	25/210
20	TIBPAL20R4-25	25	105	AmPAL20R4A	25/210	PAL20R4A	25/210	DMPAL20R4A	25/210
24	TIBPAL20L10-20	20	165	AmPAL20L10-20	20/165	----	----	----	----
24	TIBPAL20X10-20	20	180	----	----	----	----	----	----
24	TIBPAL20X8-20	20	180	----	----	----	----	----	----
24	TIBPAL20X4-20	20	180	----	----	----	----	----	----
24	TIBPAL20L10-30	20	165	----	----	PAL20L10A	30/165	DMPAL20L10	30/165
24	TIBPAL20X10-30	20	180	----	----	PAL20X10A	30/180	DMPAL20X10	30/180
24	TIBPAL20X8-30	20	180	----	----	PAL20X8A	30/180	DMPAL20X8	30/180
24	TIBPAL20X4-30	20	180	----	----	PAL20X4A	30/180	DMPAL20X4	30/180
24	TIBPALR19L8,R8,R6,R4	25	210	----	----	----	----	----	----
24	TIBPALT19L8,R8,R6,R4	25	210	----	----	----	----	----	----
24	TIBPAL22V10	35	180	AmPAL22V10	35/180	----	----	----	----
24	TIBPAL22V10A	25	180	AmPAL22V10A	25/180	----	----	----	----
24	TIBPAL22VP10-20	20	210	----	----	----	----	----	----
24	TIEPAL10H16P8-6	6	240	----	----	----	----	PL1016P8	6/220

## PROGRAMMABLE LOGIC SEQUENCERS

PINS	DEVICE TYPE	F <sub>max</sub> (MHz)	I <sub>cc</sub> (ma)	SIGNETICS		TYPE	F <sub>max</sub> /I <sub>cc</sub>	TYPE	F <sub>max</sub> /I <sub>cc</sub>
				TYPE	F <sub>max</sub> /I <sub>cc</sub>				
28	TIB82S105BCN	50MHz	180	N82S105ACN	20/180	----	----	----	----
24	TIB82S167BCNT	50MHz	180	N82S167ACN	20/180	----	----	----	----

## TEXAS INSTRUMENTS NEW PAL® PRODUCTS

PINS	DEVICE TYPE (FAMILY)	T <sub>pd</sub> (ns)	I <sub>cc</sub> (ma)	FEATURES	AVAIL
20	TICPAL16L8,R8,R6,R4-55	55	0-70	UV-ERASABLE, ZERO STANDBY POWER, CMOS PAL	NOW
20	TICPAL18V8-25	25	0-70	UV-ERASABLE, GENERIC ARCHITECTURE, CMOS PAL	1Q88
24	TICPAL22V10-25	25	0-70	UV-ERASABLE, CMOS VERSION OF 22V10	1Q88
24	TIBPSG507	50MHz	180	PROGRAMMABLE SEQUENCE GENERATOR	JAN 88
24	TIBPLS506	50MHz	180	PROGRAMMABLE LOGIC SEQUENCER	JAN 88
24	TIEPAL10016P8-6	----	240	ECL IMPACT PAL, 100K VERSION	DEC 87
24	TIEPAL10016P8-3	----	240	ExCL PALS	1Q88
24	TIEPAL10K16P8-3	----	240	ExCL PALS	1Q88

Note: All speed and power specs are maximum  
SURFACE MOUNT DEVICES ARE AVAILABLE UPON REQUEST.  
PAL® is a registered trademark of Monolithic Memories, Inc.  
IMPACT™ is a trademark of TEXAS INSTRUMENTS.

 **TEXAS  
INSTRUMENTS**





# ISB12000 SERIES

1.2 $\mu$ /2 METAL HCMOS GATE ARRAYS

3,000 TO 50,000 GATES

SEMICUSTOM PRODUCTS

## FEATURES

- ☐ 1.2 micron HCMOS process, poly silicide gates, 2-layer metal with Titanium barriers and hermetic silicon nitride passivation.
- ☐ 2-input NAND delay less than 300 ps (typ).
- ☐ Channel-less architecture utilizing transistor gate isolation.
- ☐ Gate count ranging from 8,000 to 128,000.
- ☐ Extensive macrocell, macrofunction and megacell library elements available.
- ☐ Full function TTL and CMOS I/O cells.
- ☐ Configurable drive up to 8 mA with slew rate control and current spike suppression. Buffers may be paralleled to generate up to 16 mA of source/sink drive.
- ☐ Augmented metal grid to maximize power distribution.
- ☐ VAX based design system, interfaces from multiple workstations.
- ☐ Latchup trigger current  $> \pm 500$  mA.  
ESD protection  $> \pm 2000$  V.  
Short circuit protection.

- ☐ ISB12054 evaluation device available.
- ☐ Full military capability.
- ☐ Broad ceramic and plastic package offering.

## GENERAL DESCRIPTION

The ISB12000 Sea-of-Gates series uses a high performance, double level metal HCMOS process to achieve sub-nanosecond internal speeds, while, at the same time offering low power dissipation and high noise margin. The raw gate count ranges from 8,000 to 128,000. Using a conservative routing efficiency of 40%, the ten generic arrays that are offered range from 3,000 to 50,000 equivalent 2-input NAND gates. The I/O offering ranges from 76 to 320 full function cells. Output buffers have drive strengths of up to 8 mA and are provided with built in slew rate control to limit the di/dt of each buffer. Buffers may be paralleled to provide a maximum of 16 mA current drive. Internal macros are offered with multiple buffer drive capability to reduce the delay times of critical paths.

A wide range of CAD tools are combined into the design system which will allow designs to be developed on a VAX mainframe and multiple workstations. The high density channel-less structure, using transistor isolation, is ideally suited for embedded structured arrays and megafunctions like FIFO's, multiport RAMS, and data path megacells. An extensive package offering makes this series well suited for a broad range of commercial, industrial and military applications.

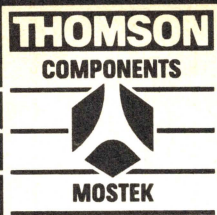
Table 1. Product Outline

DEVICE NUMBER	INTERNAL CELLS	GATE (1) COMPLEXITY	ESTIMATED (2) USEABLE GATES	TOTAL (3) DEVICE PADS	MAXIMUM I/O
ISB12008	20,000	8,000	3,000	88	76
ISB12011	28,800	11,520	4,500	104	92
ISB12015	39,200	15,680	6,000	120	108
ISB12020	51,200	20,480	8,000	136	120
ISB12025	64,800	25,920	10,000	152	136
ISB12038	96,800	38,720	15,000	184	164
ISB12054	135,200	54,080	20,000	216	200
ISB12076	192,200	76,880	30,000	256	232
ISB12103	259,200	103,680	40,000	296	256 (4)
ISB12128	320,000	128,000	50,000	328	256 (4)

### NOTES:

1. A factor of 2.5 is used to derive gate complexity from internal cells.
2. A conservative routing efficiency of 40% is quoted. This number will vary depending on the design.
3. Eight dedicated  $V_{DD}/V_{SS}$  pads. I/O pads may be reconfigured for additional  $V_{DD}/V_{SS}$  pads.
4. I/O signals currently limited to 256 by tester constraints.





# TSGC SERIES

1.2 $\mu$ /2 METAL HCMOS GATE ARRAYS

1000 TO 10000 GATES

SEMICUSTOM PRODUCTS

## FEATURES

- ☐ Gate delay: 1.0 ns typical with fan out of 2.
- ☐ Speed: up to 65 MHz operating frequency.
- ☐ Advanced HCMOS technology:
  - 1.2  $\mu$  Design rules.
  - 2 metal layers.
  - twin tub CMOS process.
- ☐ Operating temperature range:
  - commercial : 0 to 70°C
  - industrial : -40 to + 85°C
  - military : -55 to + 125°C.
- ☐ High latch-up immunity  
±500 mA (typ)
- ☐ Full Electrostatic Protection  
±2000 V (min)
- ☐ Gate Count: Up to 10000 gates.
- ☐ Power Supply:
  - maximum ratings : -0.5 to + 7 V.
  - operation : 3 to 6 V.

## ADVANCED HCMOS GATE ARRAY FAMILY

- ☐ Input/Output Cells:
  - compatability : TTL or CMOS levels.
  - configurability : individually programmable as driver receiver, 3 state, bidirectional, or power pad.
- ☐ Macro cell library:
  - hard macros : 70 different combinational/sequential SSI/MSI functions.
  - soft macros : more than 150 described soft macros.
- ☐ CAD software support:
  - fully integrated frame design automation system.
  - 98% silicon use with 100% auto place and route.
  - support of popular CAE workstations and PC schematic capture systems.

## TSGC 1.2 $\mu$ /2 METAL LAYER HCMOS SERIES

Part Number	Gate Count (1)	I/O Pads	V <sub>DD</sub> /V <sub>SS</sub> Pads	Total Pads (2)	Package Pin options
TSGC 01000	1120	56	12	68	24 to 68
TSGC 02000	2128	76	12	88	24 to 84
TSGC 03000	3264	96	12	108	28 to 120
TSGC 04000	4256	108	12	120	28 to 124
TSGC 06000	5880	132	12	144	68 to 144
TSGC 08000	7872	168	16	184	84 to 208
TSGC 10000	9776	192	16	208	84 to 208

Note 1: 1 gate is the equivalent of a 2 input NAND or NOR gate (2 N and 2 P channel transistors).

Note 2: The pad count is for the chip only. The final device pin count is package and application dependent  
- high pin count devices may require additional power and ground pins.





# TSK09 SERIES

ANALOG BIPOLAR ARRAYS

SEMICUSTOM PRODUCTS

ASICs/CUSTOM

Thomson/Mostek

## GENERAL DESCRIPTION

The K09 array is a prediffused bipolar array of components allowing the user to design his specific applications in a short period of time and with a minimum risk of errors.

The K09 array is specially intended for use in video, telecommunication, instrumentation, and other high frequency applications, but it could also be used with benefit for low frequency circuits.

It contains an array of unconnected integrated transistors, resistors and capacitors on a monolithic chip, arranged in such a regular way on the chip that MACROCELLS like Operational amplifier, voltage regulator, timer, etc., are easily predefined in a LIBRARY developed either by THOMSON-SEMICONDUCTEURS or by the customer himself.

Development of a particular circuit requires the user to place on the array the selected MACROCELLS, with possibly some other components needed for his specific application, and to route the needed interconnections thanks to one metal pattern. So, a custom linear integrated circuit is implemented through an unique interconnection mask.

The K09 array is manufactured using a very high frequency technology ( $f_t$  of NPN  $\gg 3$  GHz) which allows a 15 volts maximum supply operation voltage. This  $f_t$  and a beta of 100 are obtained at a collector current as low as 1 mA.

The K09 array fully meets military environment specifications.

The customization is made by etching only the second layer of metallization. The first layer of metallization is a standard, predefined pattern that provides the following features:

- Low resistance distribution of the positive and negative supply voltages across the chip.
- Availability of cross-overs: each NPN transistor has four collector vias connected to each other on the first metal layer. Furthermore, some first layer connections are available to easily join the centre of the die with bonding pads.
- Use of a grid for routing the second (customized) layer of metallization. The designer routes the specific interconnections by following the grid. The layout rules are automatically maintained.

Components	Description	Number
NPN transistors	QN1: NPN, 5 mA max collector current	126
	QN2: NPN, 10 mA max collector current	42
	QN3: Double emitter NPN, 10 mA max collector current	10
	QN4: Low noise NPN, ( $r_{bb'} = 100$ ohms) 40 mA max collector current	10
	<b>Total NPN transistors</b>	<b>188</b>
PNP transistors	QP: lateral PNP, up to 50 $\mu$ A collector current	28
Capacitors	C: MOS capacitor: 6 pF	4
Resistors	P +	
	100 ohms	70
	200 ohms	70
	400 ohms	70
	800 ohms	84
	(200 + 800) ohms	70
	Extrinsic P. base	
	2 kohms	70
	2 kohms	70
	4 kohms	70
	8 kohms	70
	16 kohms	42
	<b>Total resistors</b>	<b>686</b>
	<b>Total components</b>	<b>906</b>





# TSGF SERIES

MASK PROGRAMMABLE FILTERS

ANALOG SWITCHED CAPACITOR FILTER ARRAYS

SEMICUSTOM PRODUCTS

## ASIC PRODUCTS

### FEATURES

- HCMOS Mask Programmable switched capacitor Filters : fast Design turn-around time (5 to 6 weeks average), thanks to gate array approach.
- Integration of any kind of classic, non-classic filters : Bandpass, Lowpass, Highpass, Band Reject... Cauer, Chebychev, Butterworth, Legendre...
- Filter order : from 2 to 12.
- Cascadable structure : higher order achievable.
- No external components required to realize the filtering function.
- Additional options available on chip :
  - uncommitted Op-Amps (for anti-aliasing and/or smoothing filters, half or full wave rectifier...);
  - internal divider (sampling frequency generated from external clock);
  - output sample-and-hold.

### ORIGINALITY

- TSGF series provides :
  - leapfrog structure for very low sensitivity filters ;
  - cascadable biquadratic cells for non-classic filter design.

### SUPPORT

- TSGF series fully supported by "FILCAD"® CAD

## HCMOS

## MPFs

software from filter synthesis and simulation up to layout.

- Application notes.
- Evaluation Boards.

### CHARACTERISTICS

- Input Signal Frequency : 0 to 30 KHz
- Signal to Noise Ratio : 60 to 85 dB
- Power Supply : dual  $\pm 5$  V  
single 0 - 10 V  
single 0 - 5 V
- Adjustable Power Consumption : 0.5 mW to 20 mW per filter order.
- Quality factor : up to 50
- Pass-band gain : up to 40 dB
- Input sensitivity : 1mVRMS (min)

### TSGF SERIES PRODUCT RANGE

Part Number	Number of on-chip filters	Filter order	Uncommitted Op-Amps	Clock	Output Sample-and Hold	Packages
TSGF04	1	2 to 4	1	Internal oscillator* TTL/CMOS levels	external* driving	PDIP 8-14 pins CDIP 14 pins SO wide 16 pins
TSGF08	1	4 to 8	2	1 clock input TTL/CMOS levels	internal driving	PDIP 8-16 pins CDIP 16 pins SO wide 16 pins
TSGF12	1 or 2	8 to 12	2	2 clock inputs TTL/CMOS levels	external* driving	PDIP 16-18-20 pins CDIP 16-18-20 pins SO wide 18-24 pins

\* Optional

### FILTERING SOLUTION WITH GATE ARRAY TECHNIQUE

TSGF series is a family of Mask Programmable Filters (MPFs) developed by Thomson Semiconducteurs.

The TSGF product range is composed of 3 switched capacitor filter base arrays, TSGF04, TSGF08 and TSGF12 providing filter integration capabilities from 2nd to 12th order.

TSGF04/08/12 are using "gate array" technique : the filter customization is achieved only by the final metallization mask.

Therefore TSGF series provide users with filter integration solutions with very fast design turn-around time : 5 to 6 weeks up to delivery of full tested prototypes.

TSGF04/08/12 base arrays provide on chip all necessary functions to realize all kind of filters :

- transconductance amplifiers
- switches
- capacitor fields
- sample-and-hold





# TSGSM SERIES

CMOS STANDARD CELL FAMILY

MIXED ANALOG/DIGITAL

SEMICUSTOM PRODUCTS

ASICs / CUSTOM

Thomson / Mostek

## FEATURES

- ☐ 2.7 Micron HC1PA process with 800 Angstrom thin oxide gates
- ☐ Silicon-gate P-well technology
- ☐ Single-level-metal with double level polysilicon for switched capacitor applications
- ☐ Logic performance is TTL/LS compatible: 7.4 nS for a 2-input Nand gate ( $f_0 = 3$ )
- ☐ Maximum logic frequency: 25 MHz
- ☐ CMOS and TTL compatible I/O cells
- ☐ Input buffer support pull-up and pull-down resistors
- ☐ Extensive digital and analog library of 94 functions
- ☐ Commercial, industrial, and military temp ranges
- ☐ Fully supported by THOMSCAD VAX/VMS based design system
- ☐ Two operating voltage ranges specified:  
5V  $\pm$  10%  
10V  $\pm$  10%

## GENERAL DESCRIPTION

The TSGSM Standard cell Family uniquely offers the system designer full flexibility in analog and digital system design. A rich library of predefined and characterized functions, including standard logic gates, flip-flops and latches, clock generators, A/D converters, comparators, LCD drivers, and voltages references, etc., meets the needs of a broad variety of industrial, automotive, consumer, and instrumentation applications.

The THOMSCAD design system has been proven as an efficient and accurate suite of CAD tools for the successful realization of a large number of TSGSM designs - from netlist entry through simulation and layout to prototype test and production release. Complete design manuals are available to aid the designer in cell selection, and design approach.

Both standard height cells for small functions and block cells for major cells are supported, all on a grid basis for automated place and route within THOMSCAD.

The TSGSM Standard Cell may be packaged in any of a broad range of Dual-in-Line, LCC and PGA package, in both plastic and ceramic styles.

LOGIC CELLS	INPUT/OUTPUT CELLS	ANALOG CELLS
1-20X Inverters AND/NAND/OR/NOR Complex (Boolean) Gates D Flip/Flops/Latches Tristate Buffers (on-chip) Multiplexers 8-32 Bit Clock Generators 2-4 Phase Clock Generators Delay Inverter	CMOS/TTL Input Buffers — Inverting/Non-Inverting — Pull-up/Pull-down Option CMOS/TTL Output Buffers — Inverting/Non-inverting Bidirectional Buffers — CMOS/TTL Levels — Inverting/Non-Inverting Open Drain Buffers Tristate Buffers	8-12 Bit Analog/Digital Converters Comparators Operational Amplifiers LCD Driver - Segment or Backplane Crystal Oscillators Power-on Reset Analog Switches Schmitt Triggers Bipolar Transistors Capacitor Fields Potentiometer Fields





# TSSC SERIES

1.2 $\mu$ /2 METAL HCMOS STANDARD CELLS

SEMICUSTOM PRODUCTS

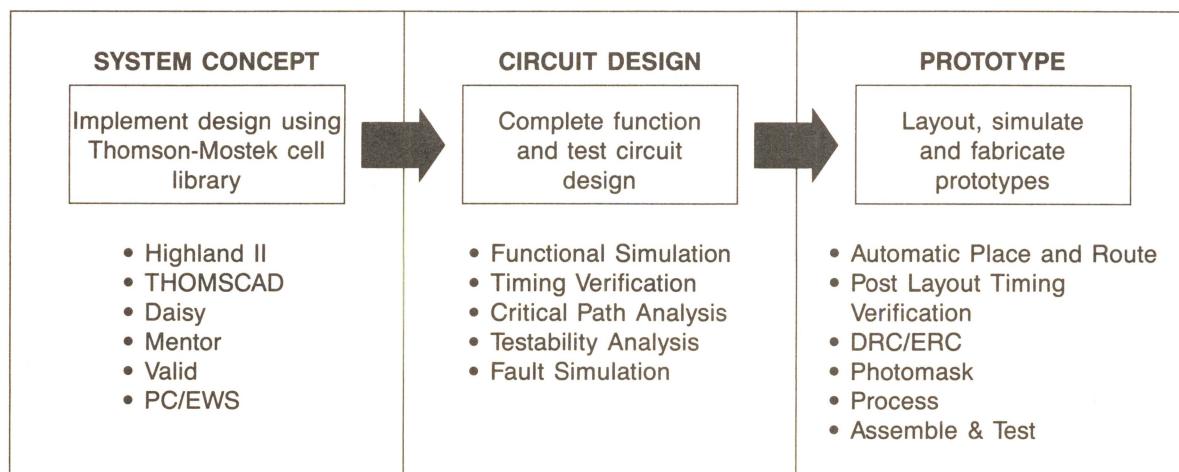
## FEATURES

- ☐ Gate delay: 1.0 ns typical with fan out of 2.
- ☐ Speed: up to 60 MHz operating frequency.
- ☐ Advanced HCMOS technology:
  - 1.2  $\mu$  Design rules.
  - 2 metal layers.
  - twin tub CMOS process.
- ☐ Operating temperature range:
  - commercial : 0 to 70°C
  - industrial : -40 to + 85°C
  - military : -55 to + 125°C.
- ☐ High latch-up immunity  
±500 mA (typ)
- ☐ Full Electrostatic Protection  
±2000 V (min)
- ☐ Power Supply:
  - maximum ratings : -0.5 to + 7 V.
  - operation : 3 to 6 V.

## ADVANCED HCMOS STANDARD CELL FAMILY

- ☐ Input/Output Cells:
  - compatibility : TTL or CMOS levels.
  - configurability : individually programmable as driver receiver, 3 state, bidirectional, or power pad.
- ☐ Standard cell library:
  - 170 fixed height standard cells with speed selections. Broad soft macro library.
  - RAM, ROM, PLA, FIFO mega cell functions
- ☐ CAD software support:
  - fully integrated frame design automation system.
  - 100% auto place and route.
  - support of popular CAE workstations and PC schematic capture systems.

## TSSC 1.2 $\mu$ /2 METAL LAYER HCMOS SERIES





# Toshiba. World Technology Leader in ASICs.

Toshiba's process technology experience made it possible to build the new 50,000 gate, 0.56 Nanosecond "Sea of Gates" Compacted Array.<sup>TM</sup>

TOSHIBA CMOS GATE ARRAYS				
Basic Characteristics	3 MICRON CHANNELLED ARRAY	2 MICRON CHANNELLED ARRAY	1.5 MICRON CHANNELLED ARRAY	SEA OF GATES COMPACTED ARRAY <sup>TM</sup>
Product line-up	*TC15G series	*TC17G series	TC19G series	TC110G series
Process technology	HC <sup>2</sup> MOS Si-gate double layer metal			
Supply voltage	5V			
Maximum toggle frequency	50 MHz	100 MHz	120 MHz	150 MHz
Design rule	3 $\mu$ m	2 $\mu$ m	1.5 $\mu$ m	1.5 $\mu$ m
Gate speed (inner gate, typ.)	2.5 ns	1.5 ns	1.0 ns	0.56 ns
Application	LSTTL/ALSTTL	STTL	ASTTL	ASTTL/ECL
Availability	NOW			

\*:TC15G/17G series are alternately-sourced by LSI Logic Corp.

## LDS SYSTEM FEATURES

Integrated Design System using Macrocell library for:

- Functional design
- Logic design
- Automatic placement & routing
- Test pattern generation

Hierarchical design using: • Macrofunctions (which consist of Macrocells)

Maximum circuit size: • 50K gates

Timing verification of critical paths and safe margin check by Toshiba Delay Path analysis System (TDPS)

TOSHIBA CMOS STANDARD CELLS			
Basic Characteristics	TC21SC	TC22SC	TC23SC***
Product line-up			
Library	TC21SC series macrocells 120 types 74 series compatible macros Functional macros (PLA, ALU, MPY)** RAM ROM **under development		ADVANCELL <sup>TM</sup> library 160 macrocells 2900 series macros 74 series compatible macros Functional macros Larger RAM Larger ROM Super macros (CPU, Peripheral) Analog macros (ADC, DAC)
Design rule	2 $\mu$ m		1.5 $\mu$ m
Process technology	HC <sup>2</sup> MOS Si-gate double layer metal		
Maximum toggle frequency	100MHz		150MHz
Gate speed (inner gate)	1.5 nsec		1.0 nsec
Supply voltage	5V		
Gate complexity (max.)	10K gates		33K gates
Availability	NOW		NOW

\*\*\*:CAD System for TC23SC Series

## VL CAD-II SYSTEM FEATURES

Integrated Design System using Macrocell library for:

- Function design
- Logic design
- Automatic placement & routing
- Test pattern generation

Hierarchical design using: • Functional blocks (which consist of Macrocell) • ROM and RAM blocks

Maximum circuit size: • 100K gates (maximum functional block size = 10K blocks)

Hierarchical Hardware Description Language (H<sup>2</sup>DL) for: • MIXED MODE level simulation • FUNCTIONAL level simulation

Timing verification of critical paths and safe margin check

For complete Technical Data call:

## TOSHIBA AMERICA, INC.

NORTHWESTERN:  
Sunnyvale, CA • (408) 733-3223

SOUTHWESTERN:  
Newport Beach, CA • (714) 752-0373

NORTH CENTRAL:  
Chicago, IL • (312) 945-1500

SOUTH CENTRAL:  
Dallas, TX • (214) 480-0470

NORTHEASTERN:  
Burlington, MA • (617) 272-4352

SOUTHEASTERN:  
Norcross, GA • (404) 368-0203



# TQ3000

## LSI GaAs Gate Array

Supports LSI Solutions to 1GHz  
3000 Equivalent Gates

Designed to extend the performance of silicon based systems

### ■ Low Power

Power per gate = 0.75mW  
More than 50% lower than fastest ECL

### ■ Large Array Size

1020 available corecell locations  
3000 equivalent gates  
Can implement 255 Master/Slave Flip-Flops

### ■ 64 Dedicated High Speed I/O's

Programmable for ECL, TTL and CMOS

### ■ High Speed

Typical Delays  
Inverter = 130ps  
2-input NOR = 150ps  
Flip-Flop = 290ps Clk-Q, 400ps setup, 50ps hold  
Airbridge metal provides ultra-low wiring capacitance

### ■ Single Power Supply

(0, -2.6V) or (2.6V, 0)

### ■ Packaging Support

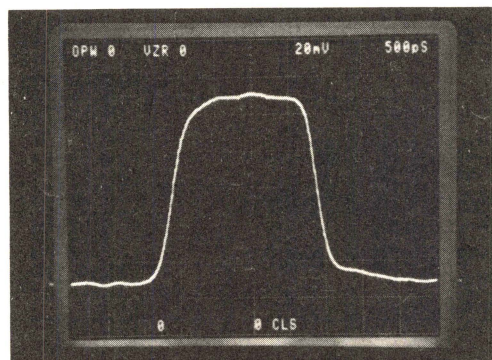
TriQuint designed 132-pin multi-layer ceramic package  
Designed for reflow solder board mount  
50 ohm environment from bond pad to package lead  
High-speed Evaluation Board with quick-connect socket

### ■ Software Support

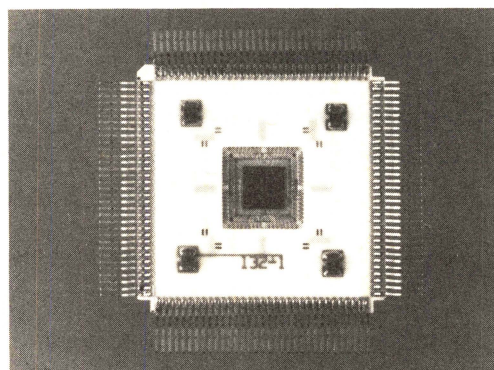
Workstation libraries for Daisy, Mentor and TEK/CAE  
Design Manual with guidelines for logic circuit design  
Complete modeling information on each cell in library

### ■ Typical Development Schedule

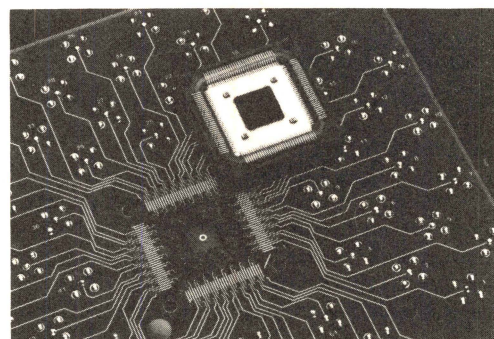
12 to 16 weeks



GHz Speed! 200mV/Div., 500 ps/Div.



132-pin MLC Package and TQ3000 Die



High Speed Evaluation Board (with socket)  
and MLC132 package

For Further Information Contact: TriQuint Semiconductor, Inc.

P.O. Box 4935, Beaverton OR, 97076 (503) 629-3535, -4227 FAX: (503) 645-8067 TELEX: 4742021

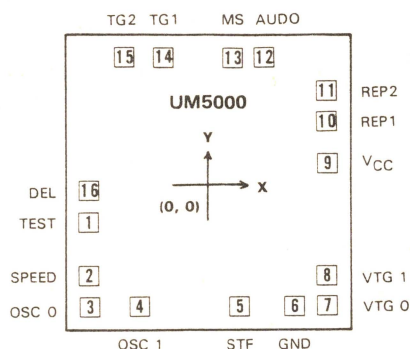


# UM5000 SERIES Voice Synthesizer

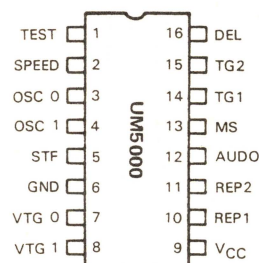
## FEATURES:

- Wide Range of Power Supplies 3~6V
- Speech Repeat Function
- DC, Pulse or Voice Trigger
- 2 Second Speech Capacity
- Speed Function

## BONDING DIAGRAM



## PIN CONFIGURATION



# UM1200 SERIES Gate Arrays

## FEATURES:

- Silicon-Gate 3-Micron HCMOS Technology
- Schottky TTL Speeds, 3.0ns Delay for 2-Input NAND Gate and Interconnection,  $T_A = 25^\circ\text{C}$ , Fanout = 2,  $V_{DD} = 5V$
- Complexity Ranging from 300 to 1100 Gates
- Maximum Pin Counts Ranging from 40 to 62
- I/O TTL/CMOS Compatible
- All Inputs and Outputs Protected from Over-Voltage and Latch-up
- Toggle Rate up to 40 MHz
- Low Power Consumption
- Correct-by-construction Design Methodology
- Fully Supported by UMC CAD System

## PRODUCT OUTLINE

Device Number	Gate Complexity	I/O Buffer	$V_{DD}$ Pads	$V_{SS}$ Pads	Max. Pads	Gate Speed (ns)	
						Typ.	Max <sup>2</sup>
UM1203	300	36	1	1	40	3.0	4.5
UM1206	600	48	1	1	52		
UM1209	900	58	1	1	62		
UM1211	1100						

Notes: 1. 2-Input NAND Gate, Fanout = 2, with Typical Interconnection.

2.  $T_A = 0$  to  $70^\circ\text{C}$ ,  $V_{DD} = 5V \pm 5\%$ .

3. Including 2 Pads without I/O Buffer.

# UA1300 SERIES Gate Arrays

## FEATURES:

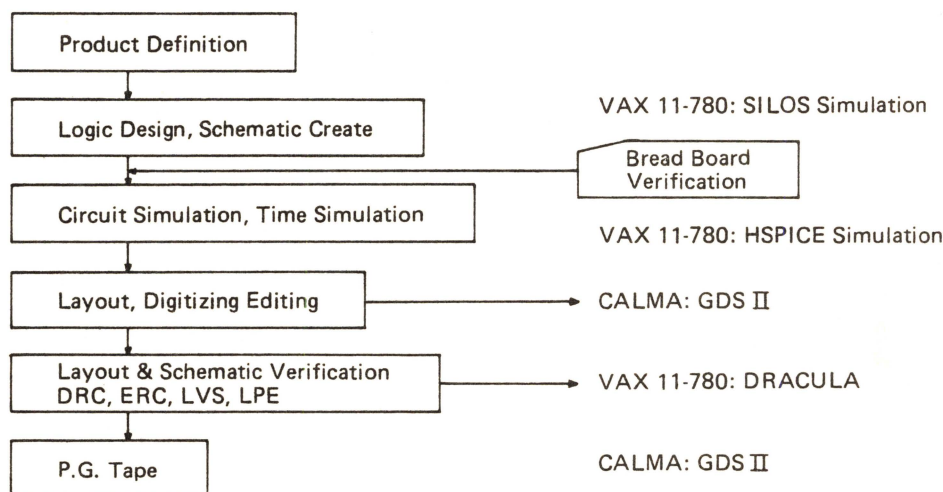
- Silicon-Gate 2.0 Micron (Drawn) Double Metal HCMOS Technology.
- Speeds Higher Than 74/TTL-1.7ns Through 2-Input NAND Gate and Interconnection,  $T_A = 25^\circ\text{C}$ , Fanout = 2,  $V_{DD} = 5\text{V}$
- Optimal Block Structure of 2N and 2P Transistors
- Complexity Ranging from 1300 to 3060 Gate Counts
- Pin Counts Ranging up to 96
- Fully Supported by DAISY System
- Extensive Macrocell and Macrofunction Libraries
- All Non-Power Pads Configurable as Inputs, Outputs, or Bidirectional I/O
- Configurable Output Drive up to 12 mA Under Worst-Case Commercial Conditions
- All Inputs and Outputs Protected from Over-Voltage and Latch up

## PRODUCT OUTLINE

Device Number	Gate Complexity	I/O Buffer	$V_{DD}$ Pads	$V_{SS}$ Pads	Max. Pads	Gate Speed (ns) <sup>1</sup>	
						Typ.	Max. <sup>2</sup>
UM1313	1320	50	2	2	54	1.7	2.5
UM1318	1820	66	2	2	70		
UM1322	2240	80	2	2	84		
UM1330	3060	92	2	2	96		

- Notes: 1. 2-Input NAND Gate, Fanout = 2, with Typical Interconnection.  
 2.  $T_A = 0$  to  $70^\circ\text{C}$ ,  $V_{DD} = 5\text{V} \pm 5\%$ .  
 3. Including 2 Pads without I/O Buffer.

## UMC Full Custom Design Development System



Notes: DRC (Design Rule Check)  
 ERC (Electrical Rule Check)

LVS (Lay-out vs. Schematic)  
 LPE (Lay-out Parameter Extraction)



United Technologies Microelectronics Center manufactures military-standard and semicustom low-power CMOS VLSI circuits for military and aerospace applications. All parts operate over full military temperature range and are screened to MIL-STD-883C.

## Military Standard Products

### MIL-STD-1553 Interface

Product	1553A/B Compatible	Package	Availability	Notes
UT1553B RTI	B	PGA, flatpack	Now	SEAFAC certified
M38510/55501BZX*	B	PGA	Now	SEAFAC certified (UT1553B RTI)
UT1553 RTMP	A/B	PGA, flatpack	Now	SEAFAC certified
UT1760A RTS	B	PGA, flatpack	1Q88	1K x 16 internal RAM
UT1553B BCRT	B	PGA, flatpack	Now	64K addressable memory space
UT1553 BCRTM	B	PGA, flatpack	1Q88	BCRT with bus monitor
UT1553 BCRTMP	A/B**	PGA, flatpack	1Q88	Multiple protocol BCRT
UT63M1XX	A/B	Ceramic DIP, flatpack	1Q88	Fit & function replacement for industry standard transceiver

Available to rad-hard specifications.

\* DESC QPL version of RTI.

\*\* Meets McDonnell Douglas A3818, A5232, A5690, and Grumman Aerospace SP-G-151A specifications.

### MIL-STD-1750

Product	1750A/B Compatible	Package	Availability	Notes
UT1750A RISC MPU	A	PGA, flatpack	Now	Operates in 1750A or RISC mode
UT1750 MMU	A/B	PGA, flatpack	Now	BPU granularity of 1K word blocks

Available to rad-hard specifications.

### Floating-Point Multiplier/ALU

Product	Throughput pipeline/flowthrough	Package	Availability	Notes
UT1732 MUL	10/5 MFLOPS	PGA, flatpack	Now	Supports MIL-STD-1750A, IEEE standard 754, DEC-VAX 32-bit formats
UT1733 ALU	10/4 MFLOPS	PGA, flatpack	Now	

Available to rad-hard specifications.

## Semicustom Products

Our 1.5-micron and 3.0-micron standard and radiation-hardened gate array families are specifically designed for military and aerospace customers using UTMC's comprehensive VAX™-based HIGHLANDSM Design System.

### 1.5μ UTD & UTD-R (Rad-Hard)

Part Numbers	Transistor Pairs	Equivalent Usable Gates	Availability	I/O Circuits (Maximum)	Total Pads
UT116DR	7774	3400	Now	96	116
UT160DR	13920	6000	Now	136	160
UT180DR	17952	7800	Now	156	180
UT212DR	25350	11000	Now	188	212

(R) denotes rad-hard part number.

### 3.0μ UTB & UTB-R (Rad-Hard)

Part Numbers	Transistor Pairs	Equivalent Usable Gates	Availability	I/O Circuits (Maximum)	Total Pads
UT040BR	2240	1000	Now	36	40
UT068BR	5607	2400	Now	60	68
UT084BR	7337	3200	Now	76	84
UT124BR	13393	5800	Now	112	124
UT144BR	17490	7600	Now	132	144

(R) denotes rad-hard part number.

## Radiation-Hardened Capabilities

UTMC's low-temperature processing techniques enhance the total-dose radiation hardness of both the gate and field oxides. These techniques also maintain the circuit density and reliability of our military-standard gate array products. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced silicon gate double-level-metal CMOS process. Features include:

#### UTB-R

- Total dose  $2 \times 10^6$  rads (Si) to data sheet specification
- Total dose  $10^6$  rads (Si) functional
- Dose rate upset  $10^9$  rads(Si)/sec
- Dose rate latchup greater than  $10^{10}$  rads (Si)/sec
- Neutron fluence  $10^{14}$  N/cm

#### UTD-R

- Total dose  $10^6$  rads (Si) to data sheet specification
- Total dose  $10^7$  rads (Si) functional
- Dose rate upset  $10^9$  rads(Si)/sec
- Dose rate latchup greater than  $10^{10}$  rads (Si)/sec
- Neutron fluence  $10^{14}$  N/cm



# VL7000/VL8000 Silicon Compilation



**VTC Incorporated**  
Performance, Pure & Simple.™

## Features

- Automated Layout Compilation and Routing
- Rapid Architectural Tradeoffs
- Placement, Pinout and Packaging Aids
- Interactive Simulation and Timing Analysis
- VTC's 1-Micron and 1.6-Micron CMOS Processing
- VTC Offers Rad-Hard 1 $\mu$  CMOS Process Variant as an Option (Total Dose of 10<sup>6</sup> Rads (Si) )

## SCSC/VTC Partnership

VTC offers access to the GENESIL™ design system from Silicon Compilers Systems Corporation (SCSC). The concept of silicon compilation was pioneered by SCSC. It has greatly extended the original Mead-Conway-Johanssen approach (developed at the California Institute of Technology) to an integrated design environment capable of producing very complex working chips in minimum time.

The VTC/SCSC partnership allows customers access to VTC's advanced 1.0 and 1.6-micron CMOS processes while using the wide variety of available GENESIL capabilities.

## Designing with GENESIL

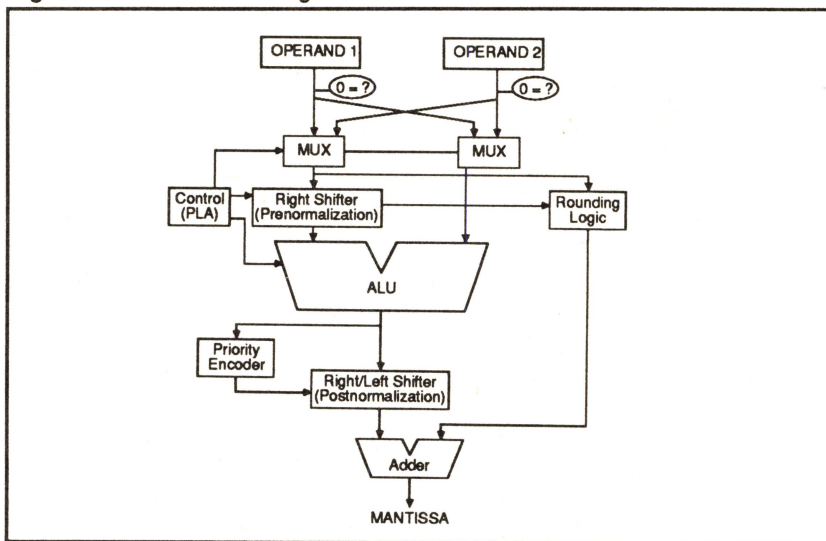
Access to the power of GENESIL can take one of two forms depending on the designer's experience with integrated circuit design. Although design expertise is not essential when using GENESIL, it simplifies the chip compilation process. Therefore, those familiar with chip design can design directly on the GENESIL system, while those with less experience can use VTC's design expertise to tap GENESIL's resources.

## Complex Architectures

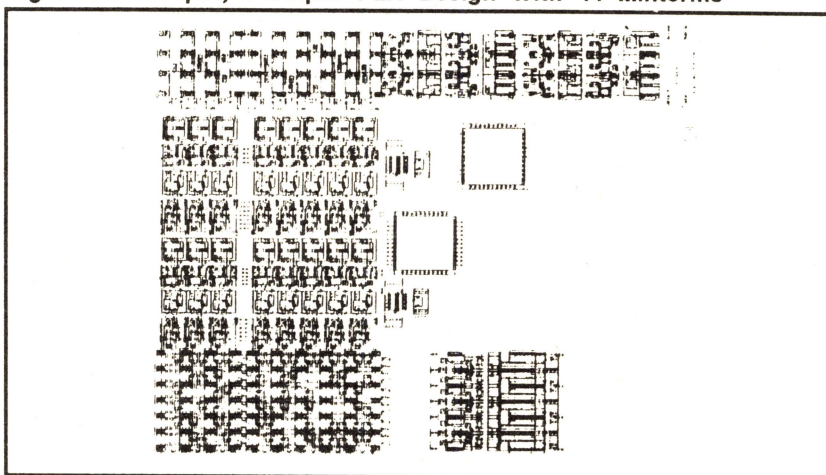
When designing directly on the GENESIL system the engineer can choose from a large array of standard functions to synthesize the most complex architectures. The list includes the following groups:

- Parallel Datapath Module
- RAM (up to 8K bits)
- ROM (up to 128K bits)
- FIFO
- PLA
- Random Logic Functions
- Pads
- External Functions

**Figure 1: Mantissa Design Path**



**Figure 2: 10-Input, 9-Output PLA Design With 44 Minterms**



## GENESIL Features

While on the surface this appears to be a standard cell approach, the GENESIL is different in three important respects. These can be illustrated in the design of the mantissa section for an IEEE floating-point chip (see Figure 1).

First, the function is standardized but the size is not. A RAM, ROM or PLA of exactly the desired size can be synthesized rather than choosing the closest available fit. This provides better use of valuable silicon area. Figure 2 illustrates a 10-input, 9-output PLA design with 44 minterms compiled in just a few minutes with GENESIL.





The second major feature of the system is the ability to design at a higher architectural level than interconnecting primitive blocks. The data path module allows rapid synthesis of an arbitrary-width path (up to 40 data bits) with two standard inputs, two buses, and includes functions such as:

- Priority Encoders
- ALUs
- MUXs
- Latches
- Zero Flags
- Barrel Shifters
- Sign Extenders.

Timing is checked automatically for consistency so the entire module is correct by construction. Figure 3 shows the layout for the mantissa.

A third advantage of the GENESIL system is its integrated nature. Diverse tasks such as adding pads, module pinout and placement, and timing analysis are on-line—not afterthoughts.

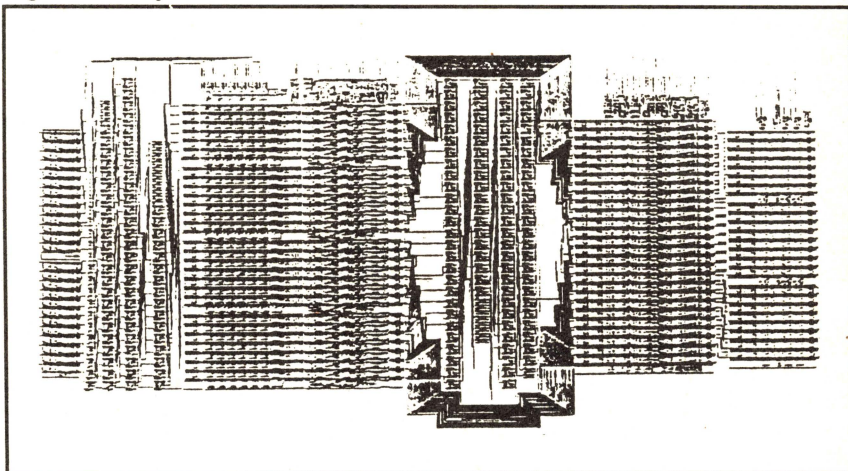
#### **Advantages of GENESIL at VTC**

Of course, arbitrary complex functions can still be synthesized from available primitive cells as in a more conventional approach. The advantage of GENESIL is that the cells can be interconnected rapidly and automatically. Figure 4 shows the 27-bit right/left shifter containing more than 1200 transistors which was completely specified, placed and routed in only a few hours on GENESIL.

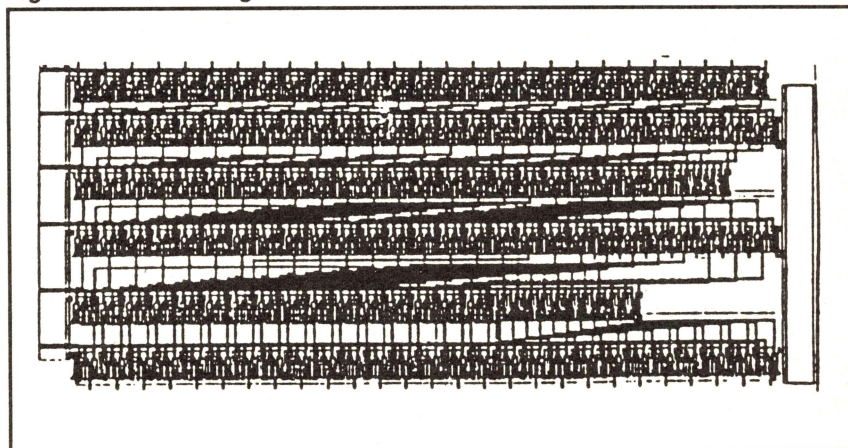
The VTC partnership offers rapid synthesis of complex designs and access to VTC's state-of-the-art CMOS processing.

Using VTC for turnkey design offers one additional advantage. Based on specific customer requirements, VTC can create critical cells and add them to the GENESIL system. This gives access to all the routing and simulation capabilities of GENESIL while providing improved chip density and circuit performance.

**Figure 3: Layout of Mantissa**



**Figure 4: 27-Bit Right/Left Shifter**





# VL5000

## 1-Micron CMOS Standard Cell Library



**VTC Incorporated**  
Performance, Pure & Simple.™

### Features

- 1-Micron CMOS with 2-Layer Metal
- Gate Delays Less than 575ps, (2-Input NAND, Fanout of 2)
- Fully Characterized Cells with Models
- High-Performance Macro Families
- Commercial and Rad-Hard Processing
- Rad Hard to Total Doses of  $10^6$  Rads (Si)
- Fully Integrated CAD System
- Positioned to Handle 50K Gate-Equivalent Complex Chips
- Over-the-Cell Routing to Optimize Layout

### Description

The VL5000 standard cell library uses 1-micron CMOS technology to guarantee state-of-the-art performance levels. VTC's CMOS technology features 0.9 $\mu$  effective channel lengths and typical gate delays of less than 575 picoseconds.

Unlike traditional cell libraries, performance has been optimized for driving large fanouts and long interconnects which are characteristic of devices with over 20K gates.

Also, features such as independent buffering of multiple outputs have been added to simplify CAD and minimize performance degradations due to variable fanouts.

Robust output drive reduces design concerns such as slow propagation delays, signal skews, and degraded transition times (problem often encountered in less performance-oriented cell libraries).

### Rad-hard

The 1-micron technology can be radiation hardened to total doses of  $10^6$  rads(Si). In addition, the cell library uses design practices that reduce radiation sensitivity and maximize latch-up immunity.

### Designs

VTC's 1-micron standard cell library is positioned to handle chip designs in the 5K to 50K gate range. To aid in designs of this complexity, high-performance macro cells such as multipliers, fast RAMs, and 2900 family units are available to complement the SSI and MSI cells in the basic cell library.

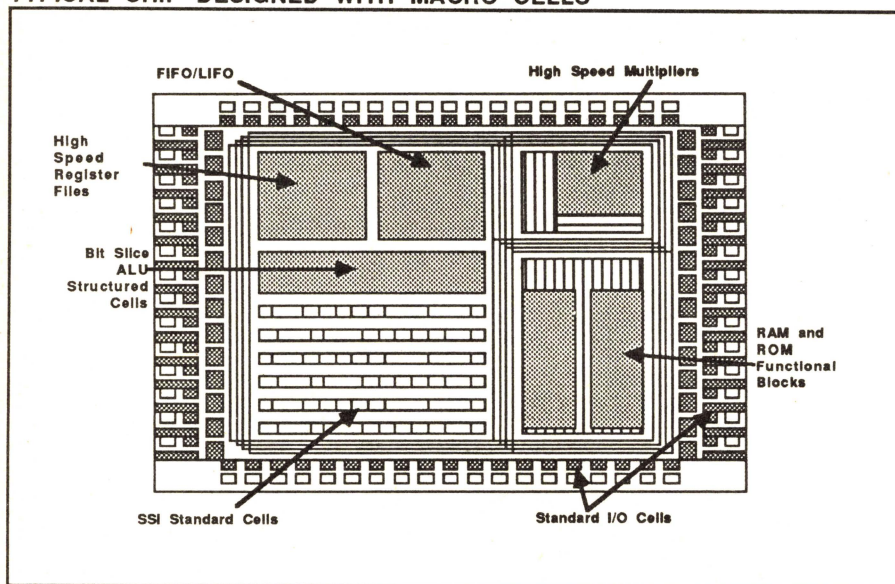
### Routing

VTC's 1-micron CMOS standard cell library is designed to optimize compatibility of the library with current and future CAD tools. For example, to aid in complex VLSI designs that require automated routers, over-the-cell routing is used taking advantage of the 1-micron technology double-level metal capabilities. This facilitates routing time, improves performance and reduces die size.

### CAD

A variety of powerful and popular industry-leading software packages for schematic capture and logic simulation are available, as is auto place and route for layout.

TYPICAL CHIP DESIGNED WITH MACRO CELLS





# VL5000

## 1-Micron CMOS Standard Cell Library



**VTC Incorporated**  
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ASICs/CUSTOM

VTC Incorporated

### MACRO CELLS

NAME	DELAY TIMES (TYP)	
LSI MACROS		
2901 4-Bit Slice	A,B address to Y	19ns
29101 16-Bit Slice	A,B address to Y	23ns
16 x 16 Multiplier	Clocked Multiply Time	30ns
16 x 16 Multiplier Accumulator	Multiply Accumulate	30ns
2910 12-Bit Microsequencer	D Input to Y Output	14ns
MSI MACROS		
2 to 4 Decoder	IN to F	1.35ns
3 to 8 Decoder	IN to F	1.82ns
4-Bit Priority Encoder	IN to FO	1.68ns
4-Bit Synchronous Up/Down Counter	C to Q <sub>n</sub>	2.0ns
	C to C <sub>AB</sub>	3.9ns
4-Bit Shifter	C <sub>n</sub> , I <sub>n</sub> to F <sub>n</sub>	1.28ns
4-Bit Adder	A <sub>n</sub> , B <sub>n</sub> to S <sub>n</sub>	3.78ns
4-Bit Comparator	E to FO	.58ns
10-Bit Priority	IN to F	3.1ns
16-Bit ALU	R,S, to B	8.0ns
2:1 Multiplexer	A to F	0.8ns
4:1 Multiplexer	A,B, to F	2.37ns
8:1 Multiplexer	A,B,C to F	2.79ns
SRAM/ROM		
512 x 8	A <sub>n</sub> to O <sub>n</sub>	20ns
256 x 8	A <sub>n</sub> to O <sub>n</sub>	20ns
256 x 16	A <sub>n</sub> to O <sub>n</sub>	18ns
256 x 32	A <sub>n</sub> to O <sub>n</sub>	18ns
256 x 64	A <sub>n</sub> to O <sub>n</sub>	18ns
128 x 16	A <sub>n</sub> to O <sub>n</sub>	16ns
128 x 32	A <sub>n</sub> to O <sub>n</sub>	16ns
128 x 64	A <sub>n</sub> to O <sub>n</sub>	16ns
REGISTER FILE - SINGLE AND DOUBLE PORT		
16 X 16	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	7.0ns
16 X 32	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	9.0ns
16 X 8	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	5.0ns
32 X 16	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	7.0ns
32 X 32	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	9.0ns
32 X 8	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	5.0ns
64 X 8	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	5.0ns
64 X 16	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	7.0ns
64 X 32	A <sub>n</sub> , B <sub>n</sub> to F <sub>An</sub> , F <sub>Bn</sub>	9.0ns
PLA*		
16 IN, 8 OUT, 16 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	9ns
16 IN, 8 OUT, 32 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	10ns
16 IN, 16 OUT, 16 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	10ns
16 IN, 16 OUT, 32 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	11ns
16 IN, 24 OUT, 16 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	12ns
16 IN, 24 OUT, 32 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	12ns
8 IN, 8 OUT, 8 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	9ns
8 IN, 8 OUT, 16 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	9ns
8 IN, 16 OUT, 8 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	10ns
8 IN, 16 OUT, 16 MINTERMS	A <sub>n</sub> to O <sub>n</sub>	10ns

\*Arbitrary sizes can be compiled upon request.



# VL3000 6GHz Linear/Digital Bipolar Cell Library



**VTC Incorporated**  
Performance, Pure & Simple.™

## Features

- Linear Functions: Amplifiers, Comparators, DACs, Line Drivers, Line Receivers, Charge Pumps, VCO
- Digital Functions: Gates, Flip-Flops, Decoders—Two Power/Speed Levels for Optimum Performance
- Memory Functions: Dual Port RAMs
- LSI Functions: Look Ahead Carry Generator, 4-bit ALU, Priority Interrupt Encoder
- 1.7nsec ECL Comparators
- TTL Advanced Schottky and/or ECL 10KH I/O Levels
- Component Library Available to Create Unique or Proprietary Functions
- Amplifier Bandwidth to 500MHz
- Digital Clock Rates to 1GHz
- Suitable for  $\pm 5V$  Supplies
- Available in Industry-Standard Packages
- Operational Over Full Military Temperature Range
- Samples Available in 10 Weeks
- High Density 2-Micron Process
- True Vertical PNP Transistor,  $f_T = 1GHz$
- NPN Transistors,  $f_T = 6GHz$  Minimum

## Applications

- Peripherals
- Telecommunications
- Automatic Test Equipment
- Local Area Networks
- Analog Signal Processing
- Linear/Digital Subsystems
- Linear LSI Subsystems
- Instrumentation
- High-Speed Video
- RF/UHF Systems

## Description

The VL3000 6GHz Linear/Digital Cell Library contains a wide variety of predesigned linear, digital and memory functions which provide the designer with versatile, cost-effective methods for LSI circuit design. With the VL3000, linear and digital circuits can be mixed on the same chip to maintain high performance, without having to design at the transistor level.

The well-defined, basic linear functions (i.e. amplifiers, comparators, etc.) can be used directly to convert discrete designs into LSI linear designs.

The digital cells have two power/speed levels that allow optimal performance trade-offs. The VL3000 LSI cells include direct replacements for several 2900 family products, as well as enhanced versions of several 10KH parts. The input and output cells offer both TTL and ECL 10KH compatibility.

Included as a subset to the VL3000 cell library is a component library for custom cell design, which allows designs of unique or proprietary circuits from predefined transistors, resistors, and capacitors.

The VL3000 is fabricated with VTC's advanced CBP semiconductor process which provides low noise, wide bandwidth linear circuits, and high-speed digital and memory circuits. The dual-metal, high density cells are structured to minimize silicon area, and to facilitate interconnect and routing. This means increased performance and economical chip size.

## Design Philosophy

The VL3000 cell library was developed for applications requiring maximum linear performance or high digital speeds, or both. The linear cells were designed primarily for use with  $\pm 5V$  or 5V power supplies allowing for full digital compatibility. VTC's complementary bipolar process (CBP) provides linear performance that exceeds typical  $\pm 15V$  circuits. For example, op amps in this library have slew rates ranging from 30 to 150V/ $\mu sec$  minimum and unity gain buffer cells have slew rates to 2500V/ $\mu sec$ .

The digital cells in the VL3000 use current mode logic (CML) for fast propagation delays and three levels of series gating. These cells range in complexity from OR gates to a 4-bit ALU. As with the linear cells, the digital cells are capable of flexible power supply configurations and -5.2V to 0V to +0.0V options are available.

## LINEAR CELLS

NAME	AREA MILS <sup>2</sup>	$I_{OC}$ MA	SUPPLIES $V_{OC} - V_{EE}$
<b>AMPLIFIERS</b>			
VA705	371	7	10( $\pm 5$ ), 10( $\pm 6$ )
VA707	371	7	10( $\pm 5$ ), 10( $\pm 6$ )
VA708	371	7	10( $\pm 5$ ), 10( $\pm 6$ )
VA703	622	6	10( $\pm 5$ ), 12( $\pm 6$ )
VA713	622	25	10( $\pm 5$ ), 12( $\pm 6$ )
<b>BUFFERS</b>			
VA003	605	30	10( $\pm 5$ ), 12( $\pm 6$ )
VA033	605	33	10( $\pm 5$ ), 12( $\pm 6$ )
<b>COMPARATORS</b>			
VC7695	—	20	10( $\pm 5$ )
VC7696	456	—	—

NAME	AREA MILS <sup>2</sup>	$I_{OC}$ MA	SUPPLIES $V_{OC} - V_{EE}$
<b>DAC</b>			
VC512	5000	40	10( $\pm 5$ )
<b>REFERENCES</b>			
BGBROKAW	129	1	5, 10, 12
PTATCURS	140	1	5, 10, 12
<b>SPECIAL FUNCTIONS</b>			
ESDCLAMP	27.4	0	5, 10, 12
QPUMP	725	22.5	+5 & +12
VCO	804	14.5	+5 & +12
ACSWITCH	407	11.5	+5 & +12
PHASEDET	365	5.4	5
DELAYPLL	2482	20.8	5



# VL3000 6GHz Linear/Digital Bipolar Cell Library



**VTC Incorporated**  
Performance, Pure & Simple.™

## DIGITAL CELLS

Typical Performance (5V, T<sub>A</sub> = 25°C, Fanout Of 1)

NAME	HIGH		
	t <sub>p</sub> Sec	P <sub>m</sub> W	Area (mil <sup>2</sup> )
<b>SIMPLE GATES</b>			
2 Input OR	420	2.25	16.46
3 Input OR	420	2.25	23.80
4 Input OR	440	2.25	23.80
2 Input OR-NOR	420	2.25	16.46
3 Input OR-NOR	430	2.25	23.80
4 Input OR-NOR	465	2.25	23.80
3 Input AND	805	2.25	24.91
2 Input AND-NAND	600	2.25	24.02
2-2 OR-AND-Invert	660	2.25	28.03
3-3 OR-AND-Invert	700	2.25	32.03
2 Input EX-OR	530	2.25	31.14
<b>FLIP-FLOPS</b>			
Data Latch W/Reset	675	2.25	28.03
Set Reset Latch Overriding Reset	650	2.25	25.58
Data Latch, Multiplexed Data Inputs	615	2.25	36.92
Data Flip-Flop With Multiplexed Data Input	705	4.50	55.61
Data Flip-Flop With Reset	875	4.50	50.26
Toggle Flip-Flop, Asynchronous Reset	880	11.25	93.42
JK Flip-Flop, Asynchronous Reset	880	11.25	93.42
<b>INPUT/OUTPUT BUFFERS</b>			
10KH Input Buffer	450	2.34	22.67
Differential Input Receiver	475	3.90	36.09
Inverting 10KH Output Buffer	1500	19.24	37.48
Non-Inverting 10KH Output Buffer	1500	19.24	37.48
Differential Output Driver	1100	19.24	33.78
Inverting and Non-Inverting TTL Input Buffer	325	4.50	24.98
Inverting Bistate TTL Output Buffer	4150	10.00	97.62
Non-Inverting Bistate TTL Output Buffer	4150	10.00	97.62
Inverting Tristate TTL Output Buffer	4450	10.00	103.87

Typical Performance (5V, T<sub>A</sub> = 25°C, Fanout Of 1)

NAME	HIGH		
	t <sub>p</sub> Sec	P <sub>m</sub> W	Area (mil <sup>2</sup> )
Non-inverting Tristate TTL Output Buffer	4450	10.00	152.60
Tristate Output Buffer Enable Gate	3000	10.30	68.71
Inverting Open Collector TTL Output Buffer	9400	10.00	139.33
Non-Inverting Open Collector TTL Output Buffer	9400	10.00	139.33
<b>MSI AND LSI FUNCTIONS</b>			
Decoder 1 of 4	470	2.25	31.14
Decoder 1 of 8	870	4.50	80.30
MUX 2 Input (A)	475	2.25	24.47
MUX 2 Input (B)	450	2.25	24.47
MUX 4 Input	575	2.25	49.38
Shift Register, 4 Bit	1000	90.00	746.00
Counter, 4 Bit	1000	90.00	782.00
Comparator, 4 Bit	1300	65.50	605.00
Carry Look Ahead, 4 Bit	1100	304.00	339.00
Parity Generator Checker, 9 Bit	2600	32.00	251.00
Full Adder, 2 Bit	1130	7.02	56.05
Priority Interrupt Encoder	1650	83.60	542.00
2901, 4 Bit ALU	2000	242.00	2542.00
Ram, 16 x 4 Dual Port	2000	245.00	2779.00
<b>SPECIAL PURPOSE</b>			
Level Shift Down L	110	0.75	16.68
Level Shift Down M	60	2.25	16.68
Level Shift Down H	40	8.00	18.46
Clock Driver	505	38.50	72.51
Signal Buffer, Level A	350	9.36	16.46
Shifter P to N	780	9.12	45.10
Shifter N to P	3.50	17.7	16.46
<b>BIAS GENERATORS</b>			
Master Bias	—	28.08	250.53
Internal Bias	—	1.60	47.42
TTL Reference	—	11.70	22.21



# VL2000 High-Performance Bipolar Digital Cell Library



**VTC Incorporated**  
Performance, Pure & Simple.™

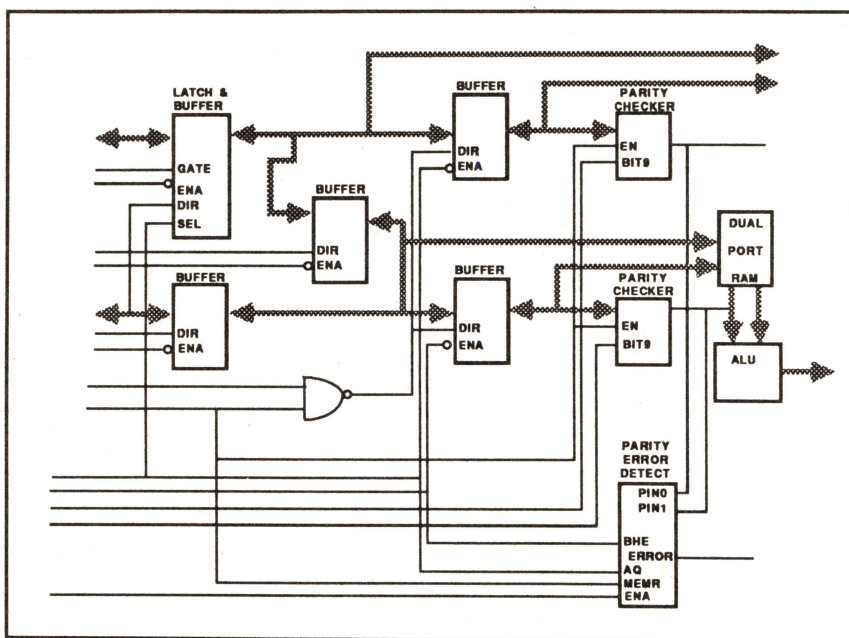
## Features

- Ultra High Gate Speed:
  - High Power Option, 1 Load = 440pSec
  - Low Power Option, 1 Load = 800pSec
- Low Power:
  - 1000 Gate equivalent, 40-Pin Circuit = 1.0 Watt Typical\*
  - 4000 Gate equivalent, 84-Pin Circuit = 3.0 Watt Typical\*
- High Density 2- Micron Process
- Digital Clock Rates to 500MHz
- Cell Library of Digital Functions
- Two Speed/Power Options for Most Cells
- ECL 10KH or TTL Input/Output Available
- Commercial or Military Temperature Range With Full Characterization
- Voltage Compensated ECL 10KH Compatibility
- Mainframe, Workstation or PC-Based
- Suitable for +5, -5 or -5.2 Volt Supplies
- Available in Industry-Standard Packages

*\*Based on one-third of the cells using the high power option and two-thirds of the cells using the low power option; input/outputs evenly split.*

## Description

The VL2000 High Performance Bipolar Digital Cell Library provides the ultra high-speed logic functions at low power levels. The VL2000 library contains a wide selection of digital functions, memory cells and either ECL 10KH or TTL inputs or outputs. The I/O cells can be mixed on any given design.



Typical VL2000 Application

Most logic cells have two-speed/power levels, allowing speed to be traded for power dissipation as required in the design. Critical paths can use fast, high-power cells, while the more numerous noncritical paths can use slower, low-power cells.

The VL2000 has design options that are mainframe, workstation or personal computer-based, and it provides the systems designer a simple, straight-forward means to integrate either new or existing designs.



# VL2000 High Performance Bipolar Digital Cell Library



**VTC Incorporated**  
Performance, Pure & Simple.™

## DIGITAL CELLS

TYPICAL PERFORMANCE ( $5_V, T_A = 25^\circ\text{C}$ , Fanout of 1)			
NAME	HIGH		
	t,pSec	P,mW	AREA (mil <sup>2</sup> )
<b>SIMPLE GATES</b>			
2 Input OR	420	2.25	16.46
3 Input OR	420	2.25	23.80
4 Input OR	440	2.25	23.80
2 Input OR-NOR	420	2.25	16.46
3 Input OR-NOR	430	2.25	23.80
4 Input OR-NOR	465	2.25	23.80
3 Input AND	805	2.25	24.91
2 Input AND-NAND	600	2.25	24.02
2-2 OR-AND-Invert	660	2.25	28.03
3-3 OR-AND-Invert	700	2.25	32.03
2 Input EX-OR	530	2.25	31.14
<b>FLIP-FLOPS</b>			
Data Latch W/Reset	675	2.25	28.03
Set Reset Latch Overriding Reset	650	2.25	25.58
Data Latch, Multiplexed Data Inputs	615	2.25	36.92
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Data Flip-Flop With Reset	875	4.50	50.26
Toggle Flip-Flop, Asynchronous Reset	880	11.25	93.42
JK Flip-Flop, Asynchronous Reset	880	11.25	93.42
<b>INPUT/OUTPUT BUFFERS</b>			
10KH Input Buffer	450	2.34	22.67
Differential Input Receiver	475	3.90	36.09
Inverting 10KH Output Buffer	1500	19.24	37.48
Non-Inverting 10KH Output Buffer	1500	19.24	37.48
Differential Output Driver	1100	19.24	33.78
Inverting and Non-Inverting TTL Input Buffer	325	4.50	24.98
Inverting Bistate TTL Output Buffer	4150	10.00	97.62
Non-Inverting Bistate TTL Output Buffer	4150	10.00	97.62
Inverting Tristate TTL Output Buffer	4450	103.87	103.87

## DIGITAL CELLS (continued)

TYPICAL PERFORMANCE ( $5_V, T_A = 25^\circ\text{C}$ , Fanout of 1)			
NAME	HIGH		
	t,pSec	P,mW	AREA (mil <sup>2</sup> )
Non-inverting Tristate TTL Output Buffer	4450	10.00	152.60
Tristate Output Buffer Enable Gate	3000	10.30	68.71
Inverting Open Collector TTL Output Buffer	9400	10.00	139.33
Non-Inverting Open Collector TTL Output Buffer	9400	10.00	139.33
<b>MSI AND LSI FUNCTIONS</b>			
Decoder 1 of 4	470	2.25	31.14
Decoder 1 of 8	870	4.50	80.30
MUX 2 Input (A)	475	2.25	24.47
MUX 2 Input (B)	450	2.25	24.47
MUX 4 Input	575	2.25	49.38
Shift Register, 4 Bit	1000	90.00	746.00
Counter, 4 Bit	1000	90.00	782.00
Comparator, 4 Bit	1300	65.50	605.00
Carry Look Ahead, 4 Bit	1100	304.00	339.00
Parity Generator Checker, 9 Bit	2600	32.00	251.00
Full Adder, 2 Bit	1130	7.02	56.05
Priority Interrupt Encoder	1650	83.60	542.00
2901, 4 Bit ALU	2000	232.00	2542.00
Ram, 16 x 4 Dual Port	2000	245.00	2779.00
<b>SPECIAL PURPOSE</b>			
Level Shift Down L	110	0.75	16.68
Level Shift Down M	60	2.25	16.68
Level Shift Down H	40	8.00	18.46
Clock Driver	505	38.50	72.51
Signal Buffer, Level A	350	9.36	16.46
Shifter P to N	780	9.12	45.10
Shifter N to P	3,500	17.7	16.46
<b>BIAS GENERATORS</b>			
Master Bias	—	28.08	250.53
Internal Bias	—	11.70	47.42
TTL Reference	—	1.60	22.21

ASICs/CUSTOM

VTC Incorporated



# VL1000

## Linear/Digital Bipolar Cell Library



**VTC Incorporated**  
Performance, Pure & Simple.™

### Features

- Linear Functions: Amplifiers, Comparators, DACs, References
- Digital Functions: Gates, Flip-Flops, Decoders, Three Power/Speed Levels for Optimum Performance
- Memory Functions: RAM or ROM
- TTL or ECL 10K I/O Levels
- Component Library Available to Create Unique or Proprietary Functions
- Workstation/PC-Based
- Amplifier Bandwidth to 200MHz
- Digital Clock Rates to 60MHz
- Suitable for  $\pm 5$  or 12 Volt Power Supplies
- Available In Most Industry-Standard Packages
- Samples Available in 7 to 10 Weeks

### Description

The VL1000 linear/digital bipolar cell library contains a wide variety of predesigned linear, digital and memory functions, which provide the system designer with versatile, cost-effective methods for LSI circuit design. With the VL1000, the designer can mix linear and digital circuits on the same chip, yet does not have to design at the transistor level in order to maintain high performance.

The well-defined, basic linear functions (i.e., amplifiers, comparators, etc.) can be used directly to convert discrete designs into LSI and VLSI linear designs.

The digital cells have three speed/power levels that allow optimal speed/power trade-off. The input and output cells offer the capability to mix both TTL and ECL10K compatible structures on the same chip.

The VL1000's advanced semiconductor process provides low-noise, wide-bandwidth linear circuits, and high-speed digital and memory circuits. The dual-metal, high-density cells are structured to minimize silicon area and facilitate interconnect and routing. This means increased performance and economical chip size.

### LINEAR CELLS

#### DAC CONVERTERS

Five Bit DAC  
Six Bit DAC  
Seven Bit DAC  
Eight Bit DAC

#### ADC CONVERTERS

Five Bit ADC  
Six Bit ADC  
Seven Bit ADC  
Eight Bit ADC

#### OPERATIONAL AMPLIFIERS

OPAMP-A  
OPAMP-B  
OPAMP-C  
OPAMP-D

#### VOLTAGE REFERENCES

Widlar Bandgap  
Brokaw Bandgap  
10mA Voltage Regulator  
60mA Voltage Regulator  
Widlar 2-Bandgap

#### CURRENT REFERENCES

Zener Current Reference  
External Zener Reference  
PTAT Current Reference  
Bandgap Current Source

#### COMPARATORS

339 Comparator  
CML Compatible Comparator 1  
CML Compatible Comparator 2

#### WIDEBAND AMPLIFIERS

733 Video Amplifier  
592 Video Amplifier

#### SPECIAL PURPOSE CELLS

DAC Bias Source  
PNP Current Mirror  
NPN Current Mirror

### DIGITAL CELLS

#### SIMPLE GATES

ORNOR2  
ORNOR3  
ORNOR4  
ORNOR5  
ORNOR6  
ORNOR7  
ANDNAND2  
ANDNAND3  
EXORNOR2  
ORAND22  
ORAND222  
ORAND33  
ORAND333

#### FLIP-FLOPS

RS LATCH  
D LATCH  
DFF1  
JKFF1  
TFF1  
DFF2  
JKFF2  
DFF1ST

#### SPECIAL PURPOSE

CLOCKBUF  
SIGBUF  
POSNEGSHFT  
SHIFTUP  
CMLTSDR  
XTAL1

#### INPUT/OUTPUT BUFFERS

IB BUFIN  
OB BUFOUT  
OB BUFOUTTS  
OB BUFOUTOC  
IB SCHMITT1  
IBBUFIN10K  
OB BUFOUT10K  
IB BUF10KD  
IB TTLTSDR

#### MSI FUNCTIONS

DECODER 10F4  
DECODER 10F8  
MUX 2TO1  
MUX 4TO1

#### BIAS GENERATORS

VCSGEN  
VBBGEN  
BIASGEN10K



# VJ900 6GHz Analog Master Chip Family



**VTC Incorporated**  
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ASICs/CUSTOM

VTC Incorporated

## Features

- 2 Array Sizes
- Block Architecture
- 2.0-Micron Geometry
- NPN  $f_T$  of 6GHz Minimum
- PNP  $f_T$  of 1GHz Minimum
- Resistors, 250 $\Omega$  to 14K $\Omega$
- On-Chip Oxide Capacitors
- Suitable for  $\pm 5V$  or 12V Power Supplies
- Economical Chip Sizes
- Two-Layer Metal for Excellent Utilization and Routability
- Accommodates up to 28 pins
- Separate Resistor Tubs for Dual Positive Power Supply Applications
- High Current Output Transistors for Driving Low Off-Chip Impedances
- Compatible with Any CAD System
- Fast Turn-Around

## Applications

- Disk Drive Subsystems
- Communications
- Analog Signal Processing
- Linear Subsystems
- Linear LSI Systems
- High-Speed Video Graphics
- ATE

## Description

The VJ900 analog master chips are a family of versatile, high-performance, bipolar circuits, containing diodes, transistors, resistors and capacitors. The components interconnect to define either analog or logic functions.

The chips are ideal for high-performance amplifiers having low noise inputs — for example, in pin drivers for ATE or preamps/amps for disk or tape drives.

The VJ900 design system can be utilized on any mainframe or computer that runs standard SPICE. In this way, any CAE schematic capture system can be used to design with the VJ900.

## VJ900 FAMILY MATRIX

FEATURES	VJ910	VJ930	VJ960	VJ970	VJ990
Bonding Pads	16	20	28	52	68
Blocks	1	6	12	24	40
Transistors	30	88	168	328	572
Schottky Diodes	0	52	74	84	132
Resistors	26	180	360	720	1200
Capacitors	0	20	26	28	30
Total Components	56	340	628	1160	1934
Die Size (mils)	47x45	79x75	104x91	134x118	172x149

## Organization

The VJ900 analog master chip family uses a block architecture approach. This organization allows for maximum density and routability.

Each block is identical and composed of a fixed number of components. This technique maximizes the number of symmetry axes for improved device matching and is ideal for dual or quad functions. Each block consists of 6 medium-sized ( $I_C = 1mA$ ) NPN transistors, 4 true vertical PNP transistors ( $I_C = 1mA$ ), 2 small-geometry Schottky diodes (0.2mA), 2 low-noise NPN's, 6 enhancement resistors, and 4 base resistors. On-chip oxide capacitance up to 128pF is available.

The VJ900 family is composed of two products — VJ910, VJ930 — to accommodate different application requirements.

The base and enhancement resistors are implanted and located near the transistors cells for easy connection. The enhancement resistors are available as fixed-tapped devices with 260 $\Omega$ , 521 $\Omega$  and 1042 $\Omega$  increments, while the base resistors have fixed tap values of 2013 $\Omega$ , 4075 $\Omega$  and 8200 $\Omega$ . Both enhancement resistors (P+) and base resistors (P-) have fixed taps.

Components are interconnected using two layers of metal. VTC offers three layers of customization on this product, metal-via-metal.

## Designing

Designing with the VJ900 is straightforward. The design system provides all information necessary to design on any computer that runs SPICE and includes:

- VJ900 User's Guide
- Design Manual

The VJ900 component library simulation models from the User's Guide can be loaded into any computer running SPICE simulation. This allows the designer to choose any SPICE interface.

The VJ900 User's Guide and Design Manual provide detailed information to aid the user in analog master chip design philosophy, circuit design and simulation, and circuit layout. Forms for transmittal of circuit test requirements are also included.

## TESTING

The VJ900 User's Guide specifies requirements for automatic circuit testing.

## SUBMITTAL

When design is complete, the circuit schematic, SPICE netlist, and test specifications are forwarded to VTC where the data is entered into a CAD system, masks and wafers fabricated, and 15 functional prototypes are returned to the customer.



# VJ900

## 6GHz Analog Master Chip Family



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### ELECTRICAL CHARACTERISTICS

#### Transistors

NAME	TYPE	I <sub>c</sub> (mA) (Note 1)	BETA			BVCEs (V)			BVEBO (V)			LVCEO (V)
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN
T10NW	NPN	1.2	75	100	130	15	20	25	4.6	4.9	5.2	6.0
TLN1	NPN	10.0	75	100	130	15	20	25	4.6	4.9	5.2	6.0
T40NW	NPN	22.0	75	100	130	15	20	25	4.6	4.9	5.2	6.0
SDW1	Schottky	.2 (Note 3)										
TVPA8	PNP	1.1	50	75	180	12	—	—	—	>10	—	12
TVPA35	PNP	9.1	50	75	180	12	—	—	—	>10		12
SDGR40	Schottky	40.0 (Note 3)										

#### Resistors

NAME	RESISTOR TYPE	LINEAR TEMPERATURE COEFFICIENT	QUADRATIC TEMPERATURE COEFFICIENT	CAPACITANCE (picofarad) at 0V Bias	TOLERANCE %	
					ABS	MATCH (Note 2)
RA	ENHANCEMENT	5.7E-4	6.9E-6	0.65pF	±20%	0.1%
RB	BASE	7.6E-4	2.05E-6	0.50pF	±20%	0.1%

#### Capacitors

NAME	RESISTOR TYPE	DESCRIPTION	COMMENTS	TOLERANCE
DCAP	OXIDE	1pF Dielectric Oxide Capacitor	Capacitance is Constant at Bias	±20%

#### NOTES:

(1) Switching time and frequency response will be best at maximum I<sub>c</sub>

(2) Adjacent resistors in the same plane (% standard deviation)

(3) Maximum diode current, minimum breakdown voltage is 15V

#### VJ900 BLOCK COMPONENT LIST

BLOCK	TYPE	COMPONENT	NAME	COMMENTS
6	NPN	Medium Transistor, 1.0mA	T10NW	f <sub>T</sub> = 6GHz
2	NPN	Low Noise Transistor, 10mA	TLN1	f <sub>T</sub> = 6GHz
4	PNP	Medium Transistor, 1.0mA	TVPA8	f <sub>T</sub> = 500 MHz
4	Schottky	0.2mA Schottky Diode	SDW1	
6	ENH	1750 Ohm Resistor	RA	Tapped (Note 1)
4	BASE	14.0K Ohm Resistor	RB	Tapped (Note 2)

#### NOTES:

(1) Minimum single value is 260Ω; fixed tap values of 260Ω, 521Ω and 1042Ω

(2) Minimum single value is 2.013KΩ; fixed tap values of 2.013KΩ, 4.075KΩ and 8.200KΩ



# VJ800 800MHz Analog Master Chip Family



**VTC Incorporated**  
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## Features

- 188 to 752 Transistors, 0.5mA to 180mA
- 248 to 992 Resistors, 150Ω to 15KΩ
- 12 to 32 On-Chip Capacitors
- Suitable for ±5V or 12V Power Supplies
- NPN  $f_T$  of 800MHz Minimum
- Economical Chip Sizes
- Two-Layer Metal for Excellent Utilization and Routability
- Accommodates Up to 68 Pins
- Workstation/PC-Based Schematic Entry and Simulation Available

## PARAMETERS

Component	Beta TYP	$BV_{CEO}$ MIN	$BV_{CBO}$ MIN
T3	84	7.0	25
TLN1	86	7.0	25
TLP1	55	13.2	25
T30S	120	7.0	25
T25	65	7.0	25

## Description

The VJ800 analog master chip family is the ideal monolithic solution for many demanding linear applications. The VJ800 family is a set of versatile high-performance bipolar integrated circuits consisting of four members, the VJ800, VJ830, VJ860 and VJ890. Three evaluation chips are available for bench testing. The VJ831 and VJ861 contain discrete LHD components. The VJ801 contains several functional VJ800 circuits.

The VJ800 is organized in one large block. The VJ830, VJ860 and VJ890 devices are symmetrically placed within multiple component blocks. Each VJ800 block contains low-noise NPN transistors and sliding metal tap resistors. Additional high current transistors, Schottky transistors, diodes and junction capacitors are arranged around the grid. For maximum design flexibility, all prediffused VJ800 die have totally uncommitted bonding pads. There are 261 different resistor values available for use in VJ800 designs.

## Designing

Designing with the VJ800 family is straightforward. The design system provides all information necessary to design on a CAD workstation or personal computer and it includes:

- A User's Guide
- Design Manual (LHD Process)
- A Component Library on Diskette with Instruction Manual

The VJ800 family component library is used on a workstation for schematic entry and simulation. Simulation models from the user's guide can be loaded into any computer running SPICE simulation.

The VJ800 family user's guide and design manual provide detailed information to aid the user in analog master chip design philosophy, circuit design and simulation and circuit layout. It also includes the forms necessary for transmittal of circuit test requirements.

## COMPONENT LIST

QUANTITY				DESCRIPTION	MODEL NAME	COMMENTS
VJ800	VJ890	VJ860	VJ830			
310	256	144	64	NPN Small Transistor, 0.5 mA	T3	$f_T = 800$ MHz
168	224	126	56	NPN Medium Transistor, 2mA	T12	$f_T = 800$ MHz
26	32	18	8	NPN Low Noise Transistor, 10mA	TLN1	$f_T = 800$ MHz
5	—	—	—	NPN Power Transistor, 180mA	T50	$f_T = 800$ MHz
—	8	8	4	NPN Power Transistor, 60mA	T25	$f_T = 800$ MHz
32	32	18	8	NPN Small Schottky, 5mA	T3S	$f_T = 800$ MHz
54	72	36	20	NPN Medium Schottky, 8mA	T30S	$f_T = 800$ MHz
5	—	—	—	NPN Power Schottky, 180mA	T50S	$f_T = 800$ MHz
—	8	4	4	NPN Power Schottky, 60mA	T25S	$f_T = 800$ MHz
36	96	54	24	PNP Two Collector, 0.33mA	TLP1	$f_T = 80$ MHz
74	96	54	24	Diffused 300 Ohm Resistor	A	Variable (Note 1)
153	224	126	56	Diffused 600 Ohm Resistor	B	Variable (Note 2)
112	128	72	32	Diffused 1200 Ohm Resistor	C	Variable (Note 2)
293	448	252	112	Implant 3.2K Ohm Resistor	D	Tapped (Note 3)
74	96	54	24	Implant 15K Ohm Resistor	E	Tapped (Note 4)
18	32	18	8	Junction Capacitor, 5pF	JCAP	

Notes: (1) Minimum single value is 130 ohm

(2) Minimum single value is 150 ohm

(3) Fixed tap values of 1.6K and 3.2K ohm

(4) Fixed tap values of 5K, 10K, and 15K ohm





# XC3020 XC3042 XC3090 XC3030 XC3064 Logic Cell™ Array

## Product Brief

### FEATURES

- Fully user-programmable CMOS gate array
  - Flexible internal array architecture
  - 2000–9000 equivalent gates
  - 256–928 Flip-flops
  - 58–144 user Input/Outputs
- Minimum risk
  - Standard product; 100% factory tested
  - No customization
- Second generation architecture
  - 5 input-variable CLB's
  - 2 flip-flops per CLB and IOB
  - Enhanced routing resources
  - Tri-state drivers for wide AND's
- Complete development system support
  - XACT Design Editor
  - XACTOR In Circuit Design Verifier
  - Library and User Macros
  - Delay Path Calculator
  - Logic and Timing Simulation
  - Auto Place/Route
  - Schematic Capture for design entry

### DESCRIPTION

The XC30XX Logic Cell™ Array (LCA) is a second generation, high performance, static, CMOS integrated circuit. Its extendable, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks, a core array of Logic Blocks and an interleaved Interconnect. The XACT development system allows the user to define the logic functions of the device. Schematic capture and auto place-and-route are available for design entry, while logic and timing simulation, and in-circuit debugging are available for design verification. XACT is used to compile the data pattern which represents the configuration program. This data can then be converted to a PROM programmer format file to create the configuration program storage.

The Logic Cell Array's user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The 30XX's resources are

programmed to form networks carrying logic signals among blocks, analogous to traces on a printed circuit board connecting MSI/SSI packages.

### CONFIGURATION MEMORY

Compared with other programming alternatives, static memory provides the best combination of high density, high performance, high reliability and comprehensive testability. The static memory cell used for the configuration memory in the LCA has been designed specifically for high reliability and noise immunity. The basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation the pass transistor is "off" and does not affect the stability of the cell.

The memory cell outputs Q and  $\bar{Q}$  use full Ground and Vcc levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide stability to the cell. Due to the structure of the configuration memory cells they are not affected by extreme power supply excursions or very high levels of alpha particle radiation. In reliability testing no soft errors have been observed, even in the presence of very high doses of alpha radiation.

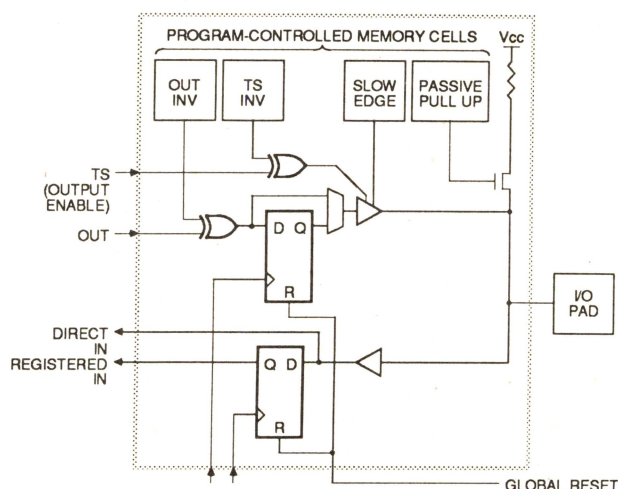


Figure 1. I/O Block

485 02



## I/O BLOCK

Each of the user configurable I/O Blocks (IOB) provides an interface between the external package pin of the device and the internal user logic. The I/O Block includes both registered and direct input paths. Each package pin provides a programmable three-state output buffer which may be driven by a registered or direct output signal. Configuration options allow inversion, slew rate selection and a high impedance pull-up. See Figure 1.

## CONFIGURABLE LOGIC BLOCK

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. Each configurable logic block has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 2. There are: five logic inputs (A–E); a common clock; an asynchronous direct reset; an enable clock; and a direct flip-flop input, all of which may be driven from the interconnect resources. Each CLB also has two outputs which drive interconnect networks. Data input for either flip-flop within a CLB is supplied from the function F

or G outputs of the combinatorial logic, or the block input, data-in.

The combinatorial logic portion of the CLB uses a program memory 32 by 1 table look-up to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each, or a single function of five variables, or some functions of seven variables.

## PROGRAMMABLE INTERCONNECT

Programmable Interconnection resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logical networks. All interconnections between blocks are composed from a grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, allow the configuration program to determine the networks.

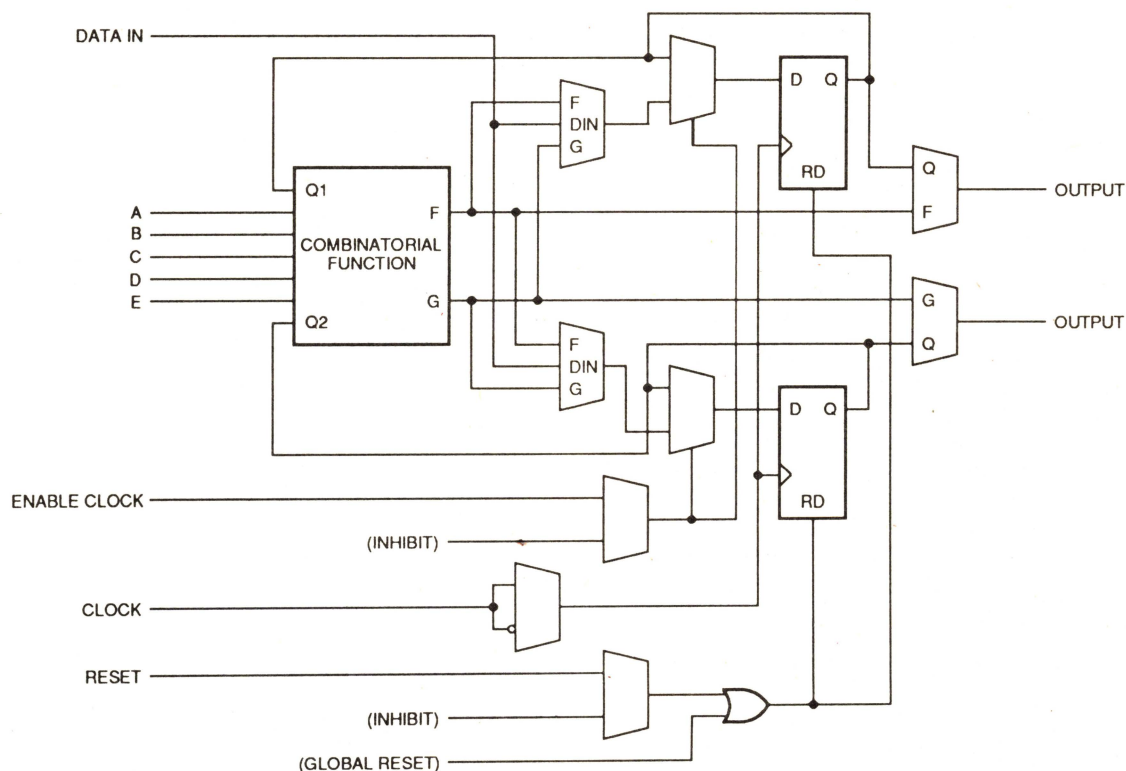


Figure 2. 3000 Series Configurable Logic Block (CLB)





# XC2064 XC2018 LOGIC CELL™ ARRAY

## Product Brief

### FEATURES

- Fully user-programmable:
  - I/O functions
  - Digital logic functions
  - Interconnections
- General-purpose array architecture
- Complete user control of design cycle
- Compatible arrays with logic cell complexity equivalent to 1200 and 1800 usable gates
- Standard product availability
- 100% factory-tested
- Selectable configuration modes
- Low-power, CMOS, static memory technology
- Three performance options: 33 MHz, 50 MHz, 70 MHz
- TTL or CMOS input thresholds
- Complete development system support
  - XACT Design Editor
  - Schematic Entry
  - XACTOR In Circuit Debugger
  - Macro Library
  - Timing Calculator
  - Logic and Timing Simulator
  - Auto Place / Route

### DESCRIPTION

The Logic Cell™ Array (LCA) is a high density CMOS programmable gate array. Its patented array architecture is made up of three types of configurable elements: Input/Output Blocks, Configurable Logic Blocks and Interconnect. The designer can define individual I/O blocks for interface to external circuitry, define logic blocks to implement logic functions and define interconnection networks to compose larger scale logic functions. The XACT™ Development System provides interactive graphic design capture and automatic routing. Both logic simulation and in-circuit emulation are available for design verification.

Part Number	Logic Capacity (usable gates)	Configurable Logic Blocks	User I/O's	Configuration Program (bits)
XC2064	1200	64	58	12038
XC2018	1800	100	74	17878

### PROGRAMMING

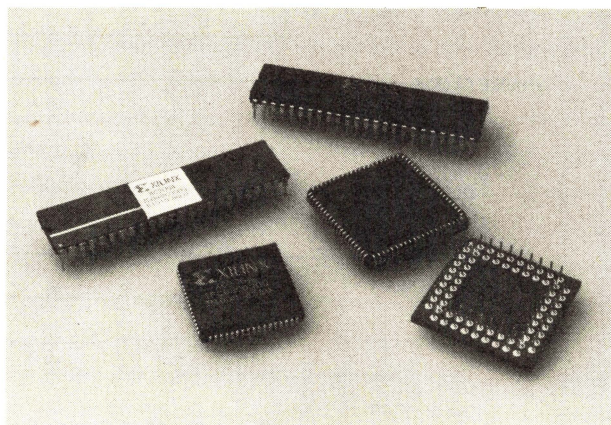
The Logic Cell Array's logic functions and interconnections are determined by a configuration program stored in internal static memory cells. On-chip logic provides for automatic loading of configuration data at power-up or on command. The program data can reside in an EEPROM, EPROM or ROM on the circuit board or on a floppy disk or hard disk.

Several methods of automatically loading the required data are designed into the Logic Cell Array and are determined by logic levels applied to mode selection pins at configuration time. The form of the data may be either serial or parallel, depending on the configuration mode. The programming data are independent of the configuration mode selected.

The Logic Cell Array is available in a variety of logic capacities, package styles, temperature ranges and speed grades.

### INPUT/OUTPUT BLOCK

Each user-configurable I/O block (IOB) provides an interface between the external package pin of the device and the internal logic. Each I/O block includes a programmable input path and a programmable output buffer. It also provides input clamping diodes to provide protection from electro-static damage, and circuits to protect the LCA from latch-up due to input currents.





The input buffer portion of each I/O block provides threshold detection to translate external signals applied to the package pin to internal logic levels. The input buffer threshold of the I/O blocks can be programmed to be compatible with either TTL (1.4 V) or CMOS (2.2 V) levels.

Output buffers in the I/O blocks provide 4 mA drive for high fan-out CMOS or TTL compatible signal levels.

## CONFIGURABLE LOGIC BLOCK

An array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The Logic Blocks are arranged in a matrix in the center of the device. The XC2064 has 64 such blocks arranged in an 8-row by 8-column matrix. The XC2018 has 100 logic blocks arranged in a 10 by 10 matrix.

Each logic block has a combinatorial logic section, a storage element, and an internal routing and control section. Each CLB has four general-purpose inputs: A, B, C and D; and a special clock input (K), which may be driven from the interconnect adjacent to the block. Each CLB also has two outputs, X and Y, which may drive interconnect networks. The Figure below shows

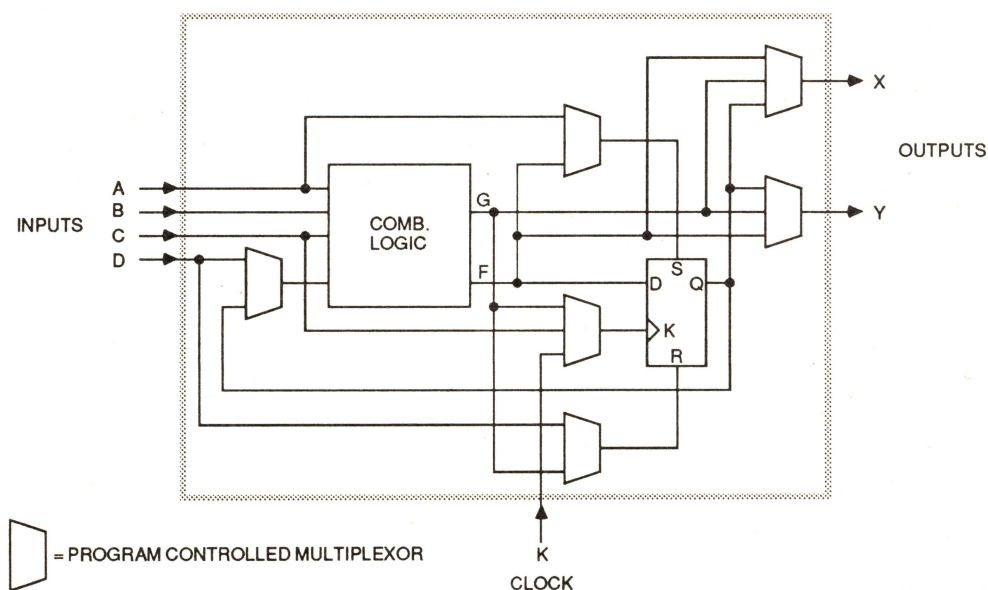
the resources of a Configurable Logic Block.

The logic block combinatorial logic uses a table look-up memory to implement Boolean functions. This technique can generate any logic function of up to four variables with a high speed sixteen-bit memory. The propagation delay through the combinatorial network is independent of the function generated. Each block can perform any function of four variables or any two functions of three variables each. The variables may be selected from among the four inputs and the block's storage element output "Q".

## PROGRAMMABLE INTERCONNECT

Programmable interconnection resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into desired networks. All interconnections are composed of metal segments, with programmable switching points provided to implement the necessary routing. Three types of resources accommodate different types of networks:

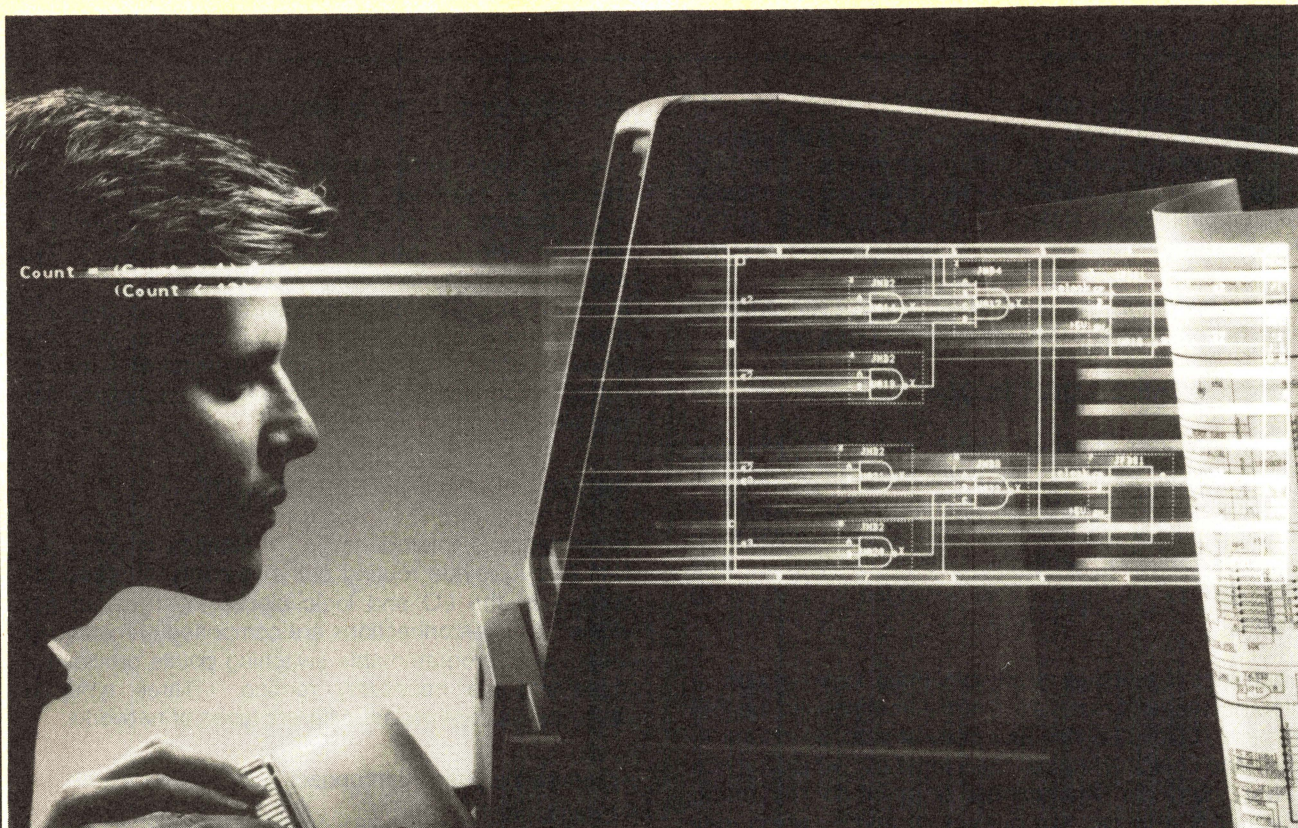
- General purpose interconnect
- Long lines
- Direct connection



### Configurable Logic Block

0010003 4





# AUTOMATIC SCHEMATIC.

## **FUTUREDESIGNER: DRAW LESS. DESIGN MORE.**

Introducing FutureDesigner™ — the only advanced design entry workstation that lets you describe your circuit in compact, high-level terms and create more complex designs faster. FutureDesigner's flexible, new techniques encourage creativity and experimentation, helping you produce innovative products quickly and more accurately.

## **MULTIPLE DESIGN ENTRY MODES FOR SPEED AND FLEXIBILITY.**

Describe your circuit with any combination of structural and behavioral representations. Use schematics to enter the structural portions of the design, such as data paths in a memory array. For portions easier to describe behaviorally, like sequencers or decoders, simply enter equations, truth tables or state diagrams using on-screen input forms.

## **ADVANCED DESIGN VERIFICATION HELPS YOU GET IT RIGHT THE FIRST TIME.**

For the behavioral portions of your design, use FutureDesigner as a "what if" tool to try different design approaches. Immediately verify that your circuit works as you intended. For the structural portions, design check tools detect and help you correct connectivity and other common design errors. Together these features significantly shorten the design iteration cycle.

## **LOGIC SYNTHESIS CONVERTS YOUR EQUATIONS INTO SCHEMATICS.**

Once you've entered equations, state diagrams or truth tables, FutureDesigner's logic synthesizer eliminates redundant circuitry and optimizes your design for size/speed trade-offs. FutureDesigner is the only design entry workstation that will then automatically produce the correct schematics and integrate them with the total structural design.

## **MORE CHOICES IN TECHNOLOGIES, VENDORS AND SYSTEMS.**

FutureDesigner is technology independent. Choose the most convenient mix of TTL, PLDs, gate arrays or other ASICs from a wide range of semiconductor manufacturers. You can easily migrate from one technology to another without redesign.

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# INTRODUCTION TO DESIGN AUTOMATION

This section provides sufficient information for making initial hardware and software selections by furnishing a number of interrelated directories complemented by manufacturers' data.

To locate tools incorporating software, hardware and a computing platform from one company, start with the Workstation Directory, which lists the design tools by name. For third-party software, which is not sold with the system, refer to the Design Tool Interface Directory which shows the hardware-software linkages. If you are searching for suitable tools to run on a given computing platform, consult the Hardware vs. Software Directory. Or if you need tools to do your own semicustom design, use this material in conjunction with the directories in the ASIC/Custom section.

To expand the above, you will find more detailed information in the various Design Tool Directories. And you will find useful system and company information right after all the directories.

## Design Automation Section

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# DESIGN AUTOMATION

What tools are provided on a given workstation?  
Use **WORKSTATION Directory**

What are the capabilities of a particular design tool?  
Use **DESIGN TOOLS Directory**

DESIGN AUTOMATION

## WORKSTATIONS

## DESIGN TOOLS

Front End Design  
Schematic Capture  
Circuit Simulators  
Logic Simulators  
Fault Simulators  
Physical Layout  
Circuit Board  
Gate Array  
Standard Cells  
Full Custom  
PLD Development

Silicon Compilers  
IC Layout Verification  
Hardware Tools  
Physical Modeling  
Circuit Simulation Accelerators  
Logic Simulation Accelerators  
Fault Simulation Accelerators  
IC Prototype Test Systems  
Miscellaneous Design Tools

## DESIGN TOOL INTERFACES

## HARDWARE vs. SOFTWARE

How are design tools linked together?  
Use **DESIGN TOOL INTERFACE Directory**

Which design tools have been ported to a particular computing platform?  
Use **HARDWARE vs. SOFTWARE Directory**

*Which design tools are particularly suited to a selected semicustom device family?*  
Turn to **CUSTOM/SEMICUSTOM Section**

**Turn to the manufacturers' data pages to learn more about their tools and to refine your selections.**



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Acasi Logic Simulator	LIBSIM	4483-1	Automated Systems Circuit Board Layout Tool	PRANCE PRANCE/SIGMA REMOTE	4519-3 4519-4
Acotech Circuit Simulator	ALLSPICE	4468-2	B&C Microsystems Circuit Board Layout Tool Schematic Capture	PCB/DE SCH/DE	4520-1 4453-4
Aida Automatic Test Pattern Generator Fault Simulation Accelerator Fault Simulator Logic Design Rules Checker Logic Simulation Accelerator Logic Simulator Schematic Capture Timing Analyzer for well clocked designs Workstation	Aida ATPG Aida CoSimulator Processor Aida Persimulator Processor Aida Fault Inferencer Aida Fault Simulator Aida Logic Design Rules Check Aida CoSimulator Processor Aida PerSimulator Processor Aida Logic Simulator Aida Design Creation System Aida Timing Verifier Aida Design System	4599-1 4588-1 4588-2 4506-1 4506-2 4611-1 4581-1 4581-2 4483-2 4452-1 4620-3 4410-1	Berne Electronics Circuit Simulator Component Modeling/Parameter Extraction Logic Simulator	ELAN-AC ELAN-Rel ELAN-TR I/CAP ELAN-MOD I/LOGIC	4469-2 4469-3 4469-4 4470-1 4601-1 4484-2
Aldec Fault Simulator Logic Analyzer to Logic Simulator Link Logic Simulator Programmable Device Development System Workstation	HASS FAST SLAV SFLD SLAV/HASS	4506-3 4610-3 4483-3 4555-1 4410-2	Bishop Graphics Circuit Board Layout Tool Schematic Capture Workstation	Pathfinder Quik Circuit Version 4.2 Pathfinder Pathfinder	4520-2 4520-3 4454-1 4413-1
Altera Programmable Device Development System	A + PLUS PLCAD-SUPREME PLDS-SAM	4555-2 4555-3 4556-1	Brainpower Circuit Simulator	DesignScope	4470-2
Analog Design Tools Circuit Simulator Library Addition Safe Operating Conditions Analysis Schematic Capture Workstation	SPICE PLUS Basic Device Library Smoke Alarm Module AnalogWorkbench Circuit Editor PC Workbench Circuit Editor Analog Workbench PC Workbench	4468-3 4609-4 4617-3 4452-2 4452-3 4410-3 4411-1	CAD Group, Inc. (CGI) Behavioral Model Simulator Logic Simulator	SHDL(SALT Hdware Descr. Lang. SALT	4599-4 4484-3
Analogy Circuit Simulator	SABER	4469-1	Cadam Circuit Board Layout Tool Fault Simulator Logic Simulator Schematic Capture Thermal Analysis	Interactive PRANCE IPC Digital Fault Simulation Digital Circuit Simulation CADEX Thermal Analysis (Thermax)	4521-1 4521-2 4507-2 4485-1 4454-2 4619-4
Applicon Circuit Board Layout Tool Fault Simulator Full Custom Layout Tool Logic Simulator Physical Modeler Schematic Capture Standard Cell Layout Tool Workstation	Interactive/Automatic Layout Logic Analysis VLSI Custom Design Editor Logic Analysis Dynamic Hardware Modeler Design Capture VLSI Design Editor Bravo3 Electronic Design Station	4518-1 4507-1 4549-1 4484-1 4574-1 4453-1 4541-1 4411-2 4411-3	CADIC, Inc. Prototype IC Test System	STM4100 Digital VLSI Test Sys. STM5100 Digital VLSI Test Sys. STM5200 Digital Test System	4592-1 4592-2 4592-3
Aptos Systems Circuit Board Layout Tool Workstation	AUTOTOOLS ICD-One RGRAPH	4518-2 4411-4 4412-1	Cadnetix Accelerator for Compilation & Analog Sim Circuit Board Layout Tool Circuit Simulator Drafting Editor Fault Simulator Logic Simulation Accelerator Logic Simulator Manufacturing Workstation Physical Modeler Schematic Capture Workstation	CDX-760 RISC Engine CDX-75000XP Route Engine III Route Editor CDX-3200 2D Drafting Editor Fault Simulation CDX-770 Accel. Digital Design Cadnetix Digital Design CDX 60000S CDX-7950 Physical Modeling Pkg Schematic Editor CDX-3000/CDX-3150 CDX-50000 CDX-50000S CDX-5000A CDX-59000S CDX-5900S CDX-70000 CDX-9300	4597-2 4521-3 4521-4 4470-3 4406-1 4507-3 4581-3 4485-2 4612-1 4574-2 4454-3 4413-2 4413-3 4413-4 4414-1 4414-2 4414-3 4415-1 4415-2
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Augat Circuit Board Layout Tool	QWIKCHECK QWIKDRAW	4518-3 4519-1			



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Calay Systems			Control Data		
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	ZX1000	4416-3	Gate Array Layout Tool	MIDAS	4536-1
			Logic Simulator	MIDAS	4487-2
Calma				SALT(see CAD Group, Inc.(CGI))	4487-3
Circuit Board Layout Tool	BOARD Series	4522-2	Schematic Capture	ED-Schematics	4457-1
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	GDSII	4550-1	Timing Analyzer	CYBERNET*EXPRESS	4422-3
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	Fast Mask Engine	4566-2		MIDAS	4423-2
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	TEXSIM/B	4485-4	DA Systems		
	TSCAN (timing verifier)	4486-1	Interface and Communications	CIM Software	4608-1
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	Logic Examiner	4417-2	Circuit Simulator	DSPICE/ Virtual Lab	4471-4
	Logic Explorer	4417-3	Fault Simulation Accelerator	MegaFAULT	4589-1
	Logic Scribe	4417-4	Fault Simulator	MegaFAULT	4509-1
	Tegastation	4418-1	Full Custom Layout Tool	CHIPMASTER	4551-1
			Gate Array Layout Tool	MegaGATEMASTER	4536-2
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			Circuit Board Layout Tool	PC800 Model 4	4527-1
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Standard Cell Layout Tool	FAIRCAD	4543-2	Logic Simulator	HILO-3 (see Genrad)	4492-1
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Kontron			Micro Linear		
Circuit Board Layout Tool	KAD System	4528-2	Circuit Simulator	PSPICE	4478-1
Laser Film Plotting	Laser Film Plotter	4609-3	Linear Array Layout	FB300 Linear Array Layout	4610-2
Programmable Device Development System	LOG/ic + EPP-80 PLD Programmer	4558-2	Schematic Capture	Linear CAD II	4462-1
Schematic Capture	KAD Editor	4461-3	Workstation	Linear CAD II	4435-3
Workstation	KAD System	4432-1			
Lattice Semiconductor			Micro Power Systems		
Programmable Device Development System	Design Development Kit	4558-3	Workstation	MCAD	4435-4
Logic Automation			MicroSim		
Software Models	SmartModels	4618-1	Analog/Digital Simulation Link	PSpice Digital Files	4597-3
			Circuit Simulator	PSpice	4478-2
			Component Modeling/Parameter Extraction	PSpice Parts	4601-4
			Graphics Post-Processor for PSpice	PSpice Probe	4607-4
			Monte Carlo Analysis of PSpice	PSpice Monte Carlo Analysis	4613-3
			Source Code (Partial) to PSpice	PSpice Device Equations	4618-3
			Modula		
			Workstation	MODULA	4436-1
			Monolithic Memories		
			Programmable Device Development System	PALASM2	4559-1



Manufacturer Function	Tool Name	Page-Col.	Manufacturer Function	Tool Name	Page-Col.
MOSAID			Racal-Redac (Cont'd)		
Component Modeling/Parameter Extraction	MOSFIT	4602-1		VISULA CADAT	4515-1
			Full Custom Layout Tool	ISIS	4551-4
Multiwire East			Logic Simulator	REDSIM CADAT	4496-3
Circuit Board Layout Tool	Design Master on VAX	4529-1		VISULA CADAT	4497-1
	Design Master with Intergraph	4529-2	Physical Modeler	VISULA CATS	4577-2
			Schematic Capture	VISULA Design Entry	4463-3
			Workstation	REDCAD	4439-2
				REDSIM	4439-3
				VISULA 3.0	4439-4
National Semiconductor			Raytheon Semiconductor Div.		
Fault Simulator	Design Automation System	4514-1, 4294	Workstation	Raytheon Design System	4440-1, 4296
Gate Array Layout Tool	Design Automation System	4539-1, 4294			
IC Layout Verification	Design Automation System	4569-4, 4294			
Logic Simulator	Design Automation System	4495-2, 4294			
Schematic Capture	Design Automation System	4462-2, 4294			
Standard Cell Layout Tool	Design Automation System	4545-1, 4294			
Workstation	Design Automation System	4436-2, 4294			
NCR Microelectronics					
IC Layout Verification	VILAY Series	4570-1			
Logic Simulator	VITA Series	4495-3			
Silicon Compiler	VIGEN Series	4562-3			
Workstation	NCR VISYS	4436-3			
Octal					
CAD Database Conversion	Direct CAD Database Converters	4600-2			
Omaton					
Schematic Capture	SCHEMA	4462-3			
Optima Technology					
Circuit Board Layout Tool	OPTIMATE Place and Route	4529-3			
Schematic Capture	OPTIMATE Design	4463-1			
Workstation	OPTIMATE	4437-1			
P-CAD					
Circuit Board Layout Tool	PC-CARDS (PCB-1 and PCB-2)	4529-4			
	PC-CARDS, PLACE, ROUTE (PCB-3)	4530-1			
Logic Simulator	PC-LOGS	4495-4			
Programmable Device Development System	CUPL	4559-2			
	PC-CUPL	4559-3			
Schematic Capture	PC-CAPS	4463-2			
Workstation	CAE-1	4437-2			
	CAE-2	4437-3			
	EDA-1	4437-4			
	PCB-1	4438-1			
	PCB-2	4438-2			
	PCB-3	4438-3			
Plessey					
Fault Simulator	CLASSIC/FAULTS	4514-2			
Gate Array Layout Tool	CLAMP/SCARP	4539-2			
	CLASSIC	4539-3			
Logic Simulator	CLASSIC	4496-1			
Standard Cell Layout Tool	CLASSIC	4545-2			
	Megacell Layout Editor	4545-3			
Praxis Systems					
Behavioral Language for VLSI Design	ELLA	4599-3			
Logic Simulator	ELLA	4496-2			
Workstation	ELLA	4439-1			
ProtoCAD					
Printed Circuit Board Prototyping System	CAD/Magic 3500	4615-4			
Quadtree					
Software Models	Designers' Choice	4618-2			
Quantic Laboratories					
Transmission Line PC Board Simulation	GREENFIELD 2	4621-2			
Racal-Redac					
Circuit Board Layout Tool	REDBOARD	4530-2			
	VISULA	4530-3			
Fault Simulator	REDSIM CADAT	4514-3			



Manufacturer Function	Tool Name	Page-Col.	Manufacturer Function	Tool Name	Page-Col.			
Silicon Compiler Systems (Cont'd)	GENESIL	4564-1	Tektronix CAE Systems	MERLYN-P	4532-3, 4658			
	GENESIS	4564-2		Circuit Board Layout Tool	HSPICE (see Meta-Software)	4480-3, 4658		
	Generator Development Tools	4546-2		Circuit Simulator	SPICE 2G.6 Interface	4481-1, 4658		
	GENESIL	4441-4		Engineering Documentation Package	TekWriter	4606-2, 4658		
	GENESIS	4442-1		Fault Simulator	HILO-3 (see Genrad)	4516-3, 4658		
Silicon Solutions/Zycad			Teradyne	LEIA	4553-2, 4658			
	Fault Simulation Accelerator	Mach 1000F		4590-3	MERLYN-G	4540-2, 4658		
	IC Layout Verification	Fast Mask Engine		4571-4	DRACULA II (see ECAD Inc.)	4573-1, 4658		
	Logic Simulation Accelerator	Mach 1000		4584-2	HILO-3 (see Genrad)	4501-4, 4658		
Silvaco Data Systems				Texas Instruments	HICHIP (see Genrad)	4577-4, 4658		
	Component Modeling/Parameter Extraction	UTMOST			4602-2	Designer's Database (DDSC)	4465-1, 4658	
Silvar-Lisco					The Great Softwestern Company	MERLYN-S	4547-2, 4658	
	Circuit Board Layout Tool	Cal-PC				4532-1	Designer's Worksystem	4443-1, 4658
		OPTIMATE				4532-2	Full Custom WorkSystem	4443-2, 4658
	Full Custom Layout Tool	PRINCESS				4553-1	Gate Array WorkSystem	4443-3, 4658
	Gate Array Layout Tool	GARDS				4540-1	PCB WorkSystem	4443-4, 4658
	IC Layout Verification	DVS				4572-1	Signal Processing WorkSystem	4444-1, 4658
		Parallel DVS				4572-2		
	Interface and Communications	IZYCAD				4609-1		
		Test Systems Strategies/S-L	4609-2					
	Logic Simulator	HELIX	4499-3					
Simucad		LOGIX-SL	4499-4			The Western Design Center		
	Fault Simulator	SILOS	4516-1				Circuit Simulator	CIRCUIT
	Logic Simulator	P-SILOS	4500-2	Logic Simulator			LOGIC	4502-2
		SILOS	4500-3					
	Simulog			Thomson/Mostek				
		Fault Simulation Accelerator	SuperSim		4591-1		SIM	4502-3, 4321
		Logic Simulation Accelerator	SuperSim		4584-3		HIGHLAND 2	4445-1, 4321
	Physical Modeler	SuperSim	4577-3					
	Spectrum Software			Trimeter Technologies				
		Circuit Simulator	MICRO-CAP II		4479-4		Logic Simulator	Logic Consultant
Logic Simulator	MICRO-LOGIC II	4501-1			Microcode Creation and Verification		Microcode Assistant	4613-1
Standard Microsystems Corp.			Unicorn Microelectronics	Workstation				
	IC Layout Verification	STANCOMP		4572-3, 4310				
	Logic Simulator	STANSIM, STANTIME		4501-2, 4310	Silicon Compiler		COMPILE	4564-3
	Wirewrap Board Emulator	STANWIRE		4621-4, 4310				
	Workstation	STANSURE		4442-3, 4310				
Systems Calculations				Valid Logic Systems Inc.				
	Database/Program Management	CircuitBase			4604-1	Circuit Board Layout Tool	Allegro	4533-1, 4660
Tangent Systems						Valid Route/Board Designer	4533-2, 4660	
	Fault Simulator	TANTEST	4516-2		Design Interface and Access Language	DIAL	4604-2, 4660	
Standard Cell Layout Tool	TANCELL	4547-1			Fault Simulator	LASAR 6 (see Teradyne)	4517-2, 4660	
Tatum Labs					Flattens Hierarchical Designs	ValidFLAT	4606-3, 4660	
	Circuit Simulator	EC-Ace	4480-1		Full Custom Layout Tool	ValidBLOCKS	4553-3, 4660	
		ECA-2	4480-2			ValidCOMPOSE	4553-4, 4660	
Logic Simulator	LSS-2	4501-3			ValidLED	4554-1, 4660		
Technology Modeling Associates					GDSII/Valid IC DesignDatabase Translator	ValidCONVERT	4607-3, 4660	
	1-D Process Modeling Program	SUPREM-3	4597-1	IC Layout Verification	ValidCOMPARE/ERC	4573-2, 4660		
	Component Modeling/Parameter Extraction	TOPEX	4602-3		ValidDRC/EXTRACT	4573-3, 4660		
	Device Modeling	CANDE	4604-3	Library Development Tool	ValidEZLIB	4610-1, 4660		
		GEMINI	4605-1	Logic Simulation Accelerator	Realfast	4585-2, 4660		
		PISCES-2B	4605-2		Realmodel	4585-3, 4660		
		SEDAN-2	4605-3	Logic Simulator	ValidSIM	4503-2, 4660		
	Process Modeling	SUPRA	4616-1		ValidTIME	4503-3, 4660		
	Process Simulation Program	DEPICT-1	4616-2	Logical Compiler	ValidCOMPILER	4611-3, 4660		
				Logical-to-Physical Database Translator	ValidPACKAGER	4611-4, 4660		
Tektronix			Physical Modeler	Networked Realchip	4578-2, 4660			
	Prototype IC Test System	DAS9100	4596-2		Realchip	4578-3, 4660		
				Realmodel	4579-1, 4660			



Manufacturer Function	Tool Name	Page-Col.	Manufacturer Function	Tool Name	Page-Col.
Valid Logic Systems Inc. (Cont'd)			Zycad		
Post IC Layout Switch Level Timing Anal	TIMEMILL	4615-2, 4660	Fault Simulation Accelerator	Fault Evaluator	4591-3
Programmable Device Development System	ValidPLD	4560-2, 4660	Logic Simulation Accelerator	Expediter	4586-3
Schematic Capture	ValidGED	4466-2, 4660		Logic Evaluator	4587-1
Standard Cell Layout Tool	ValidBLOCKS	4547-3, 4660		Magnum	4587-2
Thermal & Reliability Analysis	Thermal & Reliability Analysis	4619-3, 4660		System Development Engine	4587-3
Workstation	Analog Design System	4445-3, 4660			
	Board Design System	4445-4, 4660			
	Design Entry System	4446-1, 4660			
	Design Validation System	4446-2, 4660			
	IC Design System	4446-3, 4660			
	Logic Design System	4447-1, 4660			
	Mask Design System	4447-2, 4660			
	Silicon Design System	4447-3, 4660			
Vamp			ZyMOS		
Circuit Board Layout Tool	Autorouter	4533-3	Logic Simulator	ZyPSIM-AT	4505-1
	CPlace	4533-4	Workstation	ZyP-AT	4451-3
	PCB Design	4534-1			
Circuit Simulator	Analogsim	4481-3			
Logic Simulator	Logicsim	4503-4			
Workstation	EOS-1	4447-4			
	Idea Station	4448-1			
Vectron Graphics					
Circuit Board Layout Tool	PCB Design	4534-2			
Workstation	Distributed Design Station	4448-2			
	Personal Design Station	4448-3			
	Stand Alone Design Station	4449-1			
VIA Systems					
Full Custom Layout Tool	ChipTool	4554-2			
Full Custom PG Fracturing	PG-Tool	4607-1			
Schematic Capture	CircuitTool	4466-3			
Standard Cell Layout Tool	BuildingBLOCKS	4547-4			
Workstation	BuildingBLOCKS	4449-2			
Viewlogic Systems					
Circuit Simulator	PSPICE	4481-4			
Fault Simulator	PFG	4517-3			
Logic Simulator	ViewSim	4504-1			
Workstation	Workview 1.2	4449-3			
Visionics					
Workstation	EE Designer	4449-4			
VLSI Technology					
Circuit Simulator	VTIspace	4482-1, 4665			
Full Custom Layout Tool	VTIcustom	4554-3, 4665			
IC Layout Verification	VTIverify	4573-4, 4665			
Logic Simulator	VTIsim	4504-2, 4665			
Schematic Capture	VTIschematic	4467-1, 4665			
Silicon Compiler	VTIcellLib	4565-1, 4665			
Standard Cell Layout Tool	VTIlogicComp	4548-1, 4665			
Workstation	VTITools	4450-1, 4665			
Wintek					
Circuit Board Layout Tool	smARTWORK	4534-3, 4674			
Schematic Capture	HiWIRE	4467-2, 4674			
Workstation	Electronic CAD Software Tools	4450-2, 4674			
XCAT					
Fault Simulation Accelerator	MX/MXT Fault/Logic Accelerator	4591-2			
Logic Simulation Accelerator	HSE Hierarchical Accelerator	4585-4			
	MX Logic/Fault Accelerator	4586-1			
	MXT Logic/Fault/Timing Accel.	4586-2			
Workstation	MX/MXT/HSE Logic/Fault Accel.	4450-3			
Xerox					
Circuit Board Layout Tool	Expert PCB	4535-1			
Logic Simulator	Expert Logic Simulator	4504-3			
Schematic Capture	Expert Schematics	4467-3			
Workstation	Expert	4451-1			
Zuken					
Workstation	C2000	4451-2			



## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names			
Source	Aida	Aldec	Analog Design Tools
Workstation	Aida Design System	SLAV/HASS	Analog Workbench
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, SUN	IBM PC/XT/AT	APOLLO, HEWLETT-PACKARD, IBM PC/XT/AT, SUN
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	Aida Schematic Design Editor  Aida Logic Simulator Aida Timing Verifier Aida Fault Simulator & Fault Inferencer	SLAV  SLAV  SLAV/HASS	Circuit Editor SPICE Plus
Physical layout Circuit board Gate array Standard cell Full custom			
Programmable logic device devel.		SLAV	
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system	Aida CoSimulator& PerSimulator Processor Aida CoSimulator& PerSimulator Processor	SLAV	
Support Documentation software Mechanical CAD/CAM	Included		
Description	The Aida Design System is a high performance CAE workstation capable of simulating up to 1 million gates at 5 million evaluations per second. The system is for designers of medium to large complex digital systems. The AIDA tools include: 1. DESIGN CREATION- Schematic Editor- for interactive development of logic diagrams and corresponding design file. Automatic Logic Documentor- for generating design documentation using printers or plotters. 2. DESIGN VERIFICATION- Logic Design Rules Checker- rules based design verification program. Logic Simulator- performs both event driven and LCC (Levelized Compiled Code) simulation. CoSimulator Accelerator- special purpose reduced instruction set computer speeds up execution of logic and fault simulators. Timing Verifier- examines all paths in a design, compares delays with user defined minimums and maximums. 3. TEST ANALYSIS AND GENERATION- Fault Simulator- evaluates the effectiveness of test vectors as a test for logic designs. ATPG- produces test patterns with 100% coverage for detectable faults in scannable designs. Fault Inferencer- evaluates the effectiveness of test vectors for scan logic designs.	All software modules may be run on any IBM PC compatible.	The Analog Workbench includes schematic entry, editing, SPICE PLUS circuit analysis, instrument display, parameter entry, subcircuits and a sample device library. Optional add-on modules include: General Device Library with parameters for over 900 semiconductor devices and Basic Device Library with parameters for over 50 devices' Parametric Plotting for x-y graphing of circuit or component performance; Statistical Analysis with Monte Carlo and Sensitivity/Worst Case analysis; AnalogLink, for design file transfer; Power Design Module including non-linear model of transformer core magnetics, libraries of magnetic core materials and semiconductor power devices, and Smoke Alarm for safe operating conditions analysis. An interface for converting Mentor's schematic circuit database to Analog Design Tools' circuit design file and vice versa is available on the Apollo platform only.



**DESIGN AUTOMATION—Workstations****Software/Hardware Tool Name****Workstation Design Tool Names (Cont'd)**

Analog Design Tools PC Workbench	Applicon Bravo3	Applicon Electronic Design Station	Aptos Systems ICD-One
IBM PC/XT/AT	DEC VAX, DEC MICROVAX	DEC VAX, DEC MICROVAX, SUN	AT&T, HEWLETT-PACKARD, IBM PC/XT/AT, Compaq 386
PC Workbench Circuit Editor SPICE Plus	Design Capture SPICE CADAT (see HHB Systems) CADAT (see HHB Systems) CADAT (see HHB Systems)	Design Capture CADAT (see HHB Systems) CADAT (see HHB Systems) CADAT (see HHB Systems)	
	Interactive and Automatic Layout  VLSI Design Editor	Interactive and Automatic Layout  VLSI Design Editor	
	DRACULA(see ECAD)/DVS(see Silvar-Lisco)	DRACULA(see ECAD)/DVS(see Silvar-Lisco)	
	CATS (see HHB Systems)	CATS (HHB Systems)  CATS (HHB Systems)	
	Tech Doc Mechanical Design Station	Tech Doc Mechanical Design Station	
The PC Workbench is a low-cost stand-alone workstation that provides the same extensive device library, intuitive user interface, and sophisticated analyses found on the Analog Workbench. Included is schematic entry, editing, SPICE PLUS circuit analysis, instrument display, parameter entry, subcircuits and a sample device library. Optional add-on modules include: General Device Library with parameters for over 50 devices; Parametric Plotting for x-y graphing of circuit or component performance; Statistical Analysis with Monte Carlo and Sensitivity/Worst Case analysis; AnalogLink, for design file transfer; Power Design Module including nonlinear model of transformer core magnetics, libraries of magnetic core materials and semiconductor power devices, and Smoke Alarm for safe operating condition analysis. The PC Workbench is configured as an upgrade kit to the IBM PC/AT which contains software, an accelerator board and an optical mouse.	Bravo3 software is claimed to be the first to offer electronic computer-aided engineering that is integrated with mechanical analysis capabilities. With Bravo3, the verified models created in both mechanical and electronic applications are fully compatible. This makes it possible for mechanical analysis to be performed on electronic components without re-entering data.  Electronic applications for printed circuit board engineering include schematic capture, logic and timing analysis, interactive and automatic layout, photoplotter and NC drill output. For VLSI integrated circuit work, design editor, logic and timing analysis, design/electrical rules checker, optical pattern generator formatter, logic vs. layout consistency checker, layout parameter extraction and network consistency checker capabilities are included.		Aptos Systems and offers an IBM-PC/AT and 80386 based software system for designing integrated circuits. Called ICD-one, this system offers complete two-way communications with systems utilizing GDS-II, Calma's standard IC design communication format. ICD-One is designed to provide existing big-system installations with an inexpensive additional capability for IC design. Its PC to GDS-II communication capability is said to be the first available that will allow two-way transfer of both schematics and the actual layout of design cells, including the electrical characteristics of parts.  Design size capacity is the principal difference between this AT-based workstation and a large system. ICD-One will handle 64k by 64k addressable units of design, while some big systems can allow the user to work on as much as two gigabytes squared of design. However, complex integrated circuits are usually modular. When each section of the design is finished on ICD-one, it is transferred back into the large system, where it can then be used to graphically connect the module into the IC. Reconnection is possible because the ICD-One offers the same superfine 1/8 micron physical unit resolution as the large system.

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## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source	Aptos Systems	AT&T	AT&T
Workstation	RGRAPH	AT&T OMNICARDS	AT&T OMNIRROUTE
FOR DETAILED DATA SEE:			
Tool residence	AT&T, HEWLETT-PACKARD, IBM PC/XT/AT, Compaq 386		
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation			
Physical layout Circuit board Gate array Standard cell Full custom			
Programmable logic device devel.			
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system			
Support Documentation software Mechanical CAD/CAM			
Description	RGRAPH is a CAE/CAD personal design system operating on the IBM PC, with 8087/80287 co-processor, which implements high resolution color graphics and powerful functions commonly found only on high-end CAD systems. RGRAPH is designed to operate as an end-to-end design system or as the front-end to batch oriented CAD systems. The graphics database has fifty layers of design. Each layer can be viewed individually or in combination with other layers. Graphics library includes TTL, CMOS, ECL, analog, discrete and surface mount parts. Includes 9-state event-driven RLOG logic simulator. Maximum PCB size is: 1000 parts, 200 nets, 12,000 pins, 50 layers, 64" x 64", 1:1 board size, one mil resolution and 10 hierarchical levels.	The AT&T OMNICARDS system is a high performance workstation for all phases of PC board design: from schematic capture, through packaging, placement, autorouting, editing and final CAD output. Designed for the latest advances in PC board technology, the system handles surface-mount components, high-speed ECL, and fine-line design parameters with ease. The AT&T Omnicards system runs on a UNIX-based 32-bit CPU operating at 1 MIP for quick command execution. Its color monitor provides high-resolution graphics useful in designing the layout for complex boards. An 80 MByte hard disk includes all software as well as room to work (options allow expansion to 460 MBytes for additional workspace). Its 2 MBytes of RAM enable high-speed computations (options allow expansion to 5 MBytes of RAM for even faster response time).	AT&T now offers AT&T OMNIRROUTE automatic printed circuit software for the DSP9000 Compute Server from Apollo Computer Inc. AT&T OMNIRROUTE is a third generation automatic routing package for the routing of printed circuit boards. The DSP9000 Compute Server provides up to 35 MIPS of computational power. Combining these products results in a high performance automatic router node on the DOMAIN system capable of achieving 100% route completion in a matter of minutes or hours.  AT&T OMNIRROUTE may be installed on the DSP9000 Compute Server and connected via the DOMAIN Network. AT&T OMNIRROUTE printed circuit board design software is available on Apollo's complete line of graphics workstations. Schematic capture, packaging, placement, graphics editing is accomplished on AT&T OMNICARDS while circuit files may be transferred to AT&T OMNIRROUTE for extremely fast automatic routing.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Bishop Graphics Pathfinder	Cadnetix CDX-3000/CDX-3150	Cadnetix CDX-50000	Cadnetix CDX-50000S
IBM PC/XT/AT	AT&T, HEWLETT-PACKARD, IBM PC/XT/AT, Compaq 386	Cadnetix MC68010-based workstation	Cadnetix MC68010-based workstation
Pathfinder, ASCII or IGES based file Scheduled 1st qtr '88	CDX-3000; CDX-3150 Access thru Virtual Logic Analyzer (VLA) Access to worst case timing thru VLA	Hierarchical Schematic Editor	Hierarchical Schematic Editor
Pathfinder & IGES based files		Route Editor	Route Editor
	Access thru VLA Access thru VLA Access thru concurrent fault simulator	CDX-770 Accelerated Digital Design Env.	CDX-770 Accel'td Digital Design Environ.
Documentation & on-line help Telephone Support		2D Drafting Editor Interfaces	2D Drafting Editor Interfaces
A powerful CAE/CAD software package for PCB design and layout (end-to-end solution) including schematic capture and an optional autorouter with mainframe performance (32-bit) featuring unlimited layers, top/bottom views for SMT, Gerber output, fineline routing, mirroring, sophisticated routing algorithms for less than \$5,000.	The CDX-3000 provides schematic capture on standard PC hardware. The CDX-3150 transforms the PC into a full-functioned CAE workstation which embraces Cadnetix' Virtual Logic Analyzer as the "window to the network". Created for the system designer, the CDX-3000/3150 software packages incorporate Cadnetix' user-interface, which is based on the manipulation of objects that represent intuitively recognizable operations within the schematic capture and CAE editors.  Because of the limitations of disk space and memory, only the smallest of designs can be compiled or simulated on a PC. The PC cannot compile or simulate designs of even moderate size without substantial add-in hardware driving up the cost of the PC. Cadnetix overcomes these limitations with its integrated network strategy, offering remote compilation and simulation resources accessible to the PC across the Ethernet network. The sharing of high performance resources minimizes the cost of automated engineering tools while maximizing the performance.	The CDX-50000 is a high performance color PCB layout workstation. Based on the MC68010 running UNIX, the CDX-50000 includes 3.5 MB of RAM, 80 MB Winchester disk and a 1 MB floppy. Ethernet provides access to other workstations, engines and servers. Display resolution is 1024 x 800 pixels. A graphics engine provides 400K vectors clip/transforms per second, clipped and transformed. All Cadnetix workstations use an intuitive object driven interface for ease of use. PCB design capabilities include doubled sided surface mount, analog and ECL. Placement tools include automatic pin and gate swapping and dynamic rat's nest display. Routing Editor allows both interactive and automatic routing on as many as 24 trace layers. Any-angle traces, curved traces and polygon fill capabilities are included. A full range of outputs for test and manufacturing are available.	The CDX-50000S is a high performance color PCB layout workstation. Based on the MC68020 running UNIX, the CDX-50000S includes 4 MB of RAM, 80 MB Winchester disk and a 1 MB floppy. Ethernet provides access to other workstations, engines and servers. Display resolution is 1024 x 800 pixels. A graphics engine provides 400K vectors per second, clipped and transformed. All Cadnetix workstations use an intuitive object driven interface for ease of use. PCB design capabilities include double sided, surface mount, analog and ECL. Placement tools include automatic pin and gate swapping and dynamic rat's nest display. The Route Editor allows both interactive and automatic routing on as many as 24 trace layers. Any-angle traces, curved traces and polygon fill capabilities are included. A hierarchical editor and 2-D drafting editor are included. A full range of outputs for test and manufacturing are available.

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## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation	Cadnetix CDX-5000A	Cadnetix CDX-59000S	Cadnetix CDX-5900S
FOR DETAILED DATA SEE:			
Tool residence	Cadnetix MC68010-based workstation	Cadnetix MC68020-based workstation	Cadnetix MC68020-based workstation
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	Hierarchical Schematic Editor	Hierarchical Schematic Editor SPICE Netlist Cadnetix Digital Design Environment Cadnetix Digital Design Environment Cadnetix Digital Design Environment	Schematic Editor  Cadnetix Digital Design Environment Cadnetix Digital Design Environment Cadnetix Digital Design Environment
Physical layout Circuit board Gate array Standard cell Full custom	Route Editor	Route Editor	Route Editor
Programmable logic device devel.			
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system			CDX-7900S/79000S  CDX-77000S/79000S
Support Documentation software Mechanical CAD/CAM	2D Drafting Editor Interfaces	2D Drafting Editor Interfaces	2D Drafting Editor Interfaces
Description	The CDX-5000A is a color PCB layout workstation. Based on theMC68010 running UNIX, the CDX-5000A includes 3.5 MB of RAM, 80 MB Winchester disk and a 1 MB floppy. Ethernet provides access to other workstations, engines and servers. Display resolution is 1024 x 800 pixels. All Cadnetix workstations use an intuitive object driven interface for ease of use. PCB design capabilities include double sided, surface mount, analog and ECL. Placement tools include automatic pin and gate swapping and dynamic rat's nest display. The Route Editor allows both interactive and automatic routing on up to 24 trace layers. Any-angle traces, curved traces and polygon fill capabilities are included. A 2-D drafting editor is included. A full range of outputs for test and manufacturing is available.	The CDX-59000S is an integrated CAE and CAD workstation. Based on the MC68020 running UNIX, the CDX-59000S includes 4 MB of RAM, 40 MB Winchester disk and a 1 MB floppy. Ethernet provides access to other workstations, engines and servers. Color display resolution is 1024 x 800 pixels. A graphics engine provides 400K vectors per second, clipped and transformed. All Cadnetix workstations use an intuitive object driven interface for ease of use. A graphical Virtual Logic Analyzer allows the user to create input waveforms and view simulation results. Logic simulation is based on a 21-state simulator and includes good-circuit and worst-case capabilities. Automatic placement and routing software is included for PCB design. PCB design capabilities include double side surface mount, analog and ECL. The Route Editor allows both interactive and automatic routing on as many as 24 trace layers. Any-angle traces, curved traces and polygon fill capabilities are included. A hierarchical editor and 2-D drafting editor are included. A full range of outputs for test and manufacturing is available.	The CDX-5900S CAE and CAD workstation includes UNIX & post-processing package, 100% rip up and re-route with CDX-75000 Route Engine. Based on the MC68020, it includes a 1024 x 800 pixel color monitor, 2.5 MB RAM, 40 MB disk, and a 1 MB floppy. Ethernet provides access to other workstations, engines and servers. All Cadnetix workstations use an intuitive object driven interface for ease of use. A graphical Virtual Logic Analyzer allows the user to create input waveforms and view simulation results. Logic simulation is based on a 21-state simulator and includes good-circuit and worst-case capabilities. Automatic placement and routing software is included for PCB design. PCB design capabilities include double sided, surface mount, analog and ECL. The Route Editor allows both interactive and automatic routing on as many as 24 trace layers. Any-angle traces, curved traces and polygon fill capabilities are included. A hierarchical editor and 2-D drafting editor are included. A full range of outputs for test and manufacturing is available.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Cadnetix CDX-70000	Cadnetix CDX-9300	Caeco VLSI Desygner III	Caeco VLSI Desygner IV
Cadnetix proprietary hardware	Cadnetix MC68020-based workstation	SUN	SUN
Cadnetix Analog Design Environment Cadnetix Digital Design Environment Cadnetix Digital Design Environment	Hierarchical Schematic Capture SPICE netlist Cadnetix Digital Design Environment Cadnetix Digital Design Environment Cadnetix Concurrent Fault Simulator	CAEPAC II SPICE/HSPICE (see Meta-Software) SILOS (see Simucad) SILOS (see Simucad)	Caepac II SPICE/HSPICE (see Meta-Software) SILOS (see Simucad) SILOS (see Simucad)
		CAEPAC I/III	
		DRACULA III (see ECAD)	DRACULA III (see ECAD)
Physical Modeling Package Accelerated Digital Design Environment	CDX-70000 Configurable Analysis Engine CDX-70000 Configurable Analysis Engine		
The Configurable Analysis Engine can be tailored to meet the specific needs of diverse engineering organizations. It is a network processing node that features multiple applications including accelerated compilation and simulation for both digital and analog design, physical modeling, and mass storage for database management. The Configurable Analysis Engine is designed to serve a network of standard PC-ATs or 100%-compatibles with no additional hardware.	The Cadnetix Color CAE Design and Analysis Workstation is based on the MC68020 microprocessor with 1024 x 800 pixel color monitor, 2.5 MB RAM, 40 MB disk, and a 1 MB floppy. It includes UNIX and a post processing package.	Sun 2/120.	Sun 2/50.
The basic configuration contains the MC68020 microprocessor, an Ethernet Interface, 4 MB of RAM, 80 MB of mass storage, schematic compilation software, and either nonaccelerated digital simulation or accelerated analog simulation. Hardware options to the basic system include the RISC Engine, a bit-slice processor, a physical modeler, and a hard disk. Software options to the basic system include accelerated compilation, accelerated digital simulation, accelerated analog simulation, and database management tools.			

# IC MASTER

DESIGN AUTOMATION—Workstations			
Generic Function	Software/ Hardware Tool Name		
Workstation Design Tool Names (Cont'd)			
Source	Caeco	Calay Systems	Calay Systems
Workstation	VLSI Desygner V	Design Automation Series	ZX1000
FOR DETAILED DATA SEE:			
Tool residence	SUN	DEC LSI-11	IBM PC/XT/AT
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	CAEPAC II SPICE/HSPICE (see Meta-Software) SILOS (see Simucad) SILOS (see Simucad)	ZX1000	ZX1000 Interface to CADAT (see HHB Systems)
Physical layout Circuit board Gate array Standard cell Full custom	CAEPAC I/III	DA Series	
Programmable logic device devel.			
Silicon compilation			
IC layout verification	DRACULA III (see ECAD)		
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system			Interface to CATS (see HHB Systems)
Support Documentation software Mechanical CAD/CAM		MGIOS	
Description	Sun 3/160.	The Calay DA Series of workstations for PCB design are full capability and high performance systems. Running on a standard hardware platform with proprietary hardware accelerators, they provide fast, efficient PCB Layout design and routing capability. The systems' features include hardware autorouters, which can achieve a 100 percent routing solution, component placement tools, specially designed software to handle Surface Mounted Devices, on-line design rule check, parts library, automatic design optimization for enhanced manufacturability, and interactive editing with high resolution color graphics, and hardware pan and zoom. Also offered in the systems is complete output documentation and postprocessing capabilities for manufacturing. Th DA series handles large, complex, dense, multi-layer board designs that can include a mix of surface mount and through-hole mounted components, and analog, digital, and ECL circuitry.	Calay's ZX1000 is a schematic editor that runs on IBM PC/AT compatibles and provides capabilities for engineering functions related to physical design including estimates for electrical power, part cost, and board component area. The ZX1000 features a large component library of more than 5000 components, support for both hierarchical and flat designs, fast interactive editing tools, electrical error checking, and command macro functions. Users can graphically enter designs and perform the functions of design capture as well as interface to simulation and printed circuit board design tools used to develop and create electronic circuits. The ZX1000 schematic capture system interfaces directly with Calay's Design Automation Series PCB CAD workstations and offers full forward and backward annotation capability.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Calma GDSII/32	Calma Logic Examiner	Calma Logic Explorer	Calma Logic Scribe
DATA GENERAL	APOLLO	APOLLO	APOLLO
CARDS II			
CARDS II, Techplus GDS II Custom Plus			
Vecheck Fast Mask Engine			
2D drafting on CARDS II			
Custom Plus is Calma's full custom symbolic layout package. Techplus provides thick and thin film hybrid design, microwave, flex cable, others. Fast Mask Engine is Calma's hardware accelerator for performing DRC's. Vecheck is Calma's OEM version of ECAD's Dracula II.	The Calma Logic Examiner is a design automation tool developed specifically for the test engineer. The Logic Examiner provides the link between electronic circuit design and test program development. With the Logic Examiner, the test engineers use the same database as the design engineers who developed integrated circuit and printed circuit designs on the Logic Scribe and Logic Explorer. The Logic Examiner provides a design manager that manages the project throughout the design process and provides a consistent user interface; computer aided schematic capture; fault generation for fast generation of faults throughout the network; automatic test pattern generator; fault simulator to measure the fault coverage of the test patterns; tester interface programs to format test vectors for production testers; and an interface for the IMS Logic Master, a low-cost hardware tester for accurate prototype verification. The Logic Examiner is available on Apollo workstations including the DN570A and the Domain Series 3000.	The Calma Logic Explorer is an analysis and verification system for the design of integrated circuits and printed circuit boards. The Logic Explorer provides a design manager that manages the project throughout the design process and provides a consistent user interface; computer-aided schematic capture; mixed-level logic simulator which includes behavioral, gate and transistor level simulation; waveform analysis to view simulation results; timing verifier to identify timing violations independently of functional simulation; and testability analysis to determine early in the design cycle whether a design is testable. Also available is the HSPICE analog simulator from Meta Software. The Logic Explorer is available of Apollo workstations including the DN570A and the Domain 3000.	The Calma Logic Scribe is a low-cost, front-end schematic capture and design system for the design of integrated circuits and printed circuit boards. Included in the Logic Scribe is a design manager which provides a constant user interface and manages the system throughout the design process; computer-aided schematic capture which automatically generates the database that interfaces to Calma or third party CAE or CAD products; remote simulation capability and waveform analysis to view the results of logic simulation. The Logic Scribe is offered on the Apollo Domain 3000 or as a software package to execute on other Apollo hardware.

# IC MASTER

DESIGN AUTOMATION—Workstations			
Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation FOR DETAILED DATA SEE:	Calma Tegastation	Calos CALOS 6000	Calos EWS 6000
Tool residence	APOLLO	IBM PC/XT/AT, Compaq, TI Business-Pro, Televideo 286	Calos MC68000 workstation
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	TEGATE HSPICE (see Meta-Software) TEXSIM-B TSCAN TCAT	Calos 6000  (see Design Tool Interfaces)	EWS 6000  (see Design Tool Interfaces)
Physical layout Circuit board Gate array Standard cell Full custom	TBOARDS TARRAYS Cell Plus Link to GDS II	(see Design Tool Interfaces)	(see Design Tool Interfaces)
Programmable logic device devel.			
Silicon compilation			
IC layout verification	VECHECK		
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system	(see Design Tool Interfaces) (see Design Tool Interfaces) CATSCOPE		
Support Documentation software Mechanical CAD/CAM	DDM, Geomod	Pen Plotters (HP 7580, HI DMP51, Calcomp	
Description	Link available between TBoards and DDM 3-D mechanical software.	The CALOS 6000 is an electronic engineering workstation that features schematic capture, simulation, and interface capability. Its compact data base handles multipage schematics as a single database. The database is conductive and offers real time error checking. CALOS has a library system that effectively handles board and system level schematics. Other features include high resolution interactive color graphics, complete forward and backward annotation, and IBM PC XT/AT hardware configuration.	Database compatible with CALOS 6000.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Case Technology CT10000	Case Technology CT2000	Case Technology CT4000	Case Technology Vanguard
DEC VAX	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, NEC PC, SUN	DEC MICROVAX	DEC MICROVAX
CT2000 PSPICE (Meta-Software) SILOS/CADAT (Simucad/HHB Systems) CT2600 CADAT (HHB Systems)	CT2000 PSPICE (Meta-Software) SILOS/CADAT (Simucad/HHB Systems) CT2600 CADAT (HHB Systems)	CT2000 PSPICE (Meta-Software) SILOS/CADAT (Simucad/HHB Systems) CT2600 CADAT (HHB Systems)	CT2000 PSPICE (Meta-Software) SILOS/CADAT (Simucad/HHB Systems) CT2600 CADAT (HHB Systems)
CT2400 Layout System	CT2400 Layout System	CT2400 Layout System	CT2400 Layout System
CUPL (P-CAD)	CUPL (P-CAD)	CUPL (P-CAD)	CUPL (P-CAD)
CATS DHM (HHB Systems) CATS Accelerator (HHB Systems) CATS Accelerator (HHB Systems)	CATS DHM (HHB Systems) CATS Accelerator (HHB Systems) CATS Accelerator (HHB Systems)	CATS DHM (HHB Systems) CATS Accelerator (HHB Systems) CATS Accelerator (HHB Systems)	CATS DHM (HHB Systems) CATS Accelerator (HHB Systems) CATS Accelerator (HHB Systems)
Case Technology has implemented its popular CAE schematic design software on the DEC VAX mini-computer under the VMS operating system.	All software tools may be run on IBM-PC series and compatibles, VAX 730, 780, 8600, MicroVAX, Rainbow. Supports major standard cell & gate array manufacturers as well as auto layout systems.	Case Technology's CAE software now runs on the DEC MicroVAX/VSI (VAXstation II) computer. The package includes a schematic design system, logic and circuit simulation and timing verification. The CT-4000 system incorporates all the features and user interfaces of the CT-2000 personal computer based version into a MicroVAX workstation implementation.	To support the new color capabilities of DEC's VAX Station II/GPX, Case Technology has introduced a version of its Vanguard CAE/CAD system for this workstation. The Vanguard system includes schematic and PCB layout editors, logic and fault simulation, timing verification, and a variety of other design tools.

## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation FOR DETAILED DATA SEE:	Case Technology Vanguard Stellar System	Clarity Systems SuperSet 5000	Compact Software Microwave Harmonica
Tool residence	AT&T, CONTROL DATA, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, NEC PC, SUN	APOLLO	APOLLO, CRAY, DEC VAX, DEC MICROVAX, SUN
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	PSPICE CADAT, SILOS Case CADAT	StrucSet, Design Capture & Symbol Editor S-SPICE based on Berkely Spice MIXIM, mixed-mode multi-level simulator	
Physical layout Circuit board Gate array Standard cell Full custom		Symbolic Layout & Compaction & Geometric	
Programmable logic device devel.	CUPL	Automatic PLA Layout Generator	
Silicon compilation			
IC layout verification		DRC, Logic vs. Layout, Parameter Extract	
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system	CATS Dynamic Hardware Modeler (see HHB)		
Support Documentation software Mechanical CAD/CAM	Interleaf, Ventura, Case		
Description	System consists of a flexible graphics editor, powerful symbol editor and 3000 library parts. Analog and digital, compiler, user definable parts list, netlister. All output files are in ASCII format and are fully documented. ERC postprocessor, support for pen plotters, laser printers, back annotation utility all standard. PCB layout, logic and circuit simulators, timing verifier, PLD compiler, document editor.	SuperSet 5000 is a CIE system for custom VLSI design. Superset is designed to provide a complete solution from conceptual design to final chip layout. The infrastructure module, BaseSet, comprised of a single database and a single human interface, provides a consistent integrated environment for all of SuperSet's application modules.  StrucSet is an integrated set of tools used for structural and schematic design of hierarchical blocks at the architectural, functional, logic, gate, and transistor levels. SimuSet is an integrated set of tools used for digital and analog performance evaluation and validation of logical, topological and geometric designs created with the SuperSet modules. TopSet is an integrated set of tools used for topological or symbolic layout design. GeoSet is an integrated set of tools used for the geometric layout design and verification of dense leaf cells. Verification utilities include design rule checking, parameter extraction and a logic vs. layout comparison. GluSet is an integrated tool used to generate layouts of random or "glue" logic blocks. PlaSet is an integrated set of tools used to automatically generate physical layout of PLA blocks.	Microwave Harmonica is a program for mainframe computers that can very quickly and accurately analyze and optimize non-linear circuits from the MHz region well into the microwave region. Based upon the technique of Harmonic-balance Simulation, the software can provide solutions to very large and previously impractical applications.  A Sophisticated user-friendly data input module simplifies the task of defining the circuit. A library of both linear and non-linear devices is provided, as well as the ability to enter any kind of measured linear components or user-defined model. For optimizations, any physical or electrical parameter of the linear sub-network may be selected as a design variable. In addition, a menu of network functions to be optimized, such as output power or DC-to-RF efficiency, is provided. Once the user selects the function to be optimized, the program automatically computes the function and optimizes the circuit design without requiring any special intervention by the user. The overall result is that the time required to take a design from concept to market is greatly reduced and the task of determining how to achieve specific design goals is simplified. This can give the user a competitive edge in the rapidly changing microwave marketplace.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Compact Software Super-Compact	Computervision CADDStation	Computervision CDS4000	Computervision Designer V-X
APOLLO, DEC VAX, DEC MICROVAX, HEW-LETT-PACKARD, IBM MAINFRAME/MINI, IBM PC/XT/AT, RIDGE, SUN	Computervision	Proprietary	Proprietary
	Schematic Design		
	AUTOBOARD	CADDS 4X CADDS 2/VLSI	CADDS 4X CADDS 2/VLSI
<p>SUPER-COMPACT provides the necessary tools for choosing a design topology and active elements, synthesizing amplifier matching circuits, and optimizing complete circuits having as many as four external ports. Circuit elements include lumped, microstrip and stripline, filter, thin film, coupler and active devices. The circuit analysis portion of SUPER-COMPACT features tabular and interactive CRT graphics.</p> <p>Mapping and variable element analysis are also featured. Optimization features random and/or gradient methods, with performance criteria that can include combinations of parameters with noise, phase, and group delay characteristics. Circuits can be modified without exit from the program. Transistors and dielectric data banks provide for selection on a conversational basis. A Monte-Carlo analysis feature can be used with its companion program, AUTOART, to generate masks for Microwave Integrated Circuits.</p>	<p>CADDStation is Computervision's high-performance workstation. Based upon 32-bit, 68020 technology, the CADDStation uses the UNIX 4.2 bsd operating system. It has multi-windowing/multi-tasking capability; and, in conjunction with Sun's Network File System and the industry-standard TCP/IP, and Ethernet protocols, can be configured in distributed processing networks. CADDStation is easily linked in networks with Computervision's CDS 4000 and Designer V-X systems, as well as with VAX's, IBM-PCs, and IBM mainframes supporting the VM operating system.</p> <p>CADDStation uses Computervision-developed software for the engineering and design of printed circuit boards. Schematic Design software provides schematic capture with tight interfaces to HILO-3 and SPICE for digital and analog simulation. Accepting input from Schematic Designer, Auto-board is Computervision's tool for PCB design on CADDStation. Among Auto-board's notable features are: interactive and automatic placement and routing; support for surface mount devices; support for high-density digital and analog designs; and, a repositioning algorithm-based router for high completion rates and minimum trace length. ECAM capabilities include output to photoplotters, NC drill and insertion machines and to automatic test equipment.</p>		

## DESIGN AUTOMATION—Workstations

Generic Function		Software/ Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation FOR DETAILED DATA SEE:	Computervision Designer V-X Series M	Computervision Personal Engineer	Control Data CYBERNET®EXPRESS
Tool residence	Proprietary	IBM PC/XT/AT	
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation		SCHEDIT	
Physical layout Circuit board Gate array Standard cell Full custom	CADDS 4X  CADDS 2/VLSI	(netlist generator)	
Programmable logic device devel.			
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system			
Support Documentation software Mechanical CAD/CAM		MSDOS Utilities	
Description		<p>Personal Engineer provides schematic capture tools in the IBM-PC/PC-DOS environment. An integral part of Computervision's electronic engineering/design product line, graphics and databases from the Personal Engineer are fully compatible with Computervision's workstation-based schematic capture, simulation, and PCB design software.</p> <p>Personal Engineer provides high-level symbols for capturing your ideas in graphics form. Primitives are available for constructing your own symbols. The schematic editor supports hierachical design--top/down, or bottom/up. Rubberbanding for fast wiring, and split screen viewing for wiring over large areas are two convenient editing features. Tight integration with Computervision's workstation-based Logic Design software allows for circuit simulationand logic verification on CADDStation. Results are displayed on Personal Engineer's wave-form grapher.</p>	<p>With the addition of Vectron Graphic System's automatic printed circuit board layout system, Control Data has further enhanced its advanced electronics workstation offering. Called the CYBER-NET®EXPRESS Electronic Designer, the IBM-PC XT or AT based workstation includes schematic entry, behavioral simulation, digital and analog simulation, "logic analyzer" type output display, reliability (MTBF) analysis, and PCB layout. The Vectron layout system operates on a back-end host machine, either a CYBER 205 supercomputer in Control Data's worldwide supercomputer network or on a user's in-house CDC or VAX system.</p>



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Control Data Electronics Designer	Control Data MIDAS	Daisy Systems LOGICIAN 386	Daisy Systems Personal LOGICIAN 286
IBM PC/XT/AT	APOLLO, CONTROL DATA, Orcatech, Daisy	Daisy 80386	IBM PC/XT/AT
Graphic Editor ASPEC, OPTMOS SALT (see The CAD Group) ED-TV (see Design Tool Interfaces)	Mentor, Tek CAE, Daisy, CDC Symbols Local and host based (CDC Cyber) Host based (CDC Cyber) Host based (CDC Cyber)	ACE/ ACE-PI SPICE Daisy Logic Simulator Daisy Timing Verifier MegaFAULT	ACE/ ACE-PI DSPIICE Daisy Logic Simulator Daisy Timing Verifier
PEPPER	Interactive layout. Apollo, Orcatech	BOARDMASTER Personal GATEMASTER & MegaGATEMASTER CELLMASTER CHIPMASTER	Personal BOARDMASTER Personal GATEMASTER Personal CELLMASTER Personal CHIPMASTER
CUPL (P-CAD)		PLDMASTER	PLD Master
(see Design Tool Interfaces)		MAX-IRC	MAX- IRC
		Physical Modeling Extension MegaLOGICIAN MegaFAULT	Physical Modeling Extension
Word Processing Structures, Piping, Power codes avail.		DocuMaker MDP- Mechanical Documentation Program	DocuMaker MDP- Mechanical Documentation Program
<p>The Electronics Designer workstation is claimed to be one of the most complete electronic design systems on the market today. The workstation includes seven different analysis applications and three graphics systems. Also included is an ever expanding 2500 component library that meets EIA and MIL SPEC 1000 standards. The analysis tools include the ASPEC circuit simulator, the OPTIMOS optimizing MOS model generator, the SALT logic simulator, the VERILOG behavioral simulator, the PREDICTOR reliability prediction system, the PEPPER PCB route and place system, and ED-TV a SCALD timing verifier. Graphics applications include the EDSCHEMATICS schematic editor, ED-LAYOUT PCB layout editor, and OCEANVIEW an advanced logic waveform display system.</p> <p>The Electronics Designer includes more than 25 simulation interfaces and has something no other system has- the ability to exchange drawings (not just netlists) with PRIME, Computervision, and Mentor systems.</p>		<p>The LOGICIAN 386 is a high-end 32-bit workstation optimized for layout applications. The LOGICIAN 386 is based on the Intel 80386 CPU and comes standard with a high-performance graphics accelerator and 19-inch monitor. This system is expandable and upgradeable to handle the memory and disk capacity demands of large PCB or IC designs.</p> <p>The Logician 386 can be equipped with any of Daisy's proven CAE/ CAD application packages from schematic capture and digital/ analog simulation, to custom IC, cell-based, ASIC or board layout.</p>	<p>The Personal LOGICIAN 286 is based on the IBM PC AT with the 80286 CPU and Enhanced Graphics Adapter (EGA) graphics. The system supports the complete Daisy product line of design automation tools including schematic entry, digital and analog simulation, test and layout.</p> <p>This workstation is fully integrated into Daisy's engineering environment, with access to hardware acceleration and physical modeling. The Personal LOGICIAN 286 is capable of running a multitude of applications that require MSDOS as well as enhanced graphics.</p>

## DESIGN AUTOMATION—Workstations

Generic Function		Software / Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation FOR DETAILED DATA SEE:	Daisy Systems Personal LOGICIAN 386	Daisy Systems VX Node	Dasoft Design Systems Dasoft-16
Tool residence	Daisy 80386 PC	DEC MICROVAX	AT&T, IBM PC/XT/AT, NEC PC
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	ACE/ ACE-PI SPICE Daisy Logic Simulator Daisy Timing Verifier	DSPICE	Dasoft 16-S
Physical layout Circuit board Gate array Standard cell Full custom	Personal BOARDMASTER Personal GATEMASTER Personal CELLMASTER Personal CHIPMASTER	STAR- automatic router	Dasoft 16-B
Programmable logic device devel.	PLD Master		
Silicon compilation			
IC layout verification	MAX- IRC	Dracula I or II- layout post processor	
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system	Physical Modeling Extension		
Support Documentation software Mechanical CAD/CAM	DocuMaker MDP- Mechanical Documentation Program		
Description	<p>The Personal LOGICIAN 386 is a high performance personal engineering workstation based on the Intel 80386 CPU and the industry-standard PC AT architecture. This system comes standard with Enhanced Graphics Adapter (EGA) graphics and a 13-inch enhanced color monitor.</p> <p>The Personal LOGICIAN 386 supports all of Daisy's CAE applications including schematic capture, analog and digital simulation, and physical modeling. It also handles graphics-intensive CAD applications such as chip and board layout. The system supports a large base of existing software for the IBM PC AT. It is fully compatible with all Daisy workstations, and has network access to accelerated logic simulation on the MegaLOGICIAN with Daisy's ACCESS software.</p>	<p>Daisy's VX Node is based on the DEC 32-bit MicroVAX II. When combined with Daisy software, flexible communications, and applications packages, the MicroVAX II provides a variety of powerful capabilities for the Daisy CAE environment.</p> <p>The VX Node is fully integrated with Daisy's engineering workstations by the Ethernet-based local area network (DLAN). It can be used both as a multi-user server node, and as a network resource for compute-intensive tasks.</p> <p>Additionally, the VX Node allows the Daisy user to run any of the thousands of third-party VMS-based applications with the network VT100 terminal emulator provided on all Daisy workstations.</p>	Auto-router surface mount technology compatible.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Data General DS/7500 Workstation	Drafting Dynamics Graphic System	Electronic Software Products EDGE	Electronic Software Products ESP
DATA GENERAL	COMPUTER AUTOMATION, MOTOROLA	DEC MICROVAX, IBM MAINFRAME/MINI	IBM PC/XT/AT
TEO/Electronics Design System TEO/Electronics Interactive Simulator TEO/Electronics Interactive Simulator	Automatic Schematic SPICE	GRALE, LOGNET SIMIC, USPICE CADAT (see HHB Systems) CADAT (see HHB Systems)	Lognet PC-USPICE
	PC	EDGE EDGE EDGE	
		UDRC	
TEO/3D			
The DS/7500 series of entry-level workstations are part of a complete family of systems for the engineering, scientific, and technical communities. It combines the power of a dedicated 32-bit processor, and the productivity of a multi-window, multi-tasking environment, with high-performance graphics and intelligent I/O processing. The result is a tightly integrated workstation that can function either as an intelligent dedicated workstation, or as a resource in Data General's distributed-systems environment. The DS/7500 workstation can support up to 256 concurrent processes with four gigabytes of virtual address space and multiple display windows. It offers up to 10 megabytes of main memory.	Porting to IBM PC/AT.	Software sold bundled or unbundled. Available on IBM and other mainframes.	Software available on PC/AT and clones. Uses Mouse Systems mouse.

## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation FOR DETAILED DATA SEE:	ES2/US2 SOLO 1000	ES2/US2 SOLO 1200	EXAR Flexar Layout System page 4222
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, VAXstation 2000	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, VAXstation 2000	APOLLO, IBM PC/XT/AT
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	Proprietary & Daisy/Mentor/Valid/others Proprietary Proprietary, HILO, SILOS, CADAT Proprietary, HILO, SILOS, CADAT Proprietary, HILO, SILOS, CADAT	Proprietary, Daisy/Mentor/Valid & others Proprietary Proprietary, HILO, SILOS, CADAT Proprietary, HILO, SILOS, CADAT Proprietary, HILO, SILOS, CADAT	Case Tech. CT2000/Silvar-Lisco SL2000 PSPICE (see MicroSim)
Physical layout Circuit board Gate array Standard cell Full custom	Physical Design Subsystem Physical Design Subsystem	Physical Design Subsystem Physical Design Subsystem	
Programmable logic device devel.			
Silicon compilation	Proprietary		
IC layout verification	Proprietary		DRC/ERC embedded
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system	Sentry	Sentry	
Support Documentation software Mechanical CAD/CAM	Design Manager	Design Manager	Flexar user manual
Description	<p>The SOLO 1000 is an optimised and integrated semi-custom workstation that brings together high performance hardware and proven cell generation software. It provides an exceptionally powerful chip design tool that is easy to use for engineers involved in systems design at all levels. SOLO 1000 consists of tools for graphical schematic capture, logic and timing simulation, fault analysis, automated layout design, post layout simulation, design management and test vector generation.</p> <p>Starting with the hardware description language or a schematic diagram, the system engineer can take the design right through layout, placement, routing or post-layout simulation. Using SOLO 1000, an engineer, with or without IC design experience, can produce custom optimized designs that are correct by design and guaranteed to work the first time. Different design ideas can be compared and evaluated before the manufacturing process is selected, and the performance of the finished parts can be predicted well in advance of committing to fabrication.</p>	<p>The SOLO 1200 is an optimized and integrated semi-custom workstation that brings together high performance hardware and proven cell generation software. It provides an exceptionally powerful chip design tool that is easy to use for engineers involved in systems design at all levels. SOLO 1200 consists of tools for graphical schematic capture, logic and timing simulation, fault analysis, automated layout design, post layout simulation, design management and test vector generation. In addition to the capabilities of the SOLO 1000, SOLO 1200 adds the ability to integrate user-defined RAM, ROM and PLA blocks.</p> <p>Starting with the hardware description language or a schematic diagram, the system engineer can take the design right through layout, placement, routing and post-layout simulation. Using SOLO 1200, an engineer with or without IC design experience, can produce custom optimized designs that are correct by design and guaranteed to work the first time. Different design ideas can be compared and evaluated before the manufacturing process is selected, and the performance of the finished parts can be predicted well in advance of committing to fabrication.</p>	<p>Flexar Layout System is a dedicated layout tool that enables users to edit and customize metal patterns implementing linear integrated designs onto any of the master chips within the Flexar Beta Series. The system caters for design rules and simple electrical rules checking while the user is on-line editing. The system comes ready with a comprehensive library of pre-designed and characterized soft macro cells which is also available in Kit-Parts to facilitate breadboarding designs. This layout system is part of a more comprehensive totally integrated development system known as FIDS.</p>



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Fairchild FAIRCAD	Ferranti Interdesign Silicon Design System	FutureNet (Data I/O) DASH-Analog Workbench page 4651 IBM PC/XT/AT	FutureNet (Data I/O) Dash-Semicustom Development page 4651 IBM PC/XT/AT
DEC VAX, DEC MICROVAX, TEKTRONIX, Valid, Mentor, Daisy, FutureNet	DEC VAX, DEC MICROVAX		
FAIRCAD FAIRCAD FAIRCAD	ULA LOG CAP ULA SIM and FSPICE ULA SIM ULA SIM	DASH-4 SPICE (see Analog Design Tools)	DASH-4 DASH CADAT-Plus (also see HHB Systems) DASH CADAT-Plus (also see HHB Systems) DASH CADAT-Plus (also see HHB Systems)
FAIRCAD FAIRCAD	ULA LAY CAP and ULASilcom		DASH-PCB
			DASH Semicustom Development System
	ULA SILCOM		DASH-GATES
	ULA CHECK		
			CATS Dynamic Hardware Modeler (see HHB) CATS Accelerator (see HHB Systems) CATS Accelerator (see HHB Systems) CATS Integrated Test System (see HHB)
	Ferranti Test System		
FAIRCAD- Fairchild's fully integrated, technology independent gate array design software- supports all design tasks from design capture through final design database creation for prototype manufacturing. FAIRCAD is available on tape for installation on a VAX VMS system or on MicroVAX II. A proven tool for designing circuitry using CMOS and ECL gate arrays, FAIRCAD combines engineering graphics with powerful programs to compile, analyze, simulate, and place and route a design. FAIRCAD is menu-driven with extensive on-line help listings and a built-in system monitor to ensure the proper program sequence is adhered to.	The Silicon Design System is a complete suite of CAD tools for the design of Ferranti ULA gate arrays. The system is VAX based and supports all aspects of the development cycle including physical layout and timing verification. Silicon compilers are also available for autoroute and generation of an optimized IC. Input to the design system can be either from schematic level or direct from Mentor, Daisy and Valid workstation designs utilizing the ULA libraries.	The DASH-Analog Workbench is a high-performance standalone PC-based workstation that uses the DASH Schematic Designer to capture the analog circuit. Once the circuit has been entered using DASH, the DASH-Analog Workbench performs simulation and analysis of the circuit. The Workbench features simple menus and mouse-oriented operation, and can be used to extract only the analog portions of the circuit for analysis. Modules allow statistical analysis, power-supply design, parametric plotting, and electrical stress analysis. Time domain measurements can be performed using a four-channel function generator, and users can specify such parameters as waveform duration, rise and fall times, dc offset, and amplitude. The system also features a frequency sweeper, a network analyzer, and a spectrum analyzer. Simulation is performed by Berkeley SPICE running on the 32-bit co-processor and using the large General Device Library.	Futurenet's DASH-Semicustom Development System enables engineers to design gate arrays using an IBM AT. The product enables engineers to use any of four design-entry methods for their gate array, then provides critical circuit simulation. The end result is a fully simulated design that is translated into the netlist format of the foundry of the engineer's choice. The Semicustom Development System contains DASH-GATES, a functional entry system that allows engineers to use equations, truth tables, or state diagrams in addition to schematics in order to enter their design. Once the design is captured, the system's library building tools, logic synthesis, and simulation capability provide the engineer with a pathway to a verified, functioning design.  The DASH-Semicustom Development System consists of a number of design and simulation tools: DASH-4 for the schematic design of circuitry such as data paths, and for placement of the macro-cell library elements. DASH-GATES for functionally describing portions of the gate array such as decoders or state machines--using truth tables, state diagrams, or logic equations. DASH-CADAT-Plus for simulation, and for performing analysis and fault grading of the chip design. DASH-Semicustom Design Kits that include: foundry symbol libraries, foundry simulation libraries, foundry netlist translators, "dial-in" worst-case-condition analysis software.

## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source	FutureNet (Data I/O)	Gateway Design Automation	Gerber Scientific Instrument
Workstation	Personal Silicon Foundry	Gateway Design Automation	PC800 Model 4
FOR DETAILED DATA SEE:	page 4651		
Tool residence	IBM PC/XT/AT	APOLLO, CONTROL DATA, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, SUN, Silicon Graphics	HEWLETT-PACKARD, MOTOROLA
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	DASH-4 + ABEL  ABEL ABEL PLD Test	VERILOG, VERILOG-XL VERILOG, VERILOG-XL TESTGRADE, STATGRADE, BITGRADE	(see Design Tool Interfaces)
Physical layout Circuit board Gate array Standard cell Full custom			PC800 Model 4
Programmable logic device devel.	Personal Silicon Foundry		
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system		VERILOG-XL TESTGRADE-A	
Support Documentation software Mechanical CAD/CAM			Component Manager, Plot Verify Drill Tape and Insertion Tape Generators
Description	Personal Silicon Foundry is said to be the first complete programmable logic development system on the market. It provides complete design, programming and testing for virtually every PLD and PROM available. Design description for the PLD can be entered using any combination of schematics, Boolean equations, truth tables, or state diagrams. Once the description is entered, the Personal Silicon Foundry automatically performs logic reduction, simulation, fault analysis, and test vector generation, leaving the designer free to concentrate on the design. Once the files have been tested and verified, a JEDEC-standard load file is sent to a Data I/O programmer where the device is programmed. Finally, the device is tested once again by using testing routines provided to the programmer. Automatic documentation of the entire process is performed throughout the design and testing cycle.		The PC800 produces artwork negatives or positives typically used in the manufacture of printed circuit boards. It can also produce component lists, N/C machine tapes, drill drawings, component layout drawings, and silkscreen mask and solder mask negatives or positives. The PC800 Model 4 is the perfect vehicle for interaction between computer and designer. A unique floating variable grid makes it easy to design SMD boards right on screen. It accepts components of any size and shape, whether metric or English standards. The PC800 Model 4 provides a large and flexible symbol storage library enabling designers to build in any number of SMDs for recall and positioning as needed. It provides forstacking of components to allow for maximum use of space. It delivers new levels of precision for timing and shielding tolerances. With four-decimal place accuracy, the PC800 Model 4 is ideal for spacing between components, traces and registration. It even designs curved traces and teardrop pads. It performs continuity checking prior to creating artwork. Its flexible software allows putting SMDs on both sides of a board. It also performs design rule checking which checks for user-defined mechanical tolerances.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Harris Semiconductor Harris/SDA Workstation page 4246	Hewlett-Packard Electronic Design System	HHB Systems CADAT 6.0	IBM CIEDS Des. Cap./Sim. for RT PC
APOLLO, DEC MICROVAX, MASSCOMP, SUN	HEWLETT-PACKARD, (HP 320 and Vectra PC)	APOLLO, DATA GENERAL, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, IBM MAINFRAME/MINI, IBM PC/XT/AT, MASSCOMP, SUN	IBM MAINFRAME/MINI, IBM RT PC
SDA schematic capture SLICE CADAT (see HHB Systems), SLICE TA CADAT (see HHB Systems), SLICE	Design Capture System Analog Workbench (see Analog Des. Tools) HILO-3 (see Genrad) HILO-3 (see Genrad) HILO-3 (see Genrad)	CADAT 6.0  CADAT 6.0	CIEDS/Design Capture CIEDS/Analog/Digital; CIEDS/Switched Cap CIEDS/Behavioral; CIEDS/Logic Simulator CIEDS/Behavioral Simulator
Standard Edge SDA Layout	Printed Circuit Design System		
OSI Logic Compiler, RAM, ROM compilers			
LVS, DRC			
CADAT PACSIM CADAT Mach 1000 CADAT Mach 1000	HICHIP (see Genrad)  HP Model 840 HP Model 840 81810S	CATS Modeler  CATS Accelerator CATS Accelerator	
Complete system documentation	Documentation/Forms Utility, ALIS ME 10		Workstation Publishing Software Personal CADAM & CAEDS
<p>Harris supports all design applications on the SDA Framework which runs on most UNIX-based workstations. Industry-standard tools from a number of vendors run on the Framework with a single consistent human interface. This system running on a Sun 3/60 is available to customers as part of an ASIC contract. This system could also be placed on a customer's UNIX platform if that were the preference.</p> <p>The tool suite running on the SDA Framework supports complete front-to-back design including schematic capture, logic simulation with timing and back annotation of parasitics, automatic place and route of macro cells and standard cells; as well as support for full custom design and layout of digital and analog CMOS, GaAs, and bipolar analog designs.</p> <p>In addition, front end applications (schematic capture and logic simulation) are supported for all of the standard cell digital CMOS library (except the LSI functions) on both Daisy and Mentor workstations. The library is available in the form of tape or floppies for these workstations.</p>	<p>The Hewlett-Packard design System provides tools to create products. The many tools available address EE and ME design through manufacturing.</p>	<p>CADAT 6.0 is an integrated simulation environment, supporting logic, fault and worst case timing. The CADAT simulation system is a virtual breadboard that allows a design engineer to debug logic and optimize circuit performance without building a prototype. Test engineers can work with the same CADAT description to develop test vectors. CADAT is ideal for the design of PCBs or ASICs. SSI and MSI components are modeled with CADAT's gate and functional models. LSI and VLSI can be modeled either behaviorally or physically with the CATS modeler. ASIC libraries can be used to simulate gate arrays and standard cell devices. Delay changes caused by fanout loading are automatically calculated by CADAT. Delays can also be calculated from the physical layout and back-annotated into the simulation. Minimum-pulse-width and setup/hold violations are reported to the designer. For PCB design, a worst case timing simulation can be performed to analyze the circuit sensitivity to variations in component device timing.</p>	<p>The heart of the CIEDS/Design Capture family is the common database and common user interface. Since the design file system is common to all options of the CIEDS/Design Capture system, designs can be easily ported between each computing environment while design integrity is maintained. Engineers can begin design portions of a design with a desk-top IBM Personal Computer AT and then easily transfer the information to the more powerful IBM RT Personal Computer or the IBM 5080 attached to an IBM System/370 processor. Engineers will interface to the same system regardless of the hardware environment. To integrate large designs created in multiple computing environments and to confirm that all portions of the logic design cross reference properly, the designs can be transferred from any of the above workstation environments to an IBM System/370 environment. Once on the IBM System/370, or the IBM RT PC, any of four CIEDS/Design Simulation tools can be used to verify the design. IBM documentation tools can be used for creating required technical reference material.</p>

# IC MASTER

## DESIGN AUTOMATION—Workstations

Generic Function

Software/Hardware Tool Name

### Workstation Design Tool Names (Cont'd)

Source	IBM	ICT Computer Drafting Systems	IKOS Systems
Workstation	CIEDS/Design Capture for PC/AT	GENIUS	IKOS 800
FOR DETAILED DATA SEE:			
Tool residence	IBM MAINFRAME/MINI, IBM PC/XT/AT, IBM PT PC, IBM PS/2		IBM PC/XT/AT
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	CIEDS/Design Capture		IKOS 800 IKOS 800
Physical layout Circuit board Gate array Standard cell Full custom			
Programmable logic device devel.			
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system			IKOS 800 IKOS 800
Support Documentation software Mechanical CAD/CAM			
Description	Computer-Integrated Electrical Design Series (CIEDS)/Design Capture is the front-end schematic entry tool for IBM's Electronic Design Automation family of products. It is an interactive graphics-based product that operates on all three of IBM's "Engineering Workstation" platforms: PC/AT, PS/2, RT PC, 5080 Graphics Workstation attached to the System/370 family of processors. CIEDS offers the following: integrated database; hierarchical design; consistent user-interface across hardware platforms, database utility routines, netlist extraction; supports Structured Design Language (SDL); and, Engineering Access Routines (EARS) which supports access into and out of the CIEDS database in user-defined format.	Based on either the IBM PC AT with 80287 co-processor or Ridge 32/110 32-bit RISC computer, ICT's GENIUS performs schematic capture, 36-state logic simulation, timing verification, and PCB interactive layout with auto-routing.	



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Intergraph InterAct 32	Intergraph InterAct 32C	Intergraph InterPro 32	Intergraph InterPro 32C
InterAct 32	InterAct 32C	InterPro 32	Interpro 32
Hierarchical Schematic Design Analog Analysis Tools HILO-3 (see Genrad) HILO-3 (see Genrad) HILO-3 (see Genrad)	Hierarchical Schematic Design Analog Analysis Tools HILO-3 (see Genrad) HILO-3 (see Genrad) HILO-3 (see Genrad)	Hierarchical Schematic Design Analog Analysis Tools HILO-3 (see Genrad) HILO-3 (see Genrad) HILO-3 (see Genrad)	Hierarchical Schematic Design Analog Analysis Tools HILO-3 (see Genrad) HILO-3 (see Genrad) HILO-3 (see Genrad)
Printed Circuit Board/Hybrid Design Sys. TANCELL (see Tangent Systems)	Printed Circuit Board/Hybrid Design Sys. TANCELL (Tangent Systems)	Printed Circuit Board/Hybrid Design Sys. TANCELL (see Tangent Systems)	Printed Circuit Board/Hybrid Design Sys. TANCELL (see Tangent Systems)
HICHIP (see Genrad)	HICHIP (see Genrad)	HICHIP (see Genrad)	HICHIP (see Genrad)
Tech Pubs MDDS	Tech Pubs MDDS	Tech Pubs MDDS	Tech Pubs MDDS
This workstation is intended for users who need a 32-bit ergonomic production station capable of functioning as a standalone schematic design and analysis station under UNIX System V or connected, via Ethernet, to a VAX for printed circuit board and hybrid layout. It is IBM PC-compatible with dual color 19" screens and a 108.6 Mbyte hard disk.	The InterAct 32C is a production-oriented graphics workstation featuring dual color screens and ergonomic design with electronics identical to the InterPro 32C. The 19" high resolution (1184 x 884 pixels) color monitor housing includes a 1.6 Mbyte floppy. The three processors (Clipper from Fairchild, a 5 MIPS machine, Intel 80186, and Intergraph ROP) provide exceptional throughput at a very attractive price.	This workstation is intended for users who need a 32-bit workstation capable of functioning as a standalone schematic design and analysis station under UNIX System V or connected, via Ethernet, to a VAX for printed circuit layout. It is IBM PC-compatible with a color 19" screen and an 80 Mbyte hard disk.	At \$25,000, the InterPro 32C is claimed to have the best price/performance of any workstation on the market. Built around a 5 MIPS Clipper processor from Fairchild, the InterPro 32C has 6 Mbytes of RAM, 80 Mbyte hard disk, a 1.2 Mbyte floppy with a 15" high resolution color monitor. It can execute schematic design and analysis programs as a standalone unit under UNIX System V, or, through its built-in Ethernet controller, access VAX-based Intergraph software. It is also IBM PC compatible and supports GKS.

DESIGN AUTOMATION—Workstations

Generic Function

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Source	Kontron	LSI Logic	M2M Robotics
Workstation	KAD System	LDS ASIC Design System	PDS 2400 Automated Wiring Sys
FOR DETAILED DATA SEE:		page 4653	
Tool residence	IBM PC/XT/AT, Kontron AT-compatible, 1280 x 1024 display	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PYRAMID, SUN, Am-dahl	APPLE, IBM PC/XT/AT, MOTOROLA
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	KAD Editor PSPICE (see MicroSim) CADAT (see HHB Systems) CADAT (see HHB Systems)	LSED (LSI Logic Schematic Editor)  LSIM LDEL LDS (extra hardware needed)	OrCAD (see OrCad, Inc.)
Physical layout Circuit board Gate array Standard cell Full custom	KAD System		smARTWORK (see Wintek)
Programmable logic device devel.	LOG/IC		
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system		Interface to Zycad accelerators Interface to Zycad accelerators	
Support Documentation software Mechanical CAD/CAM	Micro-Tex and others PC-Draft, AutoCAD, Personal Designer		Microsoft WORD AutoCAD
Description	The KAD System from Kontron Electronics includes schematic capture, simulation, and placement & layout of printed circuit boards. The system and supporting hardware can be operated with standard IBM ATs or compatibles, or with Kontron's own AT compatible computer. A separate autorouting hardware package is also available. Interfaces are available to other design automation support systems including HHB Systems' CADAT, MicroSim's PSPICE, and the Calay Autorouter.	The LDS Design System is a front-end ASIC design environment created specifically for design engineers. System components include specialized CAD programs, delay prediction algorithms, cell libraries, sophisticated database architectures, a comprehensive project management system, documentation, training and engineering services. The single-user version of LSI Logic's ASIC Design System is used at the LDS customer site to produce "right the first time" HCMOS ICs. All programs, cell models and technology-specific data are equivalent to those used at LSI design centers. The LDS Design System is an expert CAE/CAD system built around proprietary design features, chip technologies and manufacturing specifications. Design engineers rely not only on its advanced software technologies, but also on its integration with LSI Logic's manufacturing facilities.  These facilities currently produce five user-specific design prototypes per day, including 1.5-micron and 2-micron double-metal, and 3-micron single-metal HCMOS in a variety of array and cell configurations. Using the LDS System, a design engineer selects the best LSI Logic ASIC product for a specific application.	M2M Robotics' PDS 2400 fully automated wirewrapping system requires no full-time operator. One operator can handle several units with ease. Error detection and correction: The PDS 2400 performs a continuity test on each wrap and will detect and undertake to correct the bad wrap. It is specially designed to handle prototype electronic breadboards, production printed circuit/wirewrapped boards and ATE test fixtures. The PDS 2400 can perform up to 400 wraps per hour and therefore, wirewrap several boards in a single day. Since the PDS 2400 stores wire lists in RAM, several boards can be wirewrapped without having to reprogram for each wiring pass. CAD interfaces and support utilities that enable users to go from their schematic package such as P-CAD, Mentor, FutureNet, and Daisy, directly to the PDS 2400. The PDS 2400 will cut development time enabling engineers to develop products more quickly.

Bold face indicates data is provided in the page noted



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Matra Design Systems MDS	Mentor Graphics Board Station	Mentor Graphics Capture Station	Mentor Graphics Cell Station
DEC VAX, IBM PC/XT/AT	APOLLO	APOLLO	APOLLO
SEGA ARCIS ARCIS COFIS	Neted Quicksim Quicktime Quickfault	NETED	NETED RSIM
ALGA, KLGA	Pathlink		CELLGRAPH, CELLPLACE, CELLROUTE
CHECK, EVAL			
	Doc Librarian	DOC	DOC
	Board Station is a complete CAE/CAD design automation system for the development of PCB-based systems. It fully supports every phase of the design and layout cycle, including outputs to manufacturing, and is capable of working with most advanced PCB technologies, including surface mount devices and multi-layer boards.	Capture Station provides a complete design capture capability for the creation of even very large electronic designs. This station includes the NETED bit-mapped network editor as well as a flexible Relational DBMS with analysis facilities. The NETED schematic capture package is designed to allow a rapid learning curve without penalizing the experienced user. It features a user interface with mouse driven pop-up menus, function keys, and a command macro language. In addition, the user interface is programmable so that users may customize the application to their individual taste and environment.  Capture Station allows a designer to work hierarchically or use flat design techniques. Symbols are available from Mentor Graphics standard parts libraries or can be user-developed. Electrical connectivity is maintained during editing and electrical rule checking is performed. Multiple windows allow copying between schematics for efficient design entry.	Cell Station is a workstation for the complete logic and physical design of standard cell integrated circuits. Standard cells offer versatility and economy by allowing integration of many different functional elements on one chip, and Cell Station helps the designer thoroughly exploit the potential of standard cell technology. All tools used on Cell Station use the same interface and database for a streamlined standard cell design cycle. Designers may work at any level in the design hierarchy.

## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation FOR DETAILED DATA SEE:	Mentor Graphics Chip Station	Mentor Graphics Design Station	Mentor Graphics Development Station
Tool residence	APOLLO	APOLLO	APOLLO
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	NETED (opt.) (opt.) (opt.) (opt.)	NETED	
Physical layout Circuit board Gate array Standard cell Full custom	(opt.) (opt.) (opt.) CHIPGRAPH		
Programmable logic device devel.	(opt.)		
Silicon compilation	SST's CONCORDE or SCI's GENESIL		
IC layout verification	Interactive DRC/DRACULA II(ECAD)/REMEDI		
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system	(optional) (opt.) (opt.) (opt.)		
Support Documentation software Mechanical CAD/CAM	DOC	DOC	
Description	Chip Station is a workstation for the design of custom integrated circuits. Sophisticated mask editing functions integrated on a high-performance workstation offer the capabilities and processing power needed to develop complex VLSI circuits. The Chip Station system includes the Mentor Graphics CHIPGRAPH layout editor, schematic viewing capability, network editor, expand, and documentation preparation system.	Design Station includes all of the schematic capture and database software provided with Capture Station as well as the four additional tools described below.  DOC is an automated documentation preparation package integrated with the Mentor Graphics design, analysis, and layout tools database. Graphics from schematic or layout design files or waveforms from simulator output may be directly included in any document text. The Sheetlister/Pictu relister interface package allows users to integrate Mentor Graphics tools with their internal CAE and CAD tools. These tools allow the schematic database to be scanned or analyzed procedurally from a user-written program. The RSIM interface allows remote simulation of designs using the Mentor Graphics Quicksim family of digital simulators. The local Design Station is used for preparing simulation input, controlling the simulation run, and displaying output waveforms. The QuickPart Builder/Timing Editor allows the designer to create compact functional models using a simple pin-to-pin timing file and an existing electrical schematic. These models provide greater throughput and accuracy during simulation.	Mentor Graphic's Development Station is a comprehensive workstation-based set of software tools that allows users to build and maintain their own applications on the Mentor Graphics Compute Engine global accelerator. Included in the Development Station tools are: C, Fortran and Pascal optimizing compilers; a linker; a symbolic debugger and two librarians. These tools provide the capability to port a wide range of compute-intensive applications onto the Compute Engine, such as CAE/CAD tasks and general engineering and scientific applications.  The Development Station/Compute Engine combination provides a global acceleration solution for compute-bound problems. This approach is different from special-purpose hardware or microcoded accelerators which speed up a single point in the design cycle. Using Development Station, existing algorithms in standard high-level languages can be compiled into the Compute Engine. The user isn't required to rewrite any source code, a frequent limitation of other parallel machines. Instead, the Development Station compilers recognize the low-level parallelism inherent in the algorithms and exploit Compute Engine's parallel pipelined architecture to achieve high throughput for all tasks, not just for one problem area.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Mentor Graphics Gate Station	Mentor Graphics Idea Station	Micro Linear Linear CAD II	Micro Power Systems MCAD
APOLLO	APOLLO	IBM PC/XT/AT	DEC VAX, IBM PC/XT/AT
NETED RSIM	NETED MSPICE/MSIMON (opt.) QuickSim QuickTime QuickFault (opt.)	Linear CAD II PSPICE	CT-2000 SPICE, PSPICE (Meta-Software) SILOS, PSILOS (Simucad)
GATEGRAPH, GATEPLACE, GATEROUTE	(Opt.) (Opt.) (Opt.) (Opt.)		Calma GDS II Calma GDS II
			DRACULA (see ECAD)
	(Opt.) (Opt.)		PSPICE/Turbine
DOC	DOC		
Gate Station is a workstation for the complete logic and physical design of gate array integrated circuits. Gate arrays are an increasingly popular answer to the demand for application-specific ICs, and Gate Station can help create them in the most efficient and productive way. Gate Station streamlines the entire gate array design cycle by using the same interface and database for all tools. Designs may be created either hierarchically, or using flat design techniques.	Idea Station provides complete design capture, simulation, and documentation capabilities. Included in the Idea Station is IDEA Series software for design development using either hierarchical or flat design techniques. The user interface is identical to that on other IDEA Series stations, and includes multiple windows, pop-up hierarchical menus, context and edit views, programmable function keys, and stroke recognition.	Linear CAD II is a software package for the design of application specific linear and linear/digital integrated circuits which turns a PC into a design workstation. The software package runs on the PC-XT or PC-AT with schematic entry at the macro cell or component level. Linear CAD II is fully characterized and modeled for SPICE simulation on a PC or VAX system with output to either a dot-matrix printer or pen plotter. Design is facilitated by the use of 29 Macro Cells, ranging from an NE592-equivalent video amplifier to an NE555-equivalent timer. These macro cells, along with the ability to use the standard components library, allows the designer to implement an ASIC design easily. Once design is complete, circuit analysis is aided by a monitor which appears similar to an oscilloscope display.	

DESIGN AUTOMATION—Workstations			
Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source Workstation FOR DETAILED DATA SEE:	Modula MODULA	National Semiconductor Design Automation System page 4294	NCR Microelectronics NCR VISYS
Tool residence		IBM MAINFRAME/MINI, IBM PC/XT/AT, Daisy, Mentor, FutureNet workstations	Popular workstations
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation		Daisy, FutureNet, HP, Mentor  Daisy, FutureNet, Mentor Daisy, FutureNet, Mentor	Workstation-based Workstation-based Workstation-based VITA Series Workstation-based
Physical layout Circuit board Gate array Standard cell Full custom		MERLYN-G (IBM mainframe/VAX)-see Tek/ MERLYN-S (IBM mainframe/VAX)-see Tek/	
Programmable logic device devel.			
Silicon compilation			VIGEN
IC layout verification		DRACULA (IBM mainframe/VAX) (see ECAD)	VILAY
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system			
Support Documentation software Mechanical CAD/CAM			
Description	The MODULA system provides a complete coordinated, and affordable set of tools designed to place Computer Aided Circuit Design Engineering at the desk of design professionals. Easy to use mouse-driven editing features, using pop-up menus, increase the speed and the ease of schematic design as well as the design, layout, and verification of printed circuit boards. Integrated post-processors provide the complete spectrum of support functions for creating complete professional quality design and manufacturing documentation. Netlists, parts lists, design rule check reports, plotted schematics and PCB artwork are automatically created by the system. The system runs on MODULA's high-performance co-processor attached to IBM PCs and compatibles.	The Design Automation System is intended for use with National Semiconductor's gate arrays and standard cells. National supplies workstation design kits which consist of floppy disks with: 1) the symbol library for schematic capture of designs to be implemented in gate arrays or standard cells from National Semiconductor; 2) a program to extract a pinlist from the captured schematic; 3) another program to assist the designer in generating the test vectors for the design; 4) all the information required to simulate functionality and AC-performance of the gate array- or standard cell design; and, 5) communication software to enable the user to send the design and its test vectors to National's mainframe for timing verification, fault grading, place and route and generation of database tape and test tape.  Databooks and application notes help the user to quickly get familiar with National's gate arrays and standard cells and tell how to take advantage of technical consultants in National's training and design centers.	NCR VISYS, NCR Microelectronics' ASIC design system, for the design of NCR gate arrays and cell-based devices is a modular system. The designer can choose the degree of design control and function options to suit his needs, with ease of adding/expanding capabilities. Options range from design capture to complete layout and post-layout verification of gate array and cell-based designs. NCR has ported VISYS to leading engineering workstations to minimize the need for mainframe resimulations and give the user more design control. VISYS has configurable cell generators (silicon compilation), within the same design system as high-level function cells ("Supercells"), standard cells and gate arrays. Designs can be "migrated" between libraries, which means that a gate array design can be converted to a cell-based design for cost reduction, to add generated high-level functions or to move to a new process geometry library. Leadership timing analysis and test program generation software speed and ease the total design cycle from design start to production.  The major components of NCR VISYS include: Capture Package for schematic capture and basic simulation. Verification Package for pre-layout and post-layout analysis and test generation, featuring VITA series of timing analysis tools and VITEST series of test program generation tools. Layout Package with NCR's VILAY layout and post-layout tools. Opt. VIGEN cell compiler.

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DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Optima Technology OPTIMATE	P-CAD CAE-1	P-CAD CAE-2	P-CAD EDA-1
APOLLO, DEC-VAX, DEC MICROVAX	IBM PC/XT/AT	IBM PC/XT/AT	IBM PC/XT/AT
OPTIMATE Design	PC-CAPS (see Design Tool Interfaces)	PC-CAPS (see Design Tool Interfaces) LOGS II	PC-CAPS (see Design Tool Interfaces) LOGS II
OPTIMATE Place and Route			PC-CARDS
	CUPL (optional)	CUPL (optional)	
OPTIMATE provides highly interactive CAD software that allows the designer to move smoothly from schematic entry, through component placement, optimization and routing to manufacturing output. The designer may explore possibilities at any stage of the PCB design, stop, make changes, consider alternatives, and still call on automatic tools to handle necessary repetitive tasks. The designer specifies when and how to use the automatic placement, optimization and routing power of OPTIMATE's software. The result is a design that incorporates advanced CAD capabilities with the designer's ingenuity-- in short, a better and quicker PCB design.	Schematic Design System. Fully integrated software provides hierarchical schematic capture (PC-CAPS), multisheet linking, netlist extraction and formatting, bill of materials, & printer/plotter support. Package includes software, users manuals, and CAE-1 security device.	Logic Design and Simulation System. Provides all of CAE-1 plus a mixed-mode, 12-state, event-driven logic simulation system (LOGS II) with interactive user control, behavioral modeling, and post-processing capabilities. Package includes software, users manuals, and CAE-2 security device.	Electronic Design System. Fully integrated software provides all of CAE-2 plus printed circuit board layout (see PCB-1 description) and design rule checking. Package includes software, user's manuals, and EDA-1 security package.

# IC MASTER

DESIGN AUTOMATION—Workstations			
Generic Function	Software/Hardware Tool Name		
Workstation Design Tool Names (Cont'd)			
Source	P-CAD	P-CAD	P-CAD
Workstation	PCB-1	PCB-2	PCB-3
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	IBM PC/XT/AT	IBM PC/XT/AT
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation		PC-CAPS	PC-CAPS
Physical layout Circuit board Gate array Standard cell Full custom	PC-CARDS	PC-CARDS	PC-CARDS, PC-PLACE, PC-ROUTE
Programmable logic device devel.			
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system			
Support Documentation software Mechanical CAD/CAM			
Description	Basic PCB CAD System. Fully integrated software provides printed circuit board layout and design (PC-CARDS), logic and component packaging, design rules checking, netlist extraction and formatting, bill of materials, printer/plotter support, and back annotation. Package includes software, users manuals, and PCB-1 security device.	End-to-end PCB Design System. Provides schematic capture (PC-CAPS) and multisheet linking plus all of PCB-1 resulting in a fully integrated End-to-End PCB CAD system. Package includes software, users manuals, and PCB-2 security device.	Automated PCB Design System. Provides automatic placement (PC-PLACE) and automatic trace interconnecting (PC-ROUTE) plus all of the features from PCB-2. Package includes software, users manuals, and PCB-3 security device.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Praxis Systems ELLA	Racal-Redac REDCAD	Racal-Redac REDSIM	Racal-Redac VISULA 3.0
APOLLO, DEC VAX, DEC MICROVAX, SUN	IBM PC/XT/AT	IBM PC/XT/AT, with co-processor board	APOLLO, DEC MICROVAX, IBM PC/XT/AT
ELLA	REDLOG	REDLOG REDSIM CADAT (also see HHB Systems) REDSIM CADAT (also see HHB Systems) REDSIM CADAT (also see HHB Systems)	SCM SPICE VISULA CADAT (also see HHB Systems) VISULA CADAT (also see HHB Systems) VISULA CADAT (also see HHB Systems)
	REDBOARD		VISULA PCB
		CATS (optional) (see HHB Systems)	CATS (optional) (see HHB Systems)
<p>The ELLA Design System is a VLSI design system based upon a behavioral hardware description language, a simulator and comprehensive design support environment. ELLA is unique among behavioral languages in that it has a common notation for behavior and structure. This means that the decomposition of behavior to structure is very efficient, significantly speeding up the design process. Additionally, ELLA is a succinct, yet very powerful language and is easy to learn and use. A procedural interface is provided to the ELLA database which allows translations of designs to lower-level tools.</p> <p>The ELLA system is now in use in many of the UK's major electronics companies significantly reducing design time and cost and increasing design quality. ELLA is marketed in the U.S. by ECAD, Inc.</p>	Netlist compatibility with other Redac Systems.	Netlist compatibility with all other Redac systems.	<p>Visula, release 3.0 provides the electronic engineer with a complete set of tools that integrate the front end of the CAE design process--schematic capture, logic simulation and waveform analysis-- with the back-end capability for physical design. In addition, version 3.0 supports the most recent CADAT hardware simulator (version 5.1) from HHB Systems. CADAT 5.1 accommodates worst-case design capabilities with its new 21 state minimum/maximum algorithm. Combining this algorithm with the integrated hardware modeling and acceleration capability provides Visula with one of the most powerful simulation products available.</p> <p>Release 3.0 also extends Visula's capability to accommodate manufacturing information while using surface-mount devices for the design of printed circuit boards. For example, all information on any layer associated with the SMD component, such as pads and solder resists, is incorporated automatically in the design and manufacturing database, making the manufacture of printed-circuit boards more efficient. In addition, Visula 3.0 allows engineers to design split power planes, which allow them to mix analog and digital technologies on a single multilayered board.</p>

DESIGN AUTOMATION—Workstations			
Generic Function	Software / Hardware Tool Name		
Workstation Design Tool Names (Cont'd)			
Source	Raytheon Semiconductor Div.	Royal Digital Systems	Scientific Calculations
Workstation	Raytheon Design System	AutoMate	SC MC68020 Design Station
FOR DETAILED DATA SEE:	page 4296		
Tool residence	Daisy, Mentor, FutureNet, PCAD worksta.	CONTROL DATA, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, PRIME, SUN, TEKTRONIX	Scientific Calculations MC68020
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	Daisy, Mentor, P-CAD, FutureNet SPICE on Mentor, SPICE on DEC VAX Daisy, Mentor, Calma, LDS, LDS Timemill, LDS Zycad	AutoMate Schematic System AutoMate Circuit Simulator AutoMate Logic Simulator AutoMate Logic Simulator	SCHEMACTIVE
Physical layout Circuit board Gate array Standard cell Full custom	MEDS (see Scientific Calculations) MEDS (see Scientific Calculations) MEDS (see Scientific Calculations)	AutoMate Physical Design System	SCICARDS
Programmable logic device devel.			
Silicon compilation			
IC layout verification	NCA, LDS		
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system	Zycad Zycad		
Support Documentation software Mechanical CAD/CAM			
Description		<p>AutoMate system features include: easy to use design automation tools with no sacrifice of power for friendliness; rapid productivity increases; integrates engineering design, and manufacturing; aids electronic designers from circuit schematic capture through final tooling and testing for PCB, SMT, and hybrid circuits. Simulation ensures that engineering is completed before physical design begins. Continuity and clearance verification ensure that physical design is completed before manufacturing. Shared data ensure that engineering changes are reflected throughout a design.</p> <p>The AutoMate software supports completedocumentation such as assembly drawings, bills of materials, net lists, logic diagnostics, manufacturing drawing including drill summary or quantity and size, and location.</p>	<p>The SC Design Station is a fully integrated standalone computer specifically designed to run advanced CAD/CAM software. It is based on the Motorola MC68020 microprocessor and offers high speed color raster graphics.</p>



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Scientific Calculations SCIDESIGN	SDA Systems CustomEdge	SDA Systems Design Framework	Silicon Compiler Systems GENESIL
IBM PC/XT/AT	APOLLO, DEC MICROVAX, HEWLETT-PACKARD, MASSCOMP, SUN	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC VAX, DEC MICROVAX, Daisy and Mentor workstations
SCIDESIGN	Graphics Editor SPICE 2G.6 SILOS (Simucad) Timing Analyzer SILOS (Simucad)	SPICE, HSPICE (see Meta-Software) SILOS (see Simucad), HILO (see Genrad) SDA Timing Analyzer SILOS (see Simucad)	via Daisy or Mentor interfaces GENESIL Functional Simulator GENESIL Timing Analyzer HILO-3 (see Genrad)
	LAYOUT	SDA Place & Route SDA Layout	
			GENESIL Silicon Development System
	PDCHECK, PDExtract, PDCOMPARE,	PDcompare, PDextract, PDcheck	
	TestEdge		Interface to I.M.S. tester
<p>SCIDESIGN is an IBM Personal Computer based electronic design engineering tool. It features an integrated schematic sheet editor, symbol library, graphical symbol editor, and optional circuit simulation package. It provides the engineer with the capability to generate schematic diagrams, perform design rule checks on the circuit, generate net lists and a user accessible ASCII file of all SCIDESIGN data including graphics. Furthermore, those users of the SCISIM System are able to perform logic simulation on either all, or a portion, or the circuit as defined by SCIDESIGN.</p> <p>Included in SCIDESIGN Release 3.0 is the capability for the user to extract any SCIDESIGN data of interest, in a file structure of his own choosing, thus greatly reducing his dependence on an outside vendor for the supply and ongoing support of interfaces to other systems, whether commercially available or internally developed.</p>	Full custom layout.	Complete integrated system for doing all phases of IC design. All tools and design data are accessible from the SDA Design Framework. It provides a single consistent user interface for all tools as well as a unified database for storing design information.	<p>The GENESIL Silicon Development System includes all of the necessary tools to complete the design of an integrated circuit: design definition and edit, simulation, timing analysis, placement and routing, and database management.</p> <p>The GENESIL System is available in single user through 10-user configurations and is currently available on VAX, MicroVAX, Apollo, and Daisy hardware platforms. NMOS and advanced two layer metal CMOS function sets are available on the GENESIL system. Circuits designed on the GENESIL System can be manufactured in either technology at a number of Silicon Compilers Inc. franchised foundries.</p>

## DESIGN AUTOMATION—Workstations

Generic Function

Software/Hardware Tool Name

### Workstation Design Tool Names (Cont'd)

Source	Silicon Compiler Systems	Silvar-Lisco	Standard Microsystems Corp.
Workstation	GENESIS	SL2000	STANSURE
FOR DETAILED DATA SEE:			page 4310
Tool residence	DEC VAX, DEC MICROVAX	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, Mentor, Daisy, Valid
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation		Structured Design System SPICE/TURBOSPICE (see Shiva Multisystems) HELIX  HELIX	Daisy, Mentor, Valid SPICE CADAT (see HHB Systems) STANTIME CADAT, THESEUS (see HHB Systems)
Physical layout Circuit board Gate array Standard cell Full custom		OPTIMATE (see Optima Technology) GARDS CAL-MP PRINCESS	TANCELL (Tangent Sys) CAL-MP (SilvarLisco)
Programmable logic device devel.			
Silicon compilation			STANCOMP
IC layout verification		DVS (formerly offered by NCA)	DRACULA (see ECAD Inc.)
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system		Interface to Zycad Interface to Zycad	
Support Documentation software Mechanical CAD/CAM			

#### Description

The GENESIS Compiler Development System contains the tools which enable the IC designer to create parametric compilers which operate in the GENESIL design environment. The compiler development tools include: geometric model synthesis, timing model synthesis, functional model synthesis, power model synthesis, logical design rule model, and a human interface design language plus a comprehensive design verification environment.

The SL2000 Workstation, which runs on VAX, microVAX, VAXstation, Apollo and IBM mainframes performs a wide range of front-end to back-end design tasks. Schematic entry is performed using the SDS Structured Design System. Analysis tools include SPICE or TurboSPICE for circuit simulation, HELIX for multi-level logic simulation. Shiva Multisystem's TurboSPICE accelerates circuit simulation while Zycad's Logic Evaluators speed up logic simulation. All physical implementations are supported: printed circuit board layout using Optimate; gate array layout using GARDS; standard cell layout using CAL-MP; and full custom layout using Princess. Design verification for IC layout uses a set of comprehensive tools previously supplied by NCA Corp. and now provided by Silvar-Lisco. Interfaces are provided to production testers from Teradyne. Software can be purchased with or without hardware.

STANSURE is the software portion of SMC's CUSTOMATION standard cell design system. The cell library portion consists of analog and digital cells, including many Super-Cells. STANSURE consists of: STANNET- works with workstation-based schematic capture tools to convert netlists into common database and verifies all results. STANSIM- provides logic simulation interfaces between workstations and back-annotation. STANTIME- timing verification programs calculates and displays typical and worse case propagation delays (rise and fall times) of each circuit element. May be run before or after layout. Also calculates cumulative propagation delays of each path in design. STANCOMP- provides chip layout and design rule checking functions. Also checks layout extracted netlist vs. logic netlist. STANWIRE- produces wirewrap emulation board from logic netlist for functionality checking. STANTEST- produces Sentry or Genrad compatible test files from simulation vectors. STANFAULT workstation-based fault grading programs: CADAT and Theseus which run on VAX equipment.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Tektronix CAE Systems Designer's Worksystem page 4658	Tektronix CAE Systems Full Custom WorkSystem page 4658	Tektronix CAE Systems Gate Array WorkSystem page 4658	Tektronix CAE Systems PCB WorkSystem page 4658
APOLLO, DEC VAX, DEC MICROVAX	DEC VAX, DEC MICROVAX, TEKTRONIX	APOLLO, DEC VAX, DEC MICROVAX	APOLLO, DEC VAX, DEC MICROVAX
DDSC HSPICE (see MetaSoftware), SPICE opt. HILO-3 opt. (see Genrad) HILO-3 opt. (see Genrad)	DDSC SPICE	DDSC HILO-3 (see Genrad) HILO-3 (see Genrad) HILO-3 (see Genrad)	DDSC HSPICE (see Meta-Software), SPICE opt. HILO-3 opt. (see Genrad) HILO-3 opt. (see Genrad) HILO-3 opt. (see Genrad)
I/F to Calay VO4	LEIA	MERLYN-G; TurnChip ASIC Layout Modules	MERLYN-P
Opt.			
	DRACULA II (see ECAD Inc.)	Opt.	
HICHIP (see Genrad) I/F to Zycad I/F to Zycad		Opt.	HICHIP opt. (see Genrad) I/F to Zycad I/F to Zycad
TekWriter TekniCAD	TekWriter	TekWriter	TekWriter
Complete worksystem integrating design capture, documentation and verification tools with Tektronix database for schematic entry and simulation of circuits or boards for analog, digital, or microwave circuits. The Designer's WorkSystem supports HP pen plotters, Cal-comp pen and electrostatic plotters.	Complete worksystem for design of digital, analog, microwave, and hybrid integrated circuits. Tools provided for schematic capture, circuit simulation, and physical layout. DDSC is provided for schematic entry, and SPICE for circuit simulation.  The LEIA interactive graphical layout editor is especially suited for custom analog bipolar and gallium arsenide applications. LEIA's flexible interface provides multiple windows, pop-up menus and the ability to customize real-time user configurable menus.  The Full Custom WorkSystem gives you the added flexibility of using DDSC and Compact Software's SuperCompact to create a complete microwave circuit design environment.  The DRACULA Layout Verifier from ECAD Inc. allows you to measure and display design rule checker errors, extract parasitic electrical parameters, and compare your layout to your schematic.	An integrated set of design tools that provides a complete solution for designing gate arrays. A performance driven design environment is created with tools for schematic capture, logic and fault simulation, timing verification, and automated push-button layout. The Gate Array WorkSystem also offers unique TurnChip ASIC Layout Modules for automatic control of physical layout.  The Gate Array WorkSystem effectively reduces your time to market, improves design performance, provides proprietary design control by allowing all design processes to be performed at customer site, and reduces overall design costs.	Complete worksystem for electronic design capture, logic simulation, physical layout and output for computer aided manufacturing. The PCB WorkSystem accommodates layout and manufacturing constraints on the most complex board designs, including fine line technology, mixed surface mount and through-hole devices and components placed on top and bottom surfaces of the board. Engineering change orders are efficiently managed. Standard component libraries are compatible between schematic capture, simulation and layout. Full forward and back annotation between schematic capture and layout is provided. The PCB WorkSystem generates standard artwork, checkplots, documentation, and data needed to link layout to automated manufacturing.

## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source	Tektronix CAE Systems	Teradyne	The Great Softwestern Company
Workstation	Signal Processing WorkSystem	DATAView	Auto-Board System II
FOR DETAILED DATA SEE:	page 4658		
Tool residence	APOLLO, DEC VAX		
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	DDSC  Simulation Program Builder (Functional)		
Physical layout Circuit board Gate array Standard cell Full custom			
Programmable logic device devel.			
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system			
Support Documentation software Mechanical CAD/CAM	TekWriter		
Description	<p>The Signal Processing WorkSystem (SPW) combines in one integrated package all the tools needed to design, simulate and test digital signal processing (DSP) systems. It integrates, under a common user interface, DDSC for DSP system design capture with a proprietary Simulation Program Builder (SPB) for DSP simulation including a Function Block Library (FBL) and an Instrument Interface Library I,(IIL). A closely-coupled Signal Display Editor (SDE) provides the functions for signal definition, capture and analysis.</p> <p>Dramatic productivity improvements are achieved by allowing the designer to concentrate on the DSP algorithm rather than the hand coding of a custom simulation program. The SPW automatically takes care of turning the schematically captured algorithm block design of a signal flow diagram (augmented with flow of control) into a simulation program.</p>	<p>DATAView is an integrated personal-computer based program which provides a common user interface for schematic entry, simulation and anlysis using the LASAR Version 6 simulation system. DATAView, which runs on the IBM PC AT and compatible personal computers, also includes documentation and electronic mail capabilities. Based on Viewlogic Systems Inc.'s popular WorkView design program, DATAView is a proprietary, customized package whose schematic data is read directly by LASAR to provide the high-speed model compilation essential for fast simulation response times. LASAR's simulations are run on a VAX computer or on the DATAServer simulation server, and are accessed over Ethernet from the PC-AT design station; thus, engineers have access to the large capacity and power of a mainframe for creating, simulating, and storing much larger designs than could be handled by the PC alone.</p> <p>The engineer initiates LASAR simulations, and views waveform analyses and other simulation results, using the same mouse-driven system of pop-up, look-ahead menus presented by DATAView schematic entry, documentation, and electronic mail functions.</p>	<p>The Auto-Board System II is a set of printed circuit design aids for schematic capture, component layout and auto-routing of printed circuit boards. The Auto-Board System II is a companion software design tool for AutoCAD. The major change from earlier versions is the auto-routing module. This design tool can be configured to match the requirements of the user. The designer has control of trace and pad spacing, the size of the individual traces (with calculated clearances), default feed-through sizes and default trace sizes. The new system allows 1 mil resolution for the free placement of parts and signal traces.</p>

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**DESIGN AUTOMATION—Workstations****Software/Hardware Tool Name****Workstation Design Tool Names (Cont'd)**

Thomson/Mostek HIGHLAND 2 page 4321	Trimeter Technologies Consultant Family	Valid Logic Systems Inc. Analog Design System page 4660	Valid Logic Systems Inc. Board Design System page 4660
DEC VAX	APOLLO	DEC MICROVAX, IBM PC/XT/AT, SUN, Valid SCALDSsystem	DEC MICROVAX, SUN
TRANS SPICE SIM SIM, CPA FSIM	Logic Consultant, Knowledge Consultant  Knowledge Consultant	ValidGED Precise	
PATHLINK, AUTOLINK CAL-MP			Allegro
DRACULA, Net Check			
Hardware Modeling Library  Logic Evaluator Fault Evaluator Comet, TIF			
		Interleaf (Opt.)	Interleaf (Optional)
Mostek design automation system can be entered at any stage from workstations supported.	<p>Trimeter's Logic Consultant is an expert system-based, complementary CAE tool for ASIC logic design optimization. It allows you to create ASIC logic designs that use fewer gates and/or run faster without changing your current design methodology.</p> <p>The Logic Consultant accepts input logic designs as netlists from Mentor Graphics systems with generic or foundry-specific symbols, as boolean equations or in PLD format.</p> <p>The Logic Consultant first minimizes the design's logic and evaluates timing constraints. Then, using expert system technology, the Logic Consultant selects the optimal combination of cells and macrocells from the targeted ASIC library which provide the required performance and/or the least area possible.</p> <p>The Logic Consultant's Schematic Analyzer allows you to then quickly estimate propagation delays through selected signal paths, find the longest and shortest delay paths and calculate the associated timing delays of both the high-to-low and low-to-high signal changes.</p>	<p>The Analog Design System provides analog designers with a natural convenient way to design and simulate their analog circuits. It integrates schematic capture, simulation, documentation, and layout of analog designs in one system. Now an analog engineer can experiment with a design and ask "what if" questions before building actual hardware.</p> <p>The computer-modeled lab bench provides a familiar environment in which to design with a variety of test equipment including a function generator, an oscilloscope, a voltmeter, and a network analyzer.</p> <p>The Valid analysis tools bundled in the system include ValidGED graphics editor, Precise circuit simulator, and ValidPACKAGER Logic-to-layout physical translator.</p>	<p>The first rules-driven PCB design system that allows design engineers to control the physical implementation of their designs. Designers use ValidGED to attach properties to components and wires, and Allegro interprets those properties as design rules that must be followed during the physical design of the PCB.</p> <p>Supports the front-to-back layout process for digital, analog, and high-frequency circuit technologies. Offering an icon-oriented user interface, Allegro provides almost unlimited design capacity, with no constraints on numbers of components, pins, or nets supported in a single design.</p> <p>Netlists may be transferred directly from Valid and other CAE systems. Automatic gate assignment tools work exceptionally fast.</p> <p>Component placement is supported by floorplanning capability, which helps the designer logically segment and place components. The Allegro router, called INSIGHT, supports simultaneous routing of up to eight layers at a time (with a maximum of 50 signal layers) and includes rip-up/re-route and glossing algorithms to ensure high completion rates and optimized manufacturability.</p> <p>Available in interactive, automatic, or combined configurations.</p>

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DESIGN AUTOMATION—Workstations			
Generic Function	Software/Hardware Tool Name		
Workstation Design Tool Names (Cont'd)			
Source	Valid Logic Systems Inc.	Valid Logic Systems Inc.	Valid Logic Systems Inc.
Workstation	Design Entry System	Design Validation System	IC Design System
FOR DETAILED DATA SEE:	page 4660	page 4660	page 4660
Tool residence	DEC MICROVAX, IBM PC/XT/AT, SUN	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, Valid SCALDSsystem	DEC MICROVAX, SUN, Valid SCALDSsystem
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	ValidGED	ValidGED See Valid's Analog Design System ValidSIM ValidTIME LASAR 6 (optional, see Teradyne)	ValidGED Precise (optional) ValidSIM ValidTIME; TIMEMILL (Opt., see Epic) LASAR 6 (Optional, see Teradyne)
Physical layout Circuit board Gate array Standard cell Full custom			ValidBLOCKS (Opt.), ValidCOMPOSE (Opt.) ValidLED
Programmable logic device devel.		ValidPLD (Optional)	
Silicon compilation			Concorde (Optional)
IC layout verification			ValidDRC/EXTRACT, ValidCOMPARE/ERC
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Intergrated test system		Realchip, Realmodel (Optional)  Realfast (Optional)	Realchip or Realmodel (Optional)  Realfast (Optional)
Support Documentation software Mechanical CAD/CAM	Interleaf (Optional)	Interleaf (Optional)	Interleaf (Optional)
Description	Designed to bring low cost schematic capture right to the designer's desk, the Design Entry System is based on the ValidGED graphics editor, and provides a schematic capture front end to the Valid Integrated Engineering System. It is intended for multi-user environments where other systems are available (via Ethernet or RS-232 lines) to continue the design process.	A full-function CAE solution for logic designers. The Design Validation System addresses the needs of designers who require a high-performance solution to verify entire system designs.  ValidTOOLS, Valid's second generation analysis software provides an integrated set of tools for interactive schematic capture, verification and netlist generation. ValidGED graphics editor and ValidPACKAGER provide user-friendly design entry and translation to your preferred physical implementation. The ValidSIM logic simulator and ValidTIME timing verifier help designers validate their design and isolate design flaws.  A full line of libraries includes all of the commercially available technologies-- TTL, ECL, CMOS, and HCMOS--, plus 40 ASIC vendors with over 100 design kits. Coupled with Realmodel hardware system simulation, the Design Validation System can verify entire system-level designs quickly and efficiently.	The IC Design System combines the industry's first workstation-based CAE tools with advanced IC layout software into a single VLSI design solution. Schematic capture, simulation, layout editing and analysis all run from a single integrated database. There's no need to transfer files or convert formats, leaving designers more time to build and debug circuits.  ValidLED, the layout editor, sets new standards for productivity. User-configurable menus, scripts and multiple viewports allow a user to customize the user interface. Dynamic graphics give continuous feedback of where objects are placed. A powerful group capability provides wires that understand connectivity.  Complete mask verification including DRC, ERC, circuit extraction, and logic-to-layout comparison is available at the touch of a button. The tools may be run directly from the layout editor or from the operating system environment. Since the mask verification is hierarchical, analysis is fast and accurate, and provides for more accurate error reporting. Bidirectional GDS II, CIF, and EDIF interfaces are available.



DESIGN AUTOMATION—Workstations

Software/Hardware Tool Name

Workstation Design Tool Names (Cont'd)

Valid Logic Systems Inc. Logic Design System page 4660	Valid Logic Systems Inc. Mask Design System page 4660	Valid Logic Systems Inc. Silicon Design System page 4660	Vamp EOS-1
DEC MICROVAX, IBM PC/XT/AT, SUN, Valid SCALDSsystem	DEC MICROVAX, SUN, Valid SCALDSsystem	Valid SCALDSsystem	APPLE
ValidGED	ValidGED	ValidGED ValidSIM TIMEMILL (Optional, see Epic)	EDSC Logic sim Logic sim
	ValidLED ValidLED ValidLED	ValidLED	PCB Design, Autorouter, CPlace
		Concorde(see Seattle Silicon Technology)	
		See Valid's IC Design System	
Interleaf (Optional)	Interleaf (Optional)	Interleaf (Optional)	
<p>Designed to provide both low cost and a standalone CAE workstation, the Logic Design system provides a truly cost effective solution for improving productivity.</p> <p>Schematics created on the Logic Design System are compiled into a logic design database using the ValidCOMPILER. The compiled design is now ready for additional processing such as simulation. The logical design can be packaged into a physical design database using the ValidPACKAGER. The physical design database can be accessed by various ASIC or CAD interfaces to create the information (netlist, parts lists, etc.) required by ASIC vendors or by PCB CAD systems.</p> <p>For simulation (or some other additional processing) the schematics or compiled design can be easily transferred via Ethernet or RS-232 to another system where ValidSIM (or other ValidTOOLS) can be used. The engineer can interactively control and view the simulation running on the other system from the Logic Design System.</p>	<p>Designed specifically for the mask designer, the Mask Design System provides for a standalone, low-cost solution for basic integrated circuit layout. Design may be created using ValidLED layout editor and ValidGED graphics editor.</p> <p>The designer can create or import designs, modify them and export them to other systems for additional processing (such as design analysis). Designs may also be plotted, and GDSII tapes can be produced. The Mask Design System includes standard interfaces and standard libraries.</p>	<p>The Silicon Design System provides automated custom IC design, combining the power of Valid's IC design tools with the Concorde silicon compiler. The Silicon Designer is equipped with all of the high power software necessary for silicon compilation, including logic entry and simulation, artwork generation, symbolic editing and automatic routing.</p> <p>With the Silicon Design System, IC engineers can quickly and efficiently create sections of layout to mix with hand-crafted designs, or automatically create an entire IC prototype. Systems designers can now implement designs in silicon using more flexible and higher level functions than are available with either gate arrays or standard cells.</p> <p>The Silicon Design System contains a wide variety of flexible compiler modules which allow designers to efficiently control the design process. The correct-by-construction feature of the compiler modules is maintained by both interactive and automatic routers.</p>	<p>Some databases created with this software may be ported to larger mainframe machines, permitting further processing under other software systems. Depending upon the configuration of user's overall system and scope of projects, additional hardware may be required. Software can be networked.</p>

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# IC MASTER

DESIGN AUTOMATION—Workstations			
Generic Function	Software/Hardware Tool Name		
Workstation Design Tool Names (Cont'd)			
Source Workstation	Vamp Idea Station	Vectron Graphics Distributed Design Station	Vectron Graphics Personal Design Station
FOR DETAILED DATA SEE:			
Tool residence	APPLE	DEC VAX, DEC MICROVAX	IBM PC/XT/AT
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	EDSC AnalogSIM LogicSIM	Schematic Entry	Schematic Entry
Physical layout Circuit board Gate array Standard cell Full custom		DNA 2000	DNA 2000
Programmable logic device devel.			
Silicon compilation			
IC layout verification			
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system			
Support Documentation software Mechanical CAD/CAM	MacDraw, MacWrite 3-D MiniCAD		
Description	Some databases created with this software may be ported to larger mainframe machines, permitting further processing under other software systems. Depending upon the configuration of user's overall system and scope of projects, additional hardware may be required. Software can be networked.	The DNA 2000 software package can run on any VAX equipment. The software is the same for each system.	The DNA 2000 software package runs on Futurenet's IBM PC/XT or AT. The software is the same for each system.

DESIGN AUTOMATION



**DESIGN AUTOMATION—Workstations****Software/Hardware Tool Name****Workstation Design Tool Names (Cont'd)**

Vectron Graphics Stand Alone Design Station	VIA Systems BuildingBLOCKS	Viewlogic Systems Workview 1.2	Visionics EE Designer
APOLLO, MASSCOMP	APOLLO, DEC MICROVAX, SUN	IBM PC/XT/AT	IBM PC/XT/AT
Schematic Entry	Circuit Tool HSPICE CADAT (HHB Systems) CADAT (HHB Systems)	Viewdraw PSPICE Viewsim Viewsim PFG	
DNA 2000	BuildingBLOCKS ChipTool		
	DRACULA II (ECAD, Inc.)		
		Viewdoc	
The DNA 2000 software package runs on hardware from Apollo and Masscomp. Both workstations are based on the Motorola 68000 systems. The software is the same for each system.	VIA's BuildingBLOCKS Design System is a complete set of design tools for the development and layout of integrated circuits. By combining schematic capture, simulation, interactive editing, automated placement and routing, verification and data preparation, BuildingBLOCKS provides a flexible open ended design environment that supports current as well as future design requirements. All software modules are available separately on industry standard workstations.	Along with improvement to existing facilities, tools have been added to more tightly link Workview with other CAE/CAD environments. Also, Workview's simulation and symbol libraries include a number of new components. Enhanced plotting and printing capabilities have been added to Viewdraw, the drawing editor, Viewwave, the waveform processor, and Viewdoc, the document processor. Improvements include strip plotting, multi-sheet plotting, improved document output and higher-density fonts. Viewdraw's functionality has been enhanced with several user-selectable routing modes to make it easier for users to connect components. Viewwave's improvements include arithmetic and logical operations on waveforms which make it easier for users to extract information from waveforms generated by Viewsim, the Workview logic simulator, PSPICE and SILOS. Viewsim now contains 2,000 simulation models and symbols.	EE Designer is an integrated CAE/CAD/CAM system that runs on the IBM PC XT and AT and compatibles. EE Designer includes schematic drawing, schematic capture, netlist extraction, logic simulation, PC layout, design rule verification and post-processing including pen plotter and photo-plotter outputs, drill tape generation and bill of materials preparation.

## DESIGN AUTOMATION—Workstations

Generic Function		Software/Hardware Tool Name	
Workstation Design Tool Names (Cont'd)			
Source	VLSI Technology	Wintek	XCAT
Workstation	VTITools	Electronic CAD Software Tools	MX/MXT/HSE Logic/Fault Accel.
FOR DETAILED DATA SEE:	page 4665	page 4674	
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN	IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT
Front end design Schematic entry Circuit simulation Logic simulation Timing verification Fault simulation	VTIschematic VTIspice VTIsim VTIsim	HiWIRE	
Physical layout Circuit board Gate array Standard cell Full custom	(performed internally) VTIlogicComp VTIcustom	smARTWORK	
Programmable logic device devel.			
Silicon compilation	VTicellLib		
IC layout verification	VTIverify		
Hardware tools Physical modeling Circuit simulation accelerator Logic simulation accelerator Fault simulation accelerator Integrated test system			MX, MXT, and HSE Series MX, MXT Series
Support Documentation software Mechanical CAD/CAM			
Description		<p>Wintek offers two low-cost computer-aided-design software packages to speed the work of electrical engineers and technicians. Both packages run on a standard IBM Personal Computer. HiWIRE allows the quick creation and revision of schematic diagrams on the screen of the PC. Finished schematics can be drawn by a pen plotter or printed by a dot-matrix printer. The package includes an extensive library of TTL, CMOS, ECL, ladder, microcomputer, and discrete components, plus netlist and bill of material utilities.</p> <p>smARTWORK lets the design engineer create, revise, and produce printed-circuit-board artwork using the IBM PC. The interactive router finds the shortest route between two electrical networks, speeding the layout process. smARTWORK also includes an autorouter. Production-quality 2X artwork can be produced using a pen-and-ink plotter; prototype-quality 2X artwork and checkplots can be produced using a dot-matrix printer. Pad-master and soldermask plots are created automatically.</p> <p>Each package is priced at \$895 and is sold with a 30-day money-back guarantee.</p>	<p>XCAT's series of hardware accelerator systems include the MX-50, MX-100, MXT-50, MXT-100, MXT-400, HSE-400 and HSE-1000. XCAT's logic accelerator systems have simulation speeds up to 2000 times faster than software simulators running on a VAX 11/780 and fault simulations up to 100 times faster. With prices ranging from \$49,000 to \$450,000 XCAT intends to fill the need for a high performance, integrated hardware/software accelerator system at an affordable price. XCAT's systems are interactive, multi-user and have interface capabilities with several popular schematic entry systems such as Mentor and FutureNet as well as netlist inputs from TEGAS and EDIF. XCAT provides a high-speed parallel interface to VAX, IBM PC XT/AT, Apollo and other popular workstations. XCAT's hierarchical incremental compiler has the ability to compile large networks in just a few minutes.</p>



DESIGN AUTOMATION—Workstations			
Software/Hardware Tool Name			
Workstation Design Tool Names (Cont'd)			
Xerox Expert	Zuken C2000	ZyMOS ZyP-AT	
XEROX	HEWLETT-PACKARD	IBM PC/XT/AT	
Expert Schematic (see Design Tool Interfaces) Expert Logic Simulator Expert Timing Verifier (see Design Tool Interfaces)	ESI, ESIII Spice HILO-3 (see Genrad) HILO-3 (see Genrad) HILO-3 (see Genrad)	Case CT2000  ZyPSIM-AT ZyPSIM-AT	
Expert PCB (see Design Tool Interfaces) (see Design Tool Interfaces)	C2000		
Intel, ABEL			
(see Design Tool Interfaces) (see Design Tool Interfaces) (see Design Tool Interfaces)			
Xerox Viewpoint Expert Drafting			
Expert is an integrated system, which provides tools for Electronic design and verification, printed circuit board design, mechanical design, and technical documentation and publications. With true multitasking, multiwindow user interface, optical mouse, pop-up menus and accelerator keys, this system runs on either the Xerox 8014 B&W W/S, the Xerox 6080 Color W/S, or the Xerox 6085 B&W W/S.		ZyP-AT is the ZyMOS design environment on the IBM PC/AT or compatible. ZyP-AT is the shell through which the design process is managed. No knowledge of DOS is required of the user.	

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Schematic Capture			
Source	Aida	Analog Design Tools	Analog Design Tools
Tool Name	Aida Design Creation System	AnalogWorkbench Circuit Editor	PC Workbench Circuit Editor
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, SUN	APOLLO, HEWLETT-PACKARD, IBM PC/XT/AT, SUN	APOLLO, HEWLETT-PACKARD, IBM PC/XT/AT, SUN
Schematic database consists of: Graphics symbols Simulation model data Physical layout data	X X	X X	X X
Netlist compilation As symbols are entered Batch mode after capture	X	X	X
Electrical rules check Batch mode On-line (Interactive)	X	X	X
Rules checked Connectivity Open nets Unassigned pins Multiple naming of nets Connections between sheets Fanout User-defined rules	X X X X X X X	X X X	X X X
Database accessibility Procedural interface EDIF interfaces	X	X	X
Color display	X	X	X
ASIC libraries supported	LSI Logic, Toshiba, ICS. Contact AIDA for others.	Ferranti Interdesign, Micro Linear, MCE Semiconductors.	Ferranti Interdesign, Micro Linear and MCE Semiconductors.
Description	The Aida Design Creation System streamlines design capture by providing intelligent symbol creation, library development and schematic capture capabilities. This system includes the Schematic Design Editor (SDE), the Aida Design Language (ADL), the Librarian (OLIB), the Automatic Logic Documentor (ALD), and a Graphics Symbol Editor (SYMED). Simulation connectivity files are concurrently edited with the graphics to improve design-simulation cycles per day.	The Analog Workbench Circuit Editor has an easy-to-use intuitive user interface for the design of analog circuits. Using a mouse, the circuit is drawn or edited by placing components, adding semiconductors and assigning values. Supplies, sources, and function blocks can be added, and all components connected with lines. Editing is an electronic cut-and-paste procedure. Once the circuit is drawn, parameters and values can be displayed and changed. Variable expressions can be assigned. Reference designators and node numbers are automatically added.	The PC Workbench Circuit Editor has an easy-to-use intuitive user interface for the design of analog circuits. Using a mouse, the circuit is drawn or edited by placing components, adding semiconductors and assigning values. Supplies, sources, function blocks can be added, and all components connected with lines. Editing is an electronic cut-and-paste procedure. Once the circuit is drawn, parameters and values can be displayed and changed. Variable expressions can be assigned. Reference designators and node numbers are automatically added.



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Front End Design Tools—Schematic Capture (Cont'd)			
Applicon Design Capture	Argus Software McNet	AT&T AT&T OMNIPRO PC	B&C Microsystems SCH/DE
			IBM PC/XT/AT
			X
			X
			X
			X X X X
			X
Design Capture provides a comprehensive set of tools for creating, analyzing, and documenting an electronic design. The tools are applicable to a wide variety of electronic designs using digital, analog, or mixed logic. Design hierarchy can be captured, and the design can range from one to many sheets. At the heart of the package is a comprehensive set of electronic component catalogs and generic and discrete symbols.	Argus Software's McNET schematic capture package runs on the Apple Macintosh. McNET delivers a complete CAE digital schematic capture workstation which includes schematic entry, net list and parts list generator, and a component library builder. McNET is user oriented. Digital circuit designers are able to spend more time designing rather than learning about the system. McNET eliminates many tedious repetitive tasks and supports commands such as copy, move, rubberbanding, select-by-area, view-by-area, and undo/redo. Functions on McNET are user friendly and highly automated. The bus feature in McNET features auto bus-rip, auto-bus ripper numberer, auto bus width tracker, and auto bus name tracker. Net list and parts list generator allows the design to talk to other software such as simulator, wire wrap software, and printed circuit board software.	AT&T's OMNIPRO PC is a low-cost PC-based schematic capture package. A compliment to the Omniline of CAD tools, AT&T OMNIPRO PC software provides the engineer with schematic editing, symbol libraries and editing, design analysis, and formatted output. The software runs under MS-DOS in standard AT&T PC 6300 and IBM PC/AT Color Personal Computers.	Running on the IBM XT-AT and compatibles, the SCH Design package from B&C Microsystems is a customized schematic capture program for AutoDESK's AutoCAD system. The environment was designed having as guidelines the industry standard FutureNet DASH-2 editor. A comprehensive library of almost 1,200 parts is included. These include TTL, ECL, CMOS, Intel, Motorola, memory and discrete. Each part can be inserted from the menu with predefined parameters, or can be arbitrarily magnified, rotated, etc. The menu also offers a complete set of electronic primitives which permit the user to create his own symbols with maximum ease. These include all 2, 3 and 4 input gates in positive and negative logic, symbol stubs, boxes, resistors, capacitors, bridges, zeners, transistors, LEDs, FETs, UJTs, etc. On-line help is available for all the custom library entries. Following the FutureNet convention, the alphanumeric text is assigned up to 35 different attributes (layers) which permit PINLIST, NETLIST and PARTLIST generation. The layer assignment is transparent for the user being done completely from the menu.  A three-button mouse is conveniently reconfigured for pointing, line routing and inserting of interconnecting DOTS. The PINLIST and NETLIST programs generate FutureNet compatible files and are included in the package.

Bold face indicates data is provided in the page noted

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Schematic Capture (Cont'd)			
Source	Bishop Graphics	Cadam	Cadnetix
Tool Name	Pathfinder	CADEX	Schematic Editor
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	IBM MAINFRAME/MINI	SUN, MS-DOS PCs, Cadnetix 68020-based worksta
Schematic database consists of:			
Graphics symbols	X	X	X
Simulation model data			X
Physical layout data	X	X	X
Netlist compilation			
As symbols are entered			
Batch mode after capture	X	X	X
Electrical rules check			
Batch mode		X	X
On-line (Interactive)			
Rules checked			
Connectivity		X	X
Open nets		X	X
Unassigned pins		X	X
Multiple naming of nets		X	X
Connections between sheets		X	X
Fanout			
User-defined rules			
Database accessibility			
Procedural interface	X	X	X
EDIF interfaces			X
Color display	X	X	X
ASIC libraries supported			NCR, LSI Logic, Toshiba, TI, VLSI Technology, Thomson-Mostek.
Description	A powerful CAE/CAD software package for PCB design and layout (end-to-end solution) including schematic capture and an optional autorouter with mainframe performance (32-bit) featuring unlimited layers, top/bottom views for SMT, Gerber output, fineline routing, mirroring, sophisticated routing algorithms for less than \$5000.		
	The CADEX module automatically extracts a net list from a schematic or wiring diagram drawn on the CADAM system. In creating the editable net list, CADEX includes the signal name, reference designator, pin number and part number-- and automatically adds signal number and categories used in automatic placement and routing routines. The ERROR MODEL feature visually displays the error report generated by CADEX for the designer. It circles each error on the screen and at the same time displays a message identifying the type of error. Interactive aids permit quick location and resolution of errors. Interactive capabilities include: automated solder dot, signal display, and interactive library retrieval. A Starter Library of schematic symbols is also included.		



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Front End Design Tools—Schematic Capture (Cont'd)**

Calay Systems ZX1000	Calma TEGATE	Calos Calos 6000	Case Technology CT2000
IBM PC/XT/AT	APOLLO	IBM PC/XT/AT, Compaq, TI Business-Pro, Televideo 286	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN
X	X X	X X X	X X
X	X	X	X
X	X X	X	X
X X X X X	X X X X X X X	X X X X X	X X X X X X X
X	X	X	X
X	X	X	X
	SMOS 2u DLM CMOS arrays, Harris 3u SLM CMOS cells, GE 2u DLM CMOS arrays, GE 1. 25u DLM CMOS cells, RCA 1.25u DLM CMOS/SOS cells, RCA 3u DLM CMOS ar- rays, AMI 3u DLM CMOS arrays, Toshiba		LSI Logic, Zymos, Micro Linear, Thomson Mostek.
Calay's ZX1000 is a schematic editor that runs on IBM PC/AT compatibles and provides capabilities for engineering functions related to physical design including estimates for electrical power, part cost, and board component area. The ZX1000 features a large component library of more than 5000 components, support for both hierarchical and flat designs, fast interactive editing tools, electrical error checking, and command macro functions. Users can graphically enter designs and perform the functions of design capture as well as interface to simulation and printed circuit board design tools used to develop and create electronic circuits. The ZX1000 schematic capture system interfaces directly with Calay's Design Automation Series PCB CAD workstations and offers full forward and backward annotation capability.	The TEGATE schematic capture system gives the designer a method for creating, documenting and analyzing integrated circuit and printed circuit board designs. TEGATE is an interactive program applicable to a variety of design methods. An integral part of TEGATE is a database that describes the captured schematic. This database is the single source of information for simulation, layout, and other user-supplied software. TEGATE's two-way interface allows results from these systems to be back-annotated to the schematic. TEGATE provides facilities for on-line, real-time logic design in a color-graphics environment. Features include multiple symbol libraries, autorouting of interconnects, and support for bus structures, trunks and matrix operations. Advanced analysis commands maximize engineering time by ensuring the electrical integrity of the design.	This second generation schematic capture package operates on the IBM PC XT/AT, and the TI Business Professional. Both the original MC68000 based system and the new IBM and TI versions are completely database and operationally compatible. Calos 6000 electronic engineering workstations provide schematic capture and interfaces to a variety of design automation tools including simulators such as HHB Softron's PC CADAT system, auto insertion systems, automatic wire wrap systems, and PCB CAD systems.	

## DESIGN AUTOMATION—Design Tools

Generic Function	Design Tool Capability		
Front End Design Tools—Schematic Capture (Cont'd)			
Source	Case Technology	Clarity Systems	Computervision
Tool Name	Vanguard Stellar System	StrucSet	Schematic Design
FOR DETAILED DATA SEE:			
Tool residence	AT&T, DEC VAX, DEC MICROVAX, IBM PC/XT/ AT, NEC PC, SUN, Silicon Graphics	APOLLO	Computervision
Schematic database consists of:			
Graphics symbols	X	X	X
Simulation model data	X	X	X
Physical layout data	X	X	X
Netlist compilation			
As symbols are entered		X	
Batch mode after capture	X	X	X
Electrical rules check			
Batch mode	X	X	
On-line (Interactive)	X	X	X
Rules checked			
Connectivity	X	X	X
Open nets	X	X	X
Unassigned pins	X		X
Multiple naming of nets	X	X	
Connections between sheets	X		X
Fanout			
User-defined rules	X		
Database accessibility			
Procedural interface	X	X	X
EDIF interfaces	X	X	
Color display	X	X	X
ASIC libraries supported	LSI Logic, Fairchild, Zymos, Siliconix, Exar, Microlinear		
Description	Pointer based memory system for efficient editing and storage, text associated with signals, user configurable drafting standards, interactive rubberbanding, remote snap to capability for signals and components, standard library of 3000 parts: digital and analog, powerful component editor with interactive commands for circles, arcs and lines, orthogonality enforced in drawing editor.	StrucSet is an integrated set of tools used for structural and schematic design of hierarchical blocks at the architectural, functional, logic, gate, and transistor levels. It can be used in top-down design where a system block at the topmost level is decomposed into instances with definitions of their I/O ports and nets. This decomposition continues to the lowest (leaf cell) level where the internal elements of a block are implemented using primitive gates and transistors.  Conversely, the designer can start with primitive elements and standard pre-defined blocks and work bottom-up to construct the schematic for an entire system or chip. StrucSet ensures the correctness of the design by enforcing SuperSet's logical syntaxes. SYMBAD, StrucSet's symbol editor, allows graphic creation of user-defined symbols which can then be used to construct hierarchical schematics using the schematic editor, SCHEDI. The schematic's connectivity is updated dynamically in SuperSet's integrated database and is immediately available to all other SuperSet modules. This enables such features as direct simulation without netlist extraction in SimuSet, driven mode and kit mode in TopSet's topological editor, and selection across views.	Schematic Design is a UNIX-based software application program developed for CADDStation, Computervision's 32-bit workstation. It provides tools for the front-end of the PCB design process-- schematic capture and simulation. While Schematic Design performs schematic capture functions, transparent interfaces to HILO-3 and SPICE ensure comprehensive digital and analog simulation.  Schematic Design features an icon-based user interface for ease of use; a symbol editor with split screen capability allowing for the simultaneous viewing of different portions of the schematic to ensure connectivity when wiring across large areas. Schematic Design's hierarchical design structure allows you to represent your design at the systems architecture, functional gate, or device level. Netlists are easily transferred to Computervision's Autoboard PCB layout package.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Schematic Capture (Cont'd)

Control Data ED-Schematics	Control Data MIDAS	Daisy Systems ACE/ACE PI	Data General TEO/Electronics Design System
IBM PC/XT/AT	APOLLO, Daisy	IBM PC/XT/AT, Daisy Personal Logician 386/ Logician 386	DATA GENERAL
X X X	X X	X X X	X X X
X	X	X	X
X X		X X	X
X X X X X X X	X X X X X X	X X X X X	X X X X X X
X X	X	X	X X
X	X	X	X
LSI Logic, Micro Linear, Motorola, VTI, VTC, Gould Semiconductors.	VTC, National Semiconductor, Honeywell, Rock- well International.	150 ASIC libraries from 70 ASIC vendors in- cluding: Fujitsu, LSI, VTI, TI, Intel, Motorola, GE/RCA, NEC, Matsushita, Fairchild, NCR, ZyMOS, Gould/AMI, Harris, AMCC, Nation- al, IMP, Xilinx, Ferranti, Philips, Plessey.	Fujitsu Microelectronics.
The Electronics Designer schematic entry package (ED-SCHEMATICS), consists of Schematic and Component Editors. It offers advanced features previously found only in higher-priced workstations including: A split-screen display, three- cursor system, group commands, locator icons, intelligent rubber- banding, automatic component naming and hierarchical design.	Modular Integrated Design Automa- tion System.	Daisy's ACE is an advanced sche- matic editor with icon-based, graphics interface. The new user interface lets design engineers easily create and edit schematics by using a mouse to point to com- mand icons and schematic ob- jects. To use ACE, designers select such command icons as "wire", "move" or "delete", which are pic- torial representations of their function. Instead of laboring through a hierarchical menu struc- ture to execute a command, the user simply points to an icon and clicks the mouse. The intuitive in- terface virtually eliminates the typ- ical learning curve and allows schematics to be entered and ed- ited more quickly than with older user-interface methodologies.  The ACE Procedural Interface, ACE PI, is a set of Pascal procedure calls that allows data to be output from and input to the Daisy sche- matic data base. ACE PI allows us- ers to transport foreign schemat- ics into ACE, gain access to ACE schematics in later design pro- cesses, and create custom soft- ware that checks or modifies the design.	The TEO/Electronics Design System offers schematic capture, interac- tive error and design rule check- ing, and integrated documenta- tion, to support the design of LSI/ VLSI circuits, gate arrays, and printed circuit boards. The system features an easy-to-learn-and-use, highly interactive user interface that includes pop-up menus, icons, and multiple windows.  Circuit designs are represented by an intelligent, object-oriented database. TEO/Electronics offers a single integrated database for schematic capture, simulation and documentation. This eliminates the need to extract net lists, sav- ing time and easing data manage- ment. Software tools provide ac- cess to the database for integra- tion of complementary third-party applications. The engineer models with intelligent components that contain all relevant electrical infor- mation, which makes possible real-time error checking. TEO/ Electronics is part of Data Gener- al's TEO environment that pro- vides access to a set of integrated productivity tools.

**DESIGN AUTOMATION—Design Tools**

Generic Function

Design Tool Capability

**Front End Design Tools—Schematic Capture (Cont'd)**

Source	Design Computation	ES2/US2	EXAR
Tool Name	DRAFTSMAN-EE	SOLO 1000/SOLO 1200	SDS/SL2000 (see Silvar-Lisco)
FOR DETAILED DATA SEE:			page 4222
Tool residence	AT&T, IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, VAXstation 2000	APOLLO, IBM PC/XT/AT, IBM System 2
Schematic database consists of:			
Graphics symbols	X	X	X
Simulation model data		X	X
Physical layout data	X	X	
Netlist compilation			
As symbols are entered		X	
Batch mode after capture	X	X	X
Electrical rules check			
Batch mode	X	X	
On-line (Interactive)		X	
Rules checked			
Connectivity	X	X	X
Open nets		X	X
Unassigned pins	X	X	X
Multiple naming of nets		X	X
Connections between sheets	X	X	
Fanout		X	
User-defined rules		X	
Database accessibility			
Procedural interface	X	X	X
EDIF interfaces	X	X	
Color display	X	X	X
ASIC libraries supported		European Silicon Structures, Texas Instruments, Philips, AMI	FLEXAR soft macro library from EXAR.
Description	<p>DRAFTSMAN-EE is a powerful, feature-packed, graphics editor with excellent functional capability. Built from the ground up specifically for electrical engineers, it allows rapid entry and modification of graphical data, such as schematics and printed circuit layouts. DRAFTSMAN-EE is designed to handle all of the graphical needs of most EEs. Many I/O devices are supported including the IBM Enhanced Graphics Adapter, the Hercules graphics card, Hewlett-Packard plotters, Houston Instruments plotters, Epson dot matrix printers, the Microsoft mouse, and Lotus/Intel/Microsoft EMS memory boards. DRAFTSMAN-EE imposed practically no limits on drawing size or complexity. Drawings can be virtually any size and can contain over 32,000 data elements. Components library, Parts List utility, and Bill of Materials utility are included.</p> <p>The SOLO Schematic Package is an integral part of the SOLO System. It is menu-driven and is used with a mouse. The package works in a hierarchical fashion, either top-down or bottom-up. Designs may be entered by either using conventional schematics, or by specifying blocks through Hardware Description Language.</p> <p>SDS/SL2000 is a general purpose schematic capture system used as part of an integrated development system called FIDS (Flexar Integrated Development System).</p>		



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Schematic Capture (Cont'd)

Fairchild FAIRCAD	Ferranti Interdesign Silicon Design Sys. ULA LOGCAP	FutureNet (Data I/O) DASH-4 page 4651	Gould Semiconductor Division SCEPTRE III page 4244
DEC VAX, DEC MICROVAX, TEKTRONIX, Valid, Daisy, Mentor, Tek CAE, FutureNet	DEC VAX, DEC MICROVAX	IBM PC/XT/AT	IBM PC/XT/AT
X X	X X X	X X	X X
X	X X	X	X
X	X X	X	X
X X X X X X X	X X X X X X X	X X X X X X X	X X X X X X X
X	X X	X X	X
X	X	X	X
Fairchild ECL and CMOS macro libraries.	Ferranti Interdesign ULA.	Motorola, Gould, National, Fairchild.	Gould Semiconductor Division's CMOS 2- micron gate array and standard cell li- braries.
FAIRCAD schematic capture simplifies the entering and editing of a semicustom design. FAIRCAD programs are completely menu-driven and extensive on-line help listings are accessed by simply typing "h" followed by a carriage return. Logic components are accessed from the macro library of the chosen technology and, with a single keystroke, positioned within the design. Facilities such as COMPONENT MOVE and ALIGN allow the designer to quickly organize and structure the design. Interconnection of components is also quick using connection rubberbanding, which makes line segments visible during the actual connection procedure; visible connections are "stretched" between the entry points with the system crosshairs. WINDOW commands let the designer edit up to four different symbols, schematics, or windows of the same schematic or symbol simultaneously. Names, text, components, and pins can be aligned horizontally or vertically using FAIRCAD's alignment feature.	ULA LOGCAP covers capture from ULA libraries of primitive and complex circuit elements. Graphics are provided by using the DEC MicroVAX or high resolution color graphics terminals ported to VAX. The software enables capture, editing and compilation producing the Ferranti Logic Description Language net list.	The DASH schematic designer is claimed to be the first design package written specifically for the personal computer. DASH automatically performs all the tedious and time-consuming drafting and documentation chores connected with schematic design. DASH uses comprehensive guided sessions to step the user through the design process, and offers on-line help and full-screen menus to aid infrequent or casual users. DASH can be run either from the keyboard or from a mouse, and features a high-speed graphics editor with sophisticated drawing features that are equal to the demands of the most advanced users. Because DASH was first on the PC, DASH users have immediate access to dozens of gate-array foundries and hundreds of engineering service bureaus. In addition, proven DASHtranslators are available for virtually every CAD system on the market.	SCEPTRE III is a software application package that works on personal computers which enables engineers to perform schematic capture, logic simulation, placement and routing, layout verification, timing analysis, netlist generation and utility programs that compile netlist data into the system's internal database format.  SCEPTRE III has been developed for Gould as part of its workstation design kit for both gate array and standard cell circuits. The SCEPTRE software is delivered with GOULD's extensive library of 2- and 3- micron CMOS cells.

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Schematic Capture (Cont'd)			
Source	GT Systems	Harris Semiconductor	Hewlett-Packard
Tool Name	AutoNET	Harris/SDA Schematic Capture	Design Capture System
FOR DETAILED DATA SEE:		page 4246	
Tool residence		APOLLO, DEC MICROVAX, MASSCOMP, SUN	HEWLETT-PACKARD
Schematic database consists of:			
Graphics symbols		X	X
Simulation model data		X	X
Physical layout data		X	X
Netlist compilation			
As symbols are entered			X
Batch mode after capture		X	
Electrical rules check			
Batch mode		X	X
On-line (Interactive)		X	X
Rules checked			
Connectivity		X	X
Open nets		X	X
Unassigned pins		X	X
Multiple naming of nets		X	X
Connections between sheets		X	X
Fanout		X	X
User-defined rules			X
Database accessibility			
Procedural interface		X	X
EDIF interfaces		X	X
Color display		X	X
ASIC libraries supported		Harris Semiconductor	Fujitsu, NEC, Toshiba, TI.
Description	AutoNET is an enhancement to the popular AutoCAD program. AutoNET provides schematic capture and net list generation for subsequent PCB layout using AutoCAD.	The SDA schematic capture system is a completely hierarchical structure which supports user configurable, multiple windows and cross window editing and viewing commands. The system supports both color and B&W monitors with full mouse functionality. Harris has extended the system with up to 16K RAM and up to 64K ROM configurable modules. Further extensions include iconic menus supporting a very extensive standard cell design library for digital CMOS, as well as libraries supporting analog bipolar design, and digital gallium arsenide design. The system supports electrical rules checking at any point in the capture process.	The Hewlett-Packard Design Capture System software provides an easy-to-learn design environment that supports not only schematic capture, but also documentation, design database access, and interfaces to the most popular H-P printers and plotters.



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Front End Design Tools—Schematic Capture (Cont'd)**

IBM CIEDS/Design Capture	Intergraph Hierarchical Schematic Design	Kontron KAD Editor	LSI Logic LSED (LSI Logic Schematic Ed.) page 4653
IBM MAINFRAME/MINI, IBM PC/XT/AT, IBM RT PC, IBM PS/2	IBM PC/XT/AT, Intergraph InterPro, InterAct	IBM PC/XT/AT, Kontron-AT, 1280 x 1024 graphic display	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PYRAMID, SUN, Am-dahl
X X	X X	X X X	X X
X	X	X	X
X	X	X X	X
X X X X X	X  X  X	X X X X X	X X X X X X
X	X	X X	X
X	X	X	X
	Fairchild, Fujitsu, Hitachi, Raytheon, S-MOS, Thomson-Mostek, VTI, Waferscale.		LSI Logic complete ASIC product line and system design extensions.
Computer-Integrated Electrical Design Series (CIEDS)/Design Capture is the front-end schematic entry tool for IBM's Electronic Design Automation family of products. It is an interactive graphics-based product that operates on all three of IBM's "Engineering Workstation" platforms: PC/AT, PS/2, RT PC, 5080 Graphics Workstation attached to the System/370 family of processors. CIEDS offers the following: integrated database; hierarchical design; consistent user-interface across hardware platforms; database utility routines; netlist extraction; support of Structured Design Language (SDL); and Engineering Access Routines (EARS) which supports access into and out of the CIEDS database in user-defined format.	The HSD (Hierarchical Schematic Design) software supports fully hierarchical design and allows a single database to contain design, analysis, implementation, and documentation. A powerful on-line electrical rules checker and a graphical waveform editor integrate the analysis software with Genrad's HILO-3 logic simulator. This sophisticated front-end engineering system, with its strong emphasis on analysis and correct-by-construction design, can be directly linked to software supporting a range of design options: IC, PCB, hybrid, multiwire- allowing a firm to choose from a variety of implementation technologies.	Kontron's interactive graphics editor with schematic capture, structured design, netlist extractor and linker, airline generator, ground plane manager, back annotation, component libraries, including functional pin/gate attributes, links to logic simulation packages, parts list generator, netlist text editor software.	LSED is LSI Logic's advanced schematic and waveform editor and display. LDS integration, speed, and ease of use differentiate LSED from other schematic capture packages.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Schematic Capture (Cont'd)			
Source	Micro Linear	National Semiconductor	Omation
Tool Name	Linear CAD II	Design Automation System	SCHEMA
FOR DETAILED DATA SEE:		page 4294	
Tool residence	IBM PC/XT/AT	IBM MAINFRAME/MINI, IBM PC/XT/AT, Daisy, Mentor, FutureNet workstations	IBM PC/XT/AT
Schematic database consists of: Graphics symbols Simulation model data Physical layout data	X X	X X	X
Netlist compilation As symbols are entered Batch mode after capture	X	X	X
Electrical rules check Batch mode On-line (Interactive)	X	X	X
Rules checked Connectivity Open nets Unassigned pins Multiple naming of nets Connections between sheets Fanout User-defined rules	X X X X X X X	X X X X X X X	X X X X X X X
Database accessibility Procedural interface EDIF interfaces	X	X	X X
Color display		X	X
ASIC libraries supported	Micro Linear- Linear Bipolar Arrays.	National Semiconductor.	
Description		For the design of National Semiconductor gate arrays and standard cells. The symbol library consists of more than 200 core and I/O macros which are common to both gate arrays and standard cells. Beside these, the library contains a number of LSI/VLSI functions offered in standard cells only, like: large single- and dual-port RAMs, PLAs, 82C50 UART, 2901 bit-slice processor, 8- and 16-bit microcontrollers, EEPROMs, ROMs, A/D, D/A and other analog functions.	SCHEMA is a complete, integrated schematic capture software package for IBM personal computers and compatibles. SCHEMA lets engineering professionals draw schematics and other technical drawings using the IBM PC on their desk. SCHEMA automatically generates related design documentation such as wire/net/pin lists, bills of materials, design rule checks, etc. SCHEMA sells for \$495 and comes complete with a large component database, printer and plotter drivers, and a comprehensive user's manual.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Schematic Capture (Cont'd)

Optima Technology OPTIMATE Design	P-CAD PC-CAPS	Racal-Redac VISULA Design Entry	Royal Digital Systems AutoMate Schematic Capture
APOLLO, DEC VAX, DEC MICROVAX	IBM PC/XT/AT	IBM PC/XT/AT	CONTROL DATA, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, PRIME, SUN
X X	X X	X X	X X X
X	X	X	X
X X	X	X X	X
X X X X X	X  X	X X X X X X X	X X X X X X X
X		X	X
X	X	X	X
	G.E., Gould Semi, Laserpath, LSI Logic, Motorola, RCA, Texas Instruments, Universal Semi, Waferscale Integration.		LSI Logic, Micro Linear, ZyMOS, Thomson-Mostek and others.
OPTIMATE Design is a highly interactive schematic capture system that allows the designer to create a multisheet (up to 50 pages) electronic schematic and automatically extract a net list. OPTIMATE includes extensive component and function libraries that designers can add to or change. Automatic gate and pin assignment, automatic signal bussing, automatic "Z" line interconnections, and full labeling help streamline and speed schematic entry. Back annotation provides up-to-date and accurate schematic documentation that matches the PCB layout exactly. Changes in the schematic result in automatic updating of placement and routing. The user may choose between a table or on-screen menus.	By implementing new data management techniques, P-CAD has increased drawing speeds on large schematics up to 50%. Automatic layer switching lets users automatically place design information on the appropriate layer for more acceptable and segmentable data. System automatically adds solder dots at the "T" junctions in the size and shape specified by the user. Coupled with this new software release, P-CAD's component library now has over 1700 parts.	VISULA DESIGN ENTRY, the front end of the Visula software family is an intelligent design system for electronic products. Engineers can carry out individual design assignments on the IBM PC/AT using Visula Design Entry, while maintaining full compatibility across Visula's entire software product family, and complete system integration. VISULA DESIGN ENTRY is more than schematic entry; it is also an electronic decision making tool. Key features are: 1) Intelligent on-line electronic rules checking, maintaining true electrical connectivity by automatically generating the design database. 2) A fully integrated customizable library, capitalizing on Visula's powerful relational database. 3) Common design data, thus eliminating time consuming data retranslations and costly error introductions between applications. 4) Reports on design data at any time during the design process. 5) Design to simulation- VISULA DESIGN ENTRY is fully integrated with Visula's CADAT 5 logic and fault simulator, and Visula's Waveform Analyzer giving the designer the full Visula CAE product set for the IBM PC/AT.	The AutoMate Schematic Design system provides powerful tools for both creating and editing schematics. With many automated capabilities, the Schematic Editor responds intelligently to commands and allows the designer to configure key parameters. To provide maximum versatility, the AutoMate Schematic System runs on several industry-standard hardware platforms, including the IBM PC, the DEC MicroVAX and VAX. On each of the platforms, the system is virtually identical.

**DESIGN AUTOMATION—Design Tools**

Generic Function		Design Tool Capability	
Front End Design Tools—Schematic Capture (Cont'd)			
Source	Scientific Calculations	SDA Systems	Silicon Compiler Systems
Tool Name	SCIDESIGN	Schematic Editor	Generator Development Tools
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT, IBM PC compatibles	APOLLO, DEC VAX, DEC MICROVAX, MAS-SCOMP, SUN	APOLLO, DEC MICROVAX, SUN
Schematic database consists of:			
Graphics symbols	X	X	X
Simulation model data	X	X	X
Physical layout data		X	X
Netlist compilation			
As symbols are entered			X
Batch mode after capture	X	X	
Electrical rules check			
Batch mode	X	X	X
On-line (Interactive)			X
Rules checked			
Connectivity	X	X	
Open nets	X	X	
Unassigned pins		X	
Multiple naming of nets	X	X	
Connections between sheets	X	X	
Fanout			
User-defined rules	X	X	
Database accessibility			
Procedural interface	X	X	X
EDIF interfaces	X	X	X
Color display	X	X	
ASIC libraries supported			
Description	<p>SCIDESIGN is an IBM Personal Computer based electronics design engineering tool. The product features an integrated schematic sheet editor, and optional circuit simulation package. It provides the engineer with the capability to generate schematic diagrams, perform design rule checks on the circuit, generate net lists and a user accessible ASCII file of all SCIDESIGN data, including graphics. Furthermore, those users of the SCISIM System are able to perform digital logic simulation on all or a portion of the circuit defined in SCIDESIGN.</p> <p>Included in SCIDESIGN Release 3.0 is the capability for the user to extract any SCIDESIGN data of interest, in a file structure of his own choosing, thus greatly reducing his dependence on an outside vendor for the supply and ongoing support of interfaces to other systems, whether commercially available or internally developed.</p>	<p>At the front end of the design process the schematic editor captures the connectivity and properties of the design. Plots for documentation, and netlists for interfacing to various simulators are created from the schematic database. Interaction with the simulators and layout tools of the system accelerates the design process; for example, the engineer can interactively define probes on the schematic for simulation. Colors are used to display the various design elements, and also to highlight design errors, and design rule violations.</p> <p>The editor supports hierarchical designs, by allowing for the symbolic and schematic representation of functional blocks, and editor commands dynamically traverse and display the design hierarchies. Multi-sheet schematics can be easily created and managed, and they can be nested in the hierarchy of other designs. The editor's use of multiple windows allows the simultaneous display and cross-editing between multiple views of multiple schematics. Finally, through user definable properties and netlist formats, the schematic database can be easily interfaced to other design analysis tools.</p>	<p>The Generator Development Tools (GDT) can be used by IC designers to create their own silicon compilers. The power of GDT is based on a new language, L, developed by SDL. Generators, produced using L, can accept parameters from a user and develop completely custom layouts. GDT can also be used by logic designers and system designers to create larger functional blocks or complete chips using their own or Silicon Design Labs' basic functions. GDT features a Macintosh-like user interface, on-line design rule checking and an integrated hierarchical mixed-mode functional/circuit/fault simulator. GDT also includes a complete standard cell library and automatic place and route tools as well as PLA generation tools.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Schematic Capture (Cont'd)

Tektronix CAE Systems Designer's Database (DDSC) page 4658	Teradyne DATAView	Trimeter Technologies Knowledge Consultant	Trimeter Technologies Logic Consultant
APOLLO, DEC VAX, DEC MICROVAX, TEK- TRONIX	IBM PC/XT/AT		APOLLO
X X	X X	X X	X X
X	X		X
X	X	X	
X X X X  X	X X X  X	X X X  X X	
X	X		
X  NEC, Fujitsu, LSI, TriQuint, Chesapeake Group, Fairchild, Plessey, Matra Harris, ES2, Mar- coni Electronic Devices (MED), Westing- house	X  AMCC, AMD, Motorola, Fujitsu, LSI Logic.	X  Mentor Graphics' Gen Lib, LSI Logic	X  Mentor Graphics. Gen Lib, LSI Logic
<p>Designer's Database Schematic Capture (DDSC) is the schematic capture package, as well as point of integration for all analysis tools, including third party and in-house tools. Design information is entered and retrieved from a single hierarchical database, which is transparently distributed around the Tektronix WorkSystem network. DDSC is mouse driven and menu oriented. Up to 24 user-configurable windows and menus may be on the screen. A command builder menu and pop-up menu provide rapid selection of commands and options. The "open-architecture" design features single-button interface for accessing tools and hierarchical back-annotation provides bi-directional data transfer. The powerful parameter scheme accommodates a wide variety of parametric information and allows compact format for data entry and storage.</p>	<p>DATAView is an integrated design program which runs on the IBM PC AT. Its mouse-driven, pop-up, look-ahead menu system provides a user interface which is consistent across a wide range of design activities: an engineer can use it to create and edit schematics; initiate simulation operations by the LASAR Version 6 simulation system; view waveform analyses and other simulation results; create documentation, and exchange electronic mail.</p> <p>Schematics created using DATAView are read directly on a page-by-page basis by LASAR to provide high-speed model compilation essential for fast simulation response times. LASAR's simulations are run on a VAX computer or on the DATAServer simulation server, and are accessed over Ethernet from the PC AT design station; thus, engineers have access to the large capacity and power of a mainframe for creating, simulating, and storing much larger designs than could be handled by the PC alone.</p>	<p>Trimeter's Knowledge Consultant is an expert system for graphically capturing ASIC logic design expertise. It allows you to incorporate your own design expertise into a knowledge base used by Trimeter's Logic consultant for logic design optimization without writing a single line of code.</p> <p>As an ASIC user, you can use the Knowledge Consultant to build your own ASIC knowledge bases for proprietary, internal cell libraries or to modify existing knowledge bases to incorporate your proprietary logic design techniques. As an ASIC vendor, you can supply a knowledge base to your customers, making it easier for them to create logic designs for your ASIC faster and more cost effectively.</p> <p>You use the Knowledge Consultant to draw an "antecedent circuit", a pattern of cells and macrocells that commonly appear in logic designs for your chip. Then you draw a "consequent circuit", a less obvious but more efficient implementation of the antecedent circuit's functionality. Then you define the port mapping between the two circuits to establish their relationship.</p> <p>The Knowledge Consultant includes special features that ease the creation of a knowledge base and makes it possible to create a complete knowledge base with 100 or more individual cells and macrocells in a matter of weeks.</p>	<p>Trimeter's Logic Consultant is an expert system-based complementary CAE tool for ASIC logic design optimization. It allows you to create ASIC logic designs that use fewer gates and/or run faster without changing your current design methodology.</p> <p>The Logic Consultant accepts input designs as netlists from Mentor Graphics systems with generic or foundry-specific symbols, as boolean equations or in PLD format.</p> <p>The Logic Consultant first minimizes the design's logic and evaluates timing constraints. Then, using expert system technology, the Logic Consultant selects the optimal combination of cells and macrocells from the targeted ASIC library which provide the required logic functionality with the highest performance and/or the least area possible.</p> <p>The Logic Consultant's Schematic Analyzer allows you to then quickly estimate propagation delays through selected signal paths, find the longest and shortest delay paths and calculate the associated timing delays of both the high-to-low and low-to-high signal changes.</p>

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Schematic Capture (Cont'd)			
Source	Trimeter Technologies	Valid Logic Systems Inc.	VIA Systems
Tool Name	Schematic Generator	ValidGED	CircuitTool
FOR DETAILED DATA SEE:		page 4660	
Tool residence	APOLLO	DEC MICROVAX, IBM PC/XT/AT, Valid SCALD-system	APOLLO, DEC MICROVAX, SUN
Schematic database consists of: Graphics symbols Simulation model data Physical layout data	X	X X X	X X
Netlist compilation As symbols are entered Batch mode after capture		X	X
Electrical rules check Batch mode On-line (Interactive)		X X	X X
Rules checked Connectivity Open nets Unassigned pins Multiple naming of nets Connections between sheets Fanout User-defined rules		X X X X X X X	X  X X
Database accessibility Procedural interface EDIF interfaces		X X	X
Color display		X	X
ASIC libraries supported	Mentor Graphics Gen Lib, LSI Logic	AMCC, AMD, AMI, ASEA HAFO, AT&T, Control Data, Digital Equipment, Fairchild, Ferranti, Fujitsu, Harris, Hitachi, Hughes, IQSMP, IMSC, Intel, LSI Logic, Matra Harris, MEDL, Mietec, Mitsubishi, MMI, Motorola, etc.	
Description	<p>Trimeter's Schematic Generator automatically creates clear, readable schematics from netlists.</p> <p>The Schematic Generator frees you from platform-dependence: you can capture your initial schematic on one CAE system, take the resulting etlist to another system for simulation, layout, optimization, etc., and then recreate the schematic from the netlist on the new system.</p> <p>The Schematic Generator also allows you to document netlist changes resulting from simulation, testing and/or layout. You can easily create corrected schematics without having to manually capture the changes yourself.</p> <p>And the Schematic Generator allows you to clean up and standardize schematics created by different schematic capture systems and/or by different designers.</p>	<p>The ValidGED Graphics Editor is an easy-to-use schematic drawing tool developed specifically for accelerating design entry. You can use ValidGED to create and modify drawings using parts from existing component libraries or from libraries you have created yourself using ValidGED.</p> <p>The Graphics Editor serves as an entry point into Valid's family of design tools. It is used to create designs at any level of hierarchy, including block diagrams, hierarchical schematics, and flat schematics.</p> <p>ValidGED incorporates pre-assigned backannotated information into the schematic. Dynamic dragging allows objects or groups of objects to be moved anywhere on the screen in one continuous motion while retaining complete orthogonal connectivity. Snap-to-pin wiring is supplied to expedite the wiring process. Variable scaling capability lets you select any viewing area of a drawing. Simultaneous zoom and pan facility allows you to quickly find and view any portion of the schematic. ValidGED also performs design rule checking to ensure that the schematic is free from graphical errors.</p>	<p>CircuitTool features include schematic capture, interactive rule checking, symbol creation and on-line help. Netlist generation for direct interface to the CADAT and HS-PICE simulators, DRACULA layout verification and BLOCKS router are provided. All functions are supported through on-screen menus, immediate help files and on-line documentation.</p>



## DESIGN AUTOMATION—Design Tools

## Design Tool Capability

## Front End Design Tools—Schematic Capture (Cont'd)

VLSI Technology VTIschematic page 4665	Wintek HiWIRE page 4674	Xerox Expert Schematics XEROX	
APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN	IBM PC/XT/AT		
X X X	X	X X	
X	X	X	
X		X X	
X X X X X X	X X X X	X X	
X	X		
X	X	X	
VLSI Technology gate array library, standard cell library, megacell, compiler libraries.		Intel, Motorola, LSI Logic, Zilog.	
VTIschematic: The schematic editor enables the user to create, view, edit, annotate and plot hierarchical schematic diagrams of standard cells, megacells, gate arrays, cells from the cell compiler library, and custom-compiled cells. With its on-line checking feature, this editor prevents incompatible connections of conflicting signals and produces as an output an accurate netlist that can be used in the simulator for verification of the design.	HiWIRE is a computer-aided-design package that aids electrical engineers and technicians in the creation and revision of electronic schematics on an IBM Personal Computer. Finished schematics can be drawn by a pen plotter or printed by a dot matrix printer. The package includes an extensive library of TTL, CMOS, ECL, ladder, microcomputer, and discrete components. Schematics are generated by interconnecting library elements using wires and buses. Components can be moved, copied, deleted, or rotated with a click of the mouse button. New symbols can be quickly defined by combining graphical objects. No special commands are required; symbols are simply miniature diagrams created with the same commands as the drawing itself. The menu-driven operation is easy to learn and to remember. The menu appears only when it is needed and does not occupy valuable screen space. Clicking the mouse button repeats the previous operation quickly and simply. The HiWIRE package includes netlist and bill-of-materials utilities along with complete documentation. HiWIRE is sold with a 30-day money-back guarantee. Price: \$895.00.	The Expert Schematics package is a tool for design synthesis. Its database is hierarchical, and provides for ways to partition a design into functional blocks, design the logic of each block, and then combine the functional blocks into a complete schematic. Unique features of this system include user-defined properties and user-definable data Formatter and Extractor. The system attaches pages to a design in progress as needed. It allows the user to exchange, copy, move data from one design to another, with any number of designs or pages displayed on the screen simultaneously. Direct link to the Expert Simulator and Expert PCB; no net-list generation is required.	

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Circuit Simulators			
Source	A.B. Associates, Inc.	Acotech	Analog Design Tools
Tool Name	I-G Spice	ALLSPICE	SPICE PLUS
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, CONTROL DATA, CRAY, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PRIME, SUN	IBM PC/XT/AT	APOLLO, HEWLETT-PACKARD, SUN
Device types supported			
Bipolar	X	X	X
MOS	X	X	X
GaAs	X		X
Acceptable inputs			
SPICE netlist	X	X	X
Schematic	X		X
Simulated signal generator	X		X
Outputs generated			
Amplitude waveform	X	X	X
Frequency spectrum	X	X	X
Guaranteed convergence			
Interactivity			
Stop and restart	X		X
Recompile incrementally	X		X
View changing waveforms	X	X	X
Relocate and add probes	X	X	X
Change stimulus during sim.	X	X	X
Heirarchical design	X	X	X
Modeling for temperature effects	X	X	X
Statistical analysis	X	X	X
Speed compared to SPICE	Same	1X	N/A
Capacity (max. transistors)	No limit	160	5,000
Description	<p>With interactive-Graphics SPICE there is no need to buy two or three different programs since I-G Spice does analog, digital and true mixed-mode analysis, low and high frequency, discretes and ICs. Low and high power. This is an interactive graphics version of the popular SPICE 2 program. This program retains all of the normal SPICE 2 capabilities, including AC, DC and transient analysis. In addition, this I-G version offers significant features which allow the engineer to have the flexibility, on-line speed and convenience of a truly interactive graphics package.</p> <p>Important features, only available on the I-G SPICE, include: user specified equations and tabular functions; multiple plots and plot expansion; non-linear magnetics; user-defined FORTRAN sub-programs; built-in digital gates and functions; extensive discrete, IC Macro &amp; FORTRAN based model libraries; real time, on screen, monitoring during analysis; and worst-case, Monte Carlo, optimization &amp; sensitivity analysis.</p>	<p>Only requires standard PC equipped with 512k, 8087 co-processor, PC DOS 2.1 or above.</p>	<p>SPICE PLUS, an analog simulation and analysis program, is an enhanced version of SPICE3, the latest version of SPICE, introduced by the University of California at Berkeley in November 1985. SPICE PLUS provides many new and improved features over existing SPICE programs, including new and more accurate device models, and analysis quality and speed improvements. In addition, SPICE PLUS is completely compatible with the extensive device model library, consisting of over 900 devices, also available from Analog Design Tools. It incorporates the new Berkeley MOS4 model (also called BSIM, Berkeley Short-channel IGFET Model). BSIM eliminates short channel inaccuracies and uses process-characterized model parameters.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Circuit Simulators (Cont'd)

Analogy SABER	Berne Electronics ELAN-AC	Berne Electronics ELAN-Rel	Berne Electronics ELAN-TR
APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, IBM PC/XT/AT, SUN			
X X X			
X X			
X X			
X			
X X X X X			
X			
X			
10 - 15x			
No limit			
ASABER is a new generation analog simulator developed to take over where SPICE simulation left off. It has been designed from scratch using several completely new algorithms to eliminate the many disadvantages associated with other available circuit simulators. SABER runs 10-15 times faster than SPICE and CPU usage is sublinear with circuit size allowing it to simulate much larger circuits. Modeling has been separated from the simulator and allows simple definitions of both system and circuit level devices. SABER is also SPICE compatible in input format and has all the standard SPICE models making transitions very easy.	Interactive AC analysis for circuits up to 100 nodes and 300 branches containing capacitance, resistance, inductance, multiple windings and dependent generators. Interactive AC analysis program for circuit designers. Analyzes large circuits and provides information regarding circuit performance including gain, phase shift, input and output impedances, y-parameters and group delay. Sensitivity analysis can pinpoint components that most affect circuit performance. Monte Carlo simulation of production spreads (with any kind of distribution) allows economical prediction of production yields. Built-in models are included for resistors, capacitors, inductors, mutual couplings, independent and dependent generators, transistors, FETs and operational amplifiers. If more complex models are desired, user-defined FORTRAN equations can be added.	True non-linear DC analysis program for reliability and parametric studies of circuits. Exact diode and Ebers-Moll representations are used for semiconductor models. Tolerance, sensitivity, worst-case and Monte-Carlo analysis. Nonlinear, DC analysis program development for use in a time-sharing interactive mode. Performs reliability analysis. Can be used to perform detailed, nonlinear DC design analysis. An engineer with no previous knowledge of computer programming can analyze electronic circuits containing passive and/or active semiconductor components. Allows the determination of a circuit's complete DC nonlinear performance characteristics.	Interactive system of circuit analysis programs. Non-linear, DC, transient and radiation analysis of 100-node and 250-branch networks performed using sparse matrix and variable time-step algorithms and non-linear models for semiconductors and linear transimpedances. Includes nuclear radiation effects analysis and high-resolution graphic output presentations. Provides a large semiconductor data bank containing approx. 300 devices. Supplies additional FORTRAN equations to increase the possible range of analysis and linear transconductance models for Beta, Mu, Gm and Zm. Stores and retrieves problem data from disk files. Provides user-defined FORTRAN equations capability and interface for further circuit and reliability analysis.

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Circuit Simulators (Cont'd)			
Source	Berne Electronics	Brainpower	Cadnetix
Tool Name	I/CAP	DesignScope	CDX-3200
FOR DETAILED DATA SEE:			
Tool residence		APPLE	SUN, MSDOS PCs, Cadnetix Analysis Engine
Device types supported Bipolar MOS GaAs			X X
Acceptable inputs SPICE netlist Schematic Simulated signal generator			X X X
Outputs generated Amplitude waveform Frequency spectrum		X X	X X
Guaranteed convergence			X
Interactivity Stop and restart Recompile incrementally View changing waveforms Relocate and add probes Change stimulus during sim.		X  X	X  X
Heirarchical design			X
Modeling for temperature effects			X
Statistical analysis			X
Speed compared to SPICE			Speed margin incr. for more complex ckts
Capacity (max. transistors)		250 recursive nodes, unlim non-recursive	8000 ICs
Description	Conversational interactive program featuring free format input, graphical output, AC and TR analysis algorithms, double precision arithmetic and built-in text editor. Interactive version of the IBM ECAP/360 program. Data can be input using the full ECAP formats. Provides full 50-node 200-branch capability, conversational interactive language, text editor, selected output control, graphic output and stored subcircuit models.	Interactive circuit design simulation for the 512K Macintosh. With DesignScope, you can develop an optimum system without knowing component values in advance. DesignScope allows the engineer to place system components in a Macintosh window, connect them into a block diagram, assign them parameters, and, finally, run a circuit simulation of the system and view the waveforms. The engineer does all this without needing specific component values or a prototype circuit design. If simulation results warrant, the entire system can be changed in seconds and a new simulation run. The process is quick, flexible, accurate and modular.	Cadnetix' Analog Design Environment (CADE) is available on Cadnetix' Analysis Engine and MS DOS personal computers. Any Physical system that can be described by continous equations can be simulated with CADE, including systems comprised of mixed technologies (electronic, electro-mechanical, optical, chemical, etc.)  CADE's user-interface, called the Analog Data Grapher, provides input generation, simulation set-up and initiation, and graphical display capabilities. Analyses typically employed by system designers are readily available to the CADE user: AC, DC, transient, sensitivity, noise, distortion, large signal - steady state, Fourier, and Monte Carlo. These analyses are accessible through pop-up forms in the Analog Data grapher. In addition, the Analog Data Grapher emulates an eight channel oscilloscope, a network analyzer, a function analyzer, a function generator or any other instrument typically found in the lab.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Circuit Simulators (Cont'd)

Case Technology PSpice (see MicroSim)	Clarity Systems S-SPICE	Control Data ASPEC	Daisy Systems DSPICE/ Virtual Lab
DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN	APOLLO	APOLLO, CONTROL DATA, DATA GENERAL, DEC VAX, IBM MAINFRAME/MINI, IBM PC/XT/AT, RIDGE	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, Daisy Logician 386/Personal Logician 386
X X X	X X	X X X	X X X
X X	X X	X X	X X X
X X	X	X X	X X
		X	X
X	X X	X X X X X	X X X X X
X	X	X	X
X	X	X	X
X			X
	Comparable	1-2X, CYBER 205 = 300X VAX 11/780	1-5X
Platform dependent, approx 200 on PC	Limited by node memory	30,000	No limit
Based on SPICE from Berkely, includes GaAsFET models and device models for diodes, transistors, power MOSFETs, op amps and comparators. Results displayed in a graphics window with all node voltages and device currents available. Available options include Monte Carlo analysis, model extraction, subcircuit parameters for standard analog components.	In Clarity's SimuSet environment, circuit simulation is provided via the S-SPICE circuit simulator. The simulations are activated through SuperSet's Uniform Simulation Environment, USE, that provides high-level input and output in a simulated lab environment. S-SPICE is based on a widely used and trusted analog circuit simulator that has been fully integrated within SuperSet. S-SPICE is activated through USE and operates directly on either schematics or the topology of a circuit without having to extract a net list.  Typically, SPICE is used for the critical path timing simulation. S-SPICE is even more powerful and easy to use in SuperSet because of its integration with other SuperSet modules and its friendly, interactive user interface. It can directly simulate transistor level views created in GeoSet, TopSet, StrucSet, GluSet and PlaSet. The results are displayed graphically, as waveforms. Absolute and incremental values of voltage, current, and time can be read by cursor and mouse control. X and Y scales of displayed waveforms can be changed quickly through pop-up menu commands. Remote S-SPICE simulations may be run on any node in the network. Simulation results will be displayed on the user's workstation, as if the simulation was run locally.	ASPEC: Advanced Simulation Program for Electronic Circuits is an integrated circuit analog simulation program that provides extremely accurate analysis at and below one micron feature sizes. An optimizing model generator produces model fit to within .01% accuracy. Features include alphanumeric node names, modularized or encrypted data input, nested macros and global updating, circuit simulation worst-case analysis, user defined functions, and IF-THEN-ELSE constructs. The CYBER 205 version has been heavily vectorized and performs at peak speeds of up to 300 times a VAX 11/780.	Daisy's analog and circuit simulation environment consists of the Virtual Lab user interface, the DSPICE circuit simulator, and the Analog Libraries.  The Virtual Lab environment features a highly-interactive user interface that emulates the control panels and display functions of familiar analog test systems. This familiarity greatly simplifies learning and use while giving designers flexibility far surpassing that of typical breadboard/instrument setups.  The DSPICE simulator delivers complete analog simulation- including DC, time and frequency domain analysis, statistical, and worst case- without complicated netlists or batch print-outs. DSPICE is fully integrated with the Virtual Lab environment enabling designers to work interactively with their schematics.  The Analog Libraries include over 1300 models for discretes, analog ICs and functional blocks which allow high-level simulation. Several hundred power devices and over 140 magnetic core materials work with a very accurate transformer model. DSPICE allows the user to define easily new models and to modify characteristics of components in the libraries on-line.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Circuit Simulators (Cont'd)			
Source Tool Name FOR DETAILED DATA SEE:	ECAD SIMON	EEsof Microwave SPICE	EEsof TOUCHSTONE 1.5
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, SUN	APOLLO, DEC VAX, DEC MICROVAX, HEW-LETT-PACKARD, IBM PC/XT/AT, SUN	APOLLO, DEC VAX, DEC MICROVAX, HEW-LETT-PACKARD, IBM PC/XT/AT, SUN
Device types supported Bipolar MOS GaAs	X	X X X	X  X
Acceptable inputs SPICE netlist Schematic Simulated signal generator	X	X X	X
Outputs generated Amplitude waveform Frequency spectrum	X	X X	X
Guaranteed convergence	X		X
Interactivity Stop and restart Recompile incrementally View changing waveforms Relocate and add probes Change stimulus during sim.	X  X X X	  X X X	X  X X X
Heirarchical design	X	X	X
Modeling for temperature effects	X	X	
Statistical analysis			X
Speed compared to SPICE	30X	1X	100X
Capacity (max. transistors)	25,000 test to date, not a limit	260	N/A
Description	<p>SIMON is a high performance, proprietary algorithm driven, circuit simulator. SIMON is not a SPICE derivative, but is SPICE compatible and can accept SPICE netlists as an input or can output to SPICE. SIMON is targeted to address the design analysis of digital MOS ICs, and delivers DC and transient analysis for IC designs large or small. Areas that are SIMON's particular forte include: accuracy, speed of simulation, DC initialization, convergence, very large circuits, interactive or batch operation, user modeling, and extensive diagnostics.</p> <p>SIMON is very memory efficient. Memory usage is approximately 1/2 MB per 10,000 transistors. Circuits tested and used in production have included up to 25,000 transistors (this is not a limit, but rather the largest circuits attempted). The real limit is based only on virtual memory space available.</p>	<p>For non-linear analysis of RF/microwave circuits. For AC, DC, and transient power analysis as well as distortion, noise, and AC sensitivity, in both time and frequency domain. Offers in-depth analysis of the non-linear aspects of the circuits. Microwave SPICE reads Touchstone as well as standard Berkeley 2G.6 files, enabling the engineer to move easily between Touchstone and Microwave SPICE. The program also writes S-parameters automatically formatted for use by Touchstone. Use Microwave SPICE to analyze the start-up transient and spectral content of oscillators; plot conversion loss as a function of RF level in mixers; observe power compression of multi-stage amplifiers; measure output power vs. input power and output power vs. frequency.</p>	<p>For linear circuit analysis, interactive tuning, random and gradient optimization, Monte Carlo yield prediction, and network analyzer support. Applicable to the design of MMICs, complex amplifier networks, filters, microstrip and stripline circuits, multiplexers, oscillators, diplexers, and virtually all other RF/microwave circuits. Touchstone's analysis capabilities include one-to-four-stage noise figure with feedback, differential phase shift and loss, gain and noise circles, source mapping and stability circles, group delay, and voltage gain, in addition to the more common analysis tools such as S-parameters.</p> <p>Equation block uses equations among variables, numeric constants, and predefined parameters (pi and sweep frequency) to specify additional variables for use as parameters in the circuit description. These equations may include common arithmetic operations and trigonometric, logarithmic, and exponential functions. The processor block calculates the sums, differences, products and quotients of calculated scattering parameters to allow the comparison of network characteristics. Optional libraries available with MMIC models from major foundries allow accurate simulation of MMIC circuits.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Circuit Simulators (Cont'd)

EEsof TOUCHSTONE/RF	Electrical Engr'ng Software PRECISE	Electronic Software Products PC-USPICE	Electronic Software Products USPICE
IBM PC/XT/AT	APOLLO, CRAY, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, IBM PC/ XT/AT, SUN	IBM PC/XT/AT	DEC VAX, ELXSI, IBM MAINFRAME/MINI
X	X	X	X
X	X	X	X
	X	X	X
	X		
X	X	X	X
X	X		
X	X		
X	X		
X	X	X	X
	X	X	X
	X		
	X	X	X
100X	3x	1X	1X
N/A	20,000	200	20,000
<p>For design engineers working primarily in the lower frequency ranges who need Touchstone's analysis and optimization but don't need microstrip, stripline and waveguide elements, discontinuities and dispersion. Includes support for HP 3577 and 8753 Network analyzers.</p> <p>PRECISE software for analog circuit simulation. A complete set of analysis capabilities for the analog designer. Time and frequency domain, temperature, power, radiation, sensitivity, Monte Carlo, worst case, distortion and noise all available to the analog designer. Commands to selectively plot variables including overlay. Probe nodes dynamically. Define input stimuli for a set of standard waveforms. Develop custom functions. Standard parts library available includes: op amps, transistors, diodes and comparators. General device level interface and link to characterization programs. Professionally documented and supported.</p>			

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Circuit Simulators (Cont'd)			
Source	Elxsi	EXAR	Ferranti Interdesign
Tool Name	Parallel SPICE 2G.5	P Spice (see MicroSim)	Silicon Design Sys. FSPICE
FOR DETAILED DATA SEE:	page 4222		
Tool residence	ELXSI	APOLLO, IBM PC/XT/AT	DEC VAX, DEC MICROVAX
Device types supported			
Bipolar	X	X	X
MOS	X	X	
GaAs	X	X	
Acceptable inputs			
SPICE netlist	X	X	X
Schematic			X
Simulated signal generator			
Outputs generated			
Amplitude waveform	X	X	X
Frequency spectrum	X	X	X
Guaranteed convergence			X
Interactivity			
Stop and restart	X		X
Recompile incrementally			X
View changing waveforms			
Relocate and add probes		X	X
Change stimulus during sim.			
Heirarchical design	X	X	X
Modeling for temperature effects	X	X	X
Statistical analysis	X		
Speed compared to SPICE	3x using 4 CPUs	3X	1X
Capacity (max. transistors)	16,000	150	2,000
Description	This is a parallel version of Berkeley Spice 2G.5 (public domain), modified to run on multiple CPU Elxsi Systems 6400's. Available only to Elxsi users.	P Spice is a general circuit analysis system derived from SPICE. It is used as part of an integrated development system called FIDS (Flexar Integrated Development System).	For linear circuit analysis of ULA peripheral cells, a modified form of SPICE is provided (FSPICE) fully characterized for ULA transistor structures. This includes worst case analysis for voltage, temperature and processing variations.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Circuit Simulators (Cont'd)

FutureNet (Data I/O) DASH SPICE 2G3.3 page 4651 IBM PC/XT/AT	Harris Semiconductor SLICE page 4246 MASSCOMP, SUN	IBM CIEDS/Analog-Digital Simulator IBM MAINFRAME/MINI, IBM RT PC	IBM CIEDS/Switched Capacitor Sim. IBM MAINFRAME/MINI, IBM RT PC
X X	X X X	X X	X
X X X	X X 2	X	X
X X	X X	X	X X
X		X	
X X X X X	X X X X X		
X	X	X	X
X	X	X	X
X	X		
1X	Same	4-5 times faster than SPICE	
	Approx. 2,000	Memory dependent	Memory dependent
	SLICE, Simulated Language with Integrated Circuit Emphasis, is an interactive program which interfaces with the SPICE2 program developed at Berkeley. SLICE offers a wide range of commands with which one can write high-level computational algorithms as well as sending information to and receiving information from SPICE.	CIEDS/Analog-Digital Simulator is a true mixed-mode analog-digital simulator ideal for simulating analog sampled data circuits with their digital control logic. Simulation time is minimized with piecewise linear models for all non-linear devices. Simulation results can be evaluated with a graphical display utility. The simulator allows: time domain simulation of mixed analog and digital circuits; switched-capacitor circuit simulation together with applicable digital control logic; and, investigation of delay warnings and worst-case delays that are not available from a pure logic simulator.	CIEDS/SWITCHED-CAPACITOR SIMULATOR is a time-and-frequency domain simulator for switched-capacitor integrated circuits. Responses can be evaluated with a powerful graphics-based, interactive display utility. The system accommodates input/output coupling, aliasing, and duty cycles of clock signals. In addition it supports frequency analysis of: amplitude and phase, including sample and hold effects and continuous I/O coupling; component and parasitic sensitivities; group delay and amplitude slope; intermodulation and harmonic distortion due to non-linear capacitance and amplifiers; and, noise density, including noise folding and the effects of incomplete charge transfer.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Circuit Simulators (Cont'd)			
Source	Intergraph	Intusoft	Mentor Graphics
Tool Name	Analog Analysis Tools	PC Circuit Design Tools	MSIMON
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, DEC MICROVAX, InterPro 32C, SCS-40	AT&T, HEWLETT-PACKARD, IBM PC/XT/AT	APOLLO
Device types supported			
Bipolar	X	X	
MOS	X	X	X
GaAs		X	
Acceptable inputs			
SPICE netlist	X	X	X
Schematic	X		X
Simulated signal generator	X		
Outputs generated			
Amplitude waveform	X	X	X
Frequency spectrum	X	X	
Guaranteed convergence	X		X
Interactivity			
Stop and restart			X
Recompile incrementally	X		X
View changing waveforms	X		X
Relocate and add probes	X		X
Change stimulus during sim.	X		X
Heirarchical design	X	X	X
Modeling for temperature effects	X	X	X
Statistical analysis	X	X	X
Speed compared to SPICE	14X	1/5 VAX 11/780	20X
Capacity (max. transistors)	Limited by avaialbe memory	230	40,000
Description	<p>Analog Analysis Tools are a group of virtual test instruments used to simulate and observe response from the circuit under design. The AAT also provides advanced functions such as freehand waveform generators and waveform calculators. Optional modules include functions such as signal processing (convolution, deconvolution, windowing, etc.), mixed analog and digital simulations, as well as statistical techniques.</p> <p>CSPICE is a high performance circuit simulator. Accessed through Analog Analysis Tools, CSPICE features AC, DC and transient modes, along with advanced analysis. On large problems, CSPICE is up to fourteen times faster than traditional SPICE-like products. Intergraph provides an extensive library. A modeling service is available.</p> <p>Analog Circuit Simulation (ACS) is an optional modeling module that permits the user to describe devices or process in three ways: first, devices can be modeled as black boxes through laboratory measurements; second, device characteristics or transfer functions can be used; and finally, system level simulation can be accomplished by writing modules in a high level language.</p>	<p>Three programs provide a SPICE analysis capability for IBM and compatible PC's. First, data is entered using the PRE.SPICE editor and library using an extended SPICE syntax for including libraries, passing parameters to subcircuits and identifying statistical parameters. The PRE SPICE program converts the extended syntax to a standard SPICE netlist that can be run on the PC using the second program, IS.SPICE or on a mainframe. IS.SPICE is U.C. Berkeley SPICE version 2G.6 compiled for the PC. The third program, Intu.Scope provides an interactive graphical presentation of the SPICE output. Grids are statistical, log or linear. Features include integration, differentiation, Fourier transforms and polynomial regression along with algebraic, trigonometric and transcendental operations on waveforms. Output is to a dot matrix printer or plotter. The programs can be run automatically to collect Monte Carlo statistics.</p> <p>All standard SPICE devices are supported plus a library of macro models that include GaAs FET, saturable reactor, pulsewidth modulator, op-amps, comparators, SCRs, power transistors, and optoisolators.</p>	<p>MSIMON is an interactive analog simulator used with the Mentor Graphics IDEA Series of 32-bit engineering workstations. MSIMON runs directly from design files created by NETED, the Mentor Graphics schematic capture tool, and provides full interactivity during simulation.</p> <p>For designers of MOS ICs, MSIMON offers dramatic increases in simulation speed (up to 30X), as well as the ability to simulate much larger designs. MSIMON also features excellent convergence, meaning users spend less time getting designs to simulate correctly.</p>



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Front End Design Tools—Circuit Simulators (Cont'd)**

Mentor Graphics MSPICE	Meta-Software HSPICE	Meta-Software Parallel HSPICE	Meta-Software RADSPICE
APOLLO	APOLLO, CONVEX, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, IBM PC/XT/AT, PRIME, SUN, Amdahl, FPS, Alliant, Edge	ELXSI	APOLLO, CONVEX, CRAY, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, IBM PC/XT/AT, PRIME, SUN, Alliant, FPS, Amdahl, IBM RT-PC, Edge
X X X	X X X	X X X	X X X
X X	X X X	X X X	X X X
X	X X	X X	X X
	X	X	X
X X X X X	X X	X X	X X
X	X	X	X
X	X	X	X
X			
1X	.5 to 10X	.5 to 10X	
2,000	No limit	No limit	No limit
MSPICE is an interactive analog simulator used with the Mentor Graphics IDEA Series of 32-bit engineering workstations. MSPICE runs directly from design files created by NETED, the Mentor Graphics schematic capture tool, and provides full interactivity during simulation.	<p>HSPICE is an analog simulator of electronic circuits based on the U.C. Berkeley SPICE program. HSPICE is fully supported and incorporates over 20 man-years of development. It is extensively used in industry on a wide range of applications. HSPICE provides a greatly improved convergence and extensive diagnostics to help cases of non-convergence. Improved convergence is a result of a number of enhancements including improved matrix solution methods and sophisticated automatic timestep control. More accurate models also increase likelihood of convergence, especially with larger circuits.</p> <p>HSPICE features a wide variety of high quality model equations. Complementing these models equations is Meta-Software's comprehensive service for determining device model parameters. This consists of a device characterization laboratory service and model parameter extraction service. HSPICE features an interactive graphics post-processor, an up-to-date discrete device library, eight character node names, full parameterization, easy access to sub-circuit nodes, and availability on a wide selection of computers. Advanced analysis modes in HSPICE include segmented transient time point selection, operating points during transient analysis, DC temperature sweep and DC parameter sweep.</p>	Meta-Software's HSPICE has been modified to use up to 12 Elxsi CPUs simultaneously to run one simulation. Meta-Software supports only one version of Parallel HSPICE for any Elxsi configuration from 1-12 CPUs. The enhanced convergence and modeling that Meta-Software is known for in the serial version are maintained in the parallel version.	RADSPICE is a superset of the HSPICE circuit simulator, adding the modeling of radiation effects to the capabilities of HSPICE. It is the product of a joint venture between Meta-Software and the Science Applications International Corp., a recognized authority on the performance of electronics in a radiation environment. RADSPICE adds the following features to HSPICE: Transient gamma radiation effects on all P-N junctions, selection of six photocurrent generation models, neutron degradation on bipolar junction transistors, total radiation dose degradation on MOSFETs, saturable magnetic transformers and cores, and radiation voltage and current sources.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Circuit Simulators (Cont'd)			
Source	Micro Linear	MicroSim	Royal Digital Systems
Tool Name	PSPICE	PSPice	AutoMate Circuit Simulator
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	APPLE, AT&T, DEC VAX, DEC MICROVAX, HEWLETT-PACKARD, IBM PC/XT/AT, NEC PC, SUN, IBM PS-2	CONTROL DATA, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, PRIME, SUN
Device types supported			
Bipolar	X	X	X
MOS		X	X
GaAs		X	X
Acceptable inputs			
SPICE netlist	X	X	X
Schematic	X		
Simulated signal generator	X		
Outputs generated			
Amplitude waveform	X	X	X
Frequency spectrum	X	X	X
Guaranteed convergence	X	X	
Interactivity			
Stop and restart	X	X	
Recompile incrementally			
View changing waveforms		X	
Relocate and add probes		X	
Change stimulus during sim.			
Heirarchical design	X	X	X
Modeling for temperature effects	X	X	X
Statistical analysis		X	X
Speed compared to SPICE	1X	1.4X	
Capacity (max. transistors)	Same as PSPICE	Unlimited (200 for DOS)	
Description		<p>PSPice has greatly reduced the convergence problems that prevented the simulation of some circuits using Berkeley SPICE and other SPICE-based simulators. PSPice comes with a comprehensive 240 page reference manual and a continually expanding, non-encrypted, model library of common discrete devices. Included are: power MOS-FETs, bipolar transistors, opamps, diodes, voltage comparators and transformer cores.</p> <p>Innovative options such as" partial source code (DEVICE EQUATIONS), graphics post-processing (PROBE), parameter estimation (PARTS), statistical Analysis (MONTE CARLO), and an interface to digital simulators (DIGITAL FILES), are also available.</p> <p>MicroSim offers expert technical assistance provided by the same engineers who wrote the software. All of MicroSim's software engineers are experienced design engineers as well. This means that help will be available from people who understand the questions.</p> <p>PSPice was introduced in January of 1984. To date, more copies have been sold than all other commercial SPICE simulators combined.</p>	<p>SPICE has been closely integrated into the AutoMate Circuit Simulator system. This easy-to-learn version of SPICE allows the designer to accomplish in minutes what would take hours or days on a breadboard. All the analysis tools from SPICE are provided: DC (bias point), transient (time), AC (frequency), and noise behavior analysis at varying temperatures- along with a tool for viewing simulation results that acts as a graphics-based "software oscilloscope". The continually expanding library of device models includes bipolar transistors, diodes, power MOS-FETs, operational amplifiers, and voltage comparators.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Circuit Simulators (Cont'd)

SDA Systems SPICE/HSPICE Interface	Sierra Semiconductor MIXsim	Silicon Compiler Systems Lsim	Spectrum Software MICRO-CAP II
APOLLO, DEC VAX, DEC MICROVAX, MAS-SCOMP, SUN	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN, TEK-TRONIX	APOLLO, DEC VAX, DEC MICROVAX, SUN	APPLE, IBM PC/XT/AT, Macintosh
X X X	X	X	X X
X X X	X X	X X X	X X
X X	X	X	X X
X	X	X	
X	X X X X X	X X X X X	X X X X X
X	X	X	X
X	X	X	X
X		X	X
1X	Comparable to logic simulator	From 4X to >1000X	1X
Machine dependent	Unlimited	Unlimited	100 nodes
The SDA design automation environment integrates SDA's own tools with some of the industry's best known simulation packages. The system's unique framework architecture allows for the easy and quick integration of new tools. The SPICE/HSPICE interface consists of the following components: 1) the netlist tool for the automatic creation of netlists formatted appropriately for the simulators, 2) the waveform display tool to automatically convert into waveforms and display the simulators' output, and 3) the simulation and test language to create the stimulus required to drive the simulation. Through the SPICE/HSPICE interface the user gains access to these simulators without having to learn the details of their user interface, netlist and output formats. Note that SDA supports interfaces to both SPICE and HSPICE simulators. The SDA environment maintains the integrity of the databases, and a uniform user interface.	MIXsim is a behavioral, event driven, mixed analog/digital circuit simulator. Unlike other mixed analog/digital simulators MIXsim is not a hybrid of SPICE and a digital simulator. It is ideal for debugging system errors and generating test programs. The behavioral models allow for highly accurate representation of both digital and analog functions, while computer time and usage is similar to digital simulators.	Lsim is an interactive mixed mode logic/circuit simulator providing mixed degrees of freedom in both the functional and timing domain. Lsim accepts as input a hierarchical circuit description consisting of functional modules of circuit elements and their connections. Functional modules can range in complexity from transistors to microprocessors. Module development parallels generator development performed by SDL's Generator Development Tools, providing the same degree of flexibility in the simulation domain that generators provide in the layout. Users have the option of simulating their generator layouts at the transistor level or writing their own functional module for the generator using the functional compiler language-Mc.	MICRO-CAP II is an integrated, interactive electronic drawing and analysis program featuring high-speed matrix solvers that allow extremely fast simulations on networks of up to 100 nodes. Using the built-in schematic editor, AC, DC, transient or Fourier analysis may then be performed. Results are plotted during the analysis providing quick graphics feedback. The built-in Parameter Estimation Program and library make modeling easy.

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Circuit Simulators (Cont'd)			
Source	Tatum Labs	Tatum Labs	Tektronix CAE Systems
Tool Name	EC-Ace	ECA-2	HSPICE (see Meta-Software)
FOR DETAILED DATA SEE:			page 4658
Tool residence	AT&T, IBM PC/XT/AT	AT&T, IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX
Device types supported			
Bipolar	X	X	X
MOS	X	X	X
GaAs			X
Acceptable inputs			
SPICE netlist	X	X	X
Schematic			X
Simulated signal generator	X	X	X
Outputs generated			
Amplitude waveform	X	X	X
Frequency spectrum	X	X	X
Guaranteed convergence	X	X	X
Interactivity			
Stop and restart	X	X	
Recompile incrementally	X	X	
View changing waveforms	X	X	X
Relocate and add probes	X	X	
Change stimulus during sim.	X	X	
Heirarchical design	X	X	X
Modeling for temperature effects	X	X	X
Statistical analysis		X	
Speed compared to SPICE	20X	20X	10%-50% with comparable accuracy
Capacity (max. transistors)	40	200	No theoretical limit
Description	EC-Ace is a low cost subset of Tatum Labs' advanced ECA-2. It offers the same interactive style as ECA-2, and the same AC, DC, and transient analysis. It does not offer worst-case, Monte-Carlo, or component sweeping. It does have a proper diode model with temperature drift, and the macro capability, which allows the designer to model transistors. Ace runs easily on a small PC with only 128K memory and a single floppy disk drive.	ECA-2 is a high performance analog circuit simulator with AC, DC, transient, and Fourier analysis. It is a full nonlinear simulator, including nonlinear capacitors and inductors. Parts can vary with time or frequency. It includes worst-case analysis, Monte-Carlo analysis, macro-models, complex y-parameters, transmission lines, and the ability to sweep components. It is fully interactive and can also be run in batch mode.	HSPICE Simulation System provides analog circuit design verification thru use of the HSPICE circuit simulator developed by Meta-Software. The HSPICE Simulation System includes support of the Tektronix DISCRETE library of discrete PCB components. High simulation accuracy is possible through advanced device modeling. The simulation system supports all options available with the HSPICE circuit simulator. The simulator can perform nonlinear DC analysis, nonlinear transient analysis and linear small-signal AC analysis either separately or concurrently. Noise and distortion reports can be specified when performing AC analysis. Fully compatible with DDSC, the HSPICE Simulation System will allow graphical viewing of various output results. HSPICE allows the user to perform sweeping of temperature values and sweeping of parameter values during an HSPICE DC analysis. Complete command syntax checking is performed by the interface.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Circuit Simulators (Cont'd)

Tektronix CAE Systems SPICE 2G.6 Interface page 4658	The Western Design Center CIRCUIT	Vamp Analogsim	Viewlogic Systems PSPICE
APOLLO, DEC VAX, DEC MICROVAX	APPLE, DEC VAX, IBM PC/XT/AT, PRIME, Apple IIgs	APPLE	IBM PC/XT/AT
X X	X X	X X	X X
X X X		X X	X X
X X	X	X	X X
	*		
X		X X X X	X X  X
X			X
	X		X
10%-50% with comparable accuracy	Four times faster	N/A	1/5 of 11/780 when run on IBM PC/AT
Approximately 1000	100 MOSFETS standard, 100 bipolar stand.	N/A	120 on IBM PC/AT
The SPICE Interface provides analog circuit design verification through use of the University of California, Berkeley SPICE 2G.6 circuit simulator. When used with Tektronix' DDSC, the SPICE Interface allows an analog design engineer to capture an analog circuit, simulate the circuit and analyze simulation results via a graphical waveform output. The SPICE Interface supports all options available in the public domain version of SPICE 2G.6 The SPICE simulator can perform nonlinear DC analysis, nonlinear transient analysis and linear small-signal AC analysis. Noise and distortion reports can be specified when performing AC analysis. The supplied SPICE 2G.6 program has been modified to allow graphical viewing of various output results. The SPICE Interface includes a 28 component primitive library. Complete command syntax checking is performed by the interface.	Given a network description, CIRCUIT calculates the node voltages, branch currents and branch power in the quiescent state or as a function of time.  Allowed circuit elements are bipolar and MOS transistor, diodes, resistors, capacitors, inductors, current sources and grounded voltage sources. Sources may be either sinusoidal or piecewise linear functions of time. The BJT and MOSFET models simulate the nonlinear I-V relationships, junction and charge storage capacitances, inverse and saturated operation and temperature effects. * Only on Tuesdays, if we enter the data, and during leap years.	Fully compatible with Spice 2G.6.	

# IC MASTER

## DESIGN AUTOMATION—Design Tools

Generic Function

Design Tool Capability

### Front End Design Tools—Circuit Simulators (Cont'd)

Source	VLSI Technology		
Tool Name	VTIspace		
FOR DETAILED DATA SEE:	page 4665		
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN		
Device types supported Bipolar MOS GaAs	X		
Acceptable inputs SPICE netlist Schematic Simulated signal generator	X		
Outputs generated Amplitude waveform Frequency spectrum	X		
Guaranteed convergence	X		
Interactivity Stop and restart Recompile incrementally View changing waveforms Relocate and add probes Change stimulus during sim.	X X X X X		
Heirarchical design	X		
Modeling for temperature effects	X		
Statistical analysis	X		
Speed compared to SPICE			
Capacity (max. transistors)			
Description	VTIspace is a circuit simulation program for nonlinear DC, nonlinear transient, and linear AC analyses. It is most commonly used when analyzing a small schematic or the critical path in circuits containing resistors, capacitors, voltage sources, or MOSFETs. VTIspace can be used in conjunction with the VTIsim simulator and the other verification tools.		



DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers			
Source	Acasi	Aida	Aldec
Tool Name	LIBSIM	Aida Logic Simulator	SLAV
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, IBM PC/XT/AT, SUN	APOLLO, SUN	IBM PC/XT/AT
Device types supported			
Bipolar	X	X	X
MOS	X	X	X
GaAs	X	X	X
Hierarchical simulation			
Switch level	X		
Gate level	X	X	X
Functional level	X	X	X
Behavioral level	X	X	X
Physical model level			
Outputs generated			
Truth table	X	X	
Waveform	X		X
Interactivity—During simulation			
Start and restart	X	X	X
Recompile incrementally	X	X	X
View changing waveforms	X		X
Relocate and add probes	X	X	X
Change stimulus	X	X	X
Supports EDIF	X		
Test vector generation language	X	X	X
Timing verification			
Typical values	X	X	*
Min/Max		X	
Worst-case		X	
Number of states	18 visible, 36 internal	0,1, Unknown, High Impedance	12
Number of primitives	143	40	250 +
Resolution (min. ps)	Unlimited		Unlimited
Capacity (gates max.)	500,000	1 million	50,000
Speed (gate evaluations/sec)	18,000	5 million	
Link to fault simulator (name)		Aida Fault Simulator	HASS
ASIC libraries supported		Contact Aida.	Fujitsu, Fairchild.
Description	LIBSIM is a sophisticated, highly interactive logic simulator running on the standard IBM PC and many compatibles at better than half the speed of Daisy's Logician at a fraction of the cost, according to Acasi. LIBSIM is fully integrated to FutureNet Schematics and is targeted for the PCB and IC designer. It is the first simulator to have the capability of processing JEDEC fuse maps and simulating PLDs, PALs, and PLAs as part of an entire PCB taking into account propagation delays with unprecedented accuracy. LIBSIM simulates TTL, CMOS, NMOS, ECL and Schottky at the functional, gate, switch, and fuse levels simultaneously. LIBSIM is an extremely powerful tool to reduce the design iterations, debug logic circuits, verify timing, and aids in test vector generation. It eliminates the need for bread-boarding, drastically reducing design overhead and time to market.	The Aida Logic Simulator offers rapid simulation preparation and execution of multi-chip, multi-board designs. With the Aida CoSimulator Processor, the Logic Simulator can be accelerated up to 5 million gate evaluations per second, with a capacity of 1 million gates. Without hardware acceleration, it offers event-driven and leveled Compiled Code simulation using the workstation processor.	Functional simulation only.

Bold face indicates data is provided in the page noted

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Applicon	Berne Electronics	CAD Group, Inc. (CGI)
Tool Name	Logic Analysis	I/LOGIC	SALT
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, DEC MICROVAX, SUN		APOLLO, APPLE, AT&T, CONTROL DATA, CON-VEX, CRAY, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, IBM PC/XT/AT, NEC PC, RIDGE, SUN
Device types supported			
Bipolar	X		X
MOS	X		X
GaAs			X
Hierarchical simulation			
Switch level	X		X
Gate level	X		X
Functional level	X		X
Behavioral level	X		X
Physical model level	X		
Outputs generated			
Truth table	X		X
Waveform	X		X
Interactivity—During simulation			
Start and restart	X		X
Recompile incrementally	X		X
View changing waveforms	X		X
Relocate and add probes	X		X
Change stimulus	X		X
Supports EDIF			
Test vector generation language			X
Timing verification			
Typical values	X		X
Min/Max	X		X
Worst-case	X		X
Number of states	21		36
Number of primitives	>100		5 switch/96 gate/100 behav./1500 funct.
Resolution (min. ps)	100ps		1 ps
Capacity (gates max.)			Limited by RAM memory size
Speed (gate evaluations/sec)	Dependent on CPU		3,000/sec/MIP
Link to fault simulator (name)	Included		PFG
ASIC libraries supported			
Description	Logic Analysis is an integrated logic, timing, and fault simulator for electronic designers. It enables the engineer to model a network, analyze its performance, debug logic errors, and optimize the overall circuit characteristics without building a prototype. Components may be modeled using structural, functional, or behavioral level software modeling capabilities. Complex components may also be modeled with the Dynamic Hardware Modeler. Logic Analysis may also be used to generate test vectors for popular automatic test equipment, ATE, systems. A high-level language is used to describe the device stimuli and provide capabilities for macros, bus manipulation, test pattern input, and synchronous waveform generation. Logic Analysis also performs timing analysis using min/max delays of all components. Results may be displayed in either tabular or graphic form.	Used to evaluate logic networks by simulating AND gates, OR gates, flip-flops and delays in the design of digital systems for breadboarding before implementation. User can input data for each logic block, run the simulation, make modifications and store the problem on data files. The problem can then be retrieved from disk files, edited and re-run as desired. Timing diagrams are printed at the terminal, allowing the user to check designs. Handles RS, JK, T, D and one-shot flip-flop logic blocks, AND, NAND, OR, NOT and XOR gates. All gates allow up to eight inputs. Signal components can be obtained by using the negative of the signal desired. A macro command is available for definition and repeated use of special functions in a simulation. Initialization of all blocks, variable waveform inputs and race conditions are also provided.	SALT, a 36 state, event driven, advanced engineering design tool for improved logic design and verification, was created to accurately model and simulate complex situations using the principles of hierarchical design. Circuits can be simulated and verified using the multi-level (switch, gate, functional, behavioral, system, architectural) approach, and capabilities exist that will allow concurrent, mixed-mode, analog/digital simulations without exiting the SALT environment to access another simulator (e.g. SPICE, P-SPICE, etc.).  Through a unique dynamic circuit testing feature (DCT), SALT provides an accurate prediction of total propagation delay at all times during simulation, and coupled with its fanin-fanout delay computations, allows the user to generate precise design information along with test vectors for the actual device, whether it is a chip, a board, or an entire system. Features include: incremental compilation; load dependent delays; separate net model and stimulus files; degree of interactive capability; multiple checkpoint restart capability; support of SCALD syntax; grouping of nodes/signals with alias names.

Bold face indicates data is provided in the page noted



## DESIGN AUTOMATION—Design Tools

## Design Tool Capability

## Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

Cadram Digital Circuit Simulation	Cadnetix Cadnetix Digital Design	Calma TEGAS 5	Calma TEXSIM/B
IBM MAINFRAME/MINI	SUN, Servers, workstations, Analysis Engine	CRAY, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI
X X X	X X X	X X X	X X X
X X X	X X X X	X X	X X X X X
X X	X X	X X	X X
X X X X	X X X X	X X	X X X X
	X		
X		X	X
X	X X X	X X X	X X
21	21	4	18
91	458	72	76
100	100	1 ps	
125,000	1,000,000	700,000	700,000
Function of CPU	1,000 to 200,000- depends on circuit/CPU	2,000	2,000
CADAT	Cadnetix Concurrent Fault Simulator	Included	TCAT
	LSI Logic, NCR, Toshiba, TI, VLSI Technology, Thomson-Mostek	SMOS 2u DLM CMOS arrays, Harris 3u SLM CMOS cells, GE 2u DLM CMOS arrays, GE 1.25u DLM CMOS cells, RCA 1.25u DLM CMOS/SOS cells, RCA, etc.	SMOS 2u DLM CMOS arrays, Harris 3u SLM CMOS cells, GE 2u DLM CMOS arrays, GE 1.25u DLM CMOS cells, RCA 1.25u DLM CMOS/SOS cells, etc.
Cadram offers Digital Circuit Simulation, a product which applies sophisticated computer modeling techniques to the task of testing and analyzing electrical and electronic designs. Digital Circuit Simulation integrates CADAT, a high function integrated logic, timing and fault simulation package, into the Cadram interactive graphics environment. It allows printed circuit boards and integrated circuits to be tested and debugged in software, providing a fast, cost-effective alternative to prototyping with physical devices.	Depends on workstation or engine running Cadnetix Digital Design Environment and circuit characteristics.	Includes fault simulation, testability analysis, automatic test generation.	TEXSIM/B is a verification package for logic simulation and highly accurate timing analysis of bipolar and MOS technology designs. A Pascal-like hardware description language can be used to describe designs at the behavioral level. Numerous HDL features enable very easy use and a wide range of design capabilities. Behavioral modules described at this high level can be integrated with descriptions using gates and MOS devices for a mixed-level simulation.  The TEXSIM/B program enables propagation delays to be associated with the rising and falling signal elements and input and output pins. Timing models can be adjusted to reflect loading delays and delays due to interconnect properties.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Calma	Case Technology	Case Technology
Tool Name	TSCAN (timing verifier)	CADAT (see HHB Systems)	CT2600 Timing Verifier
FOR DETAILED DATA SEE:			
Tool residence	APOLLO	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN	IBM PC/XT/AT
Device types supported			
Bipolar	X	X	X
MOS	X	X	
GaAs	X	X	
Hierarchical simulation			
Switch level		X	
Gate level	X	X	X
Functional level	X		
Behavioral level		X	
Physical model level		X	
Outputs generated			
Truth table		X	
Waveform	X	X	
Interactivity—During simulation			
Start and restart	X		
Recompile incrementally	X		
View changing waveforms	X		
Relocate and add probes	X		
Change stimulus	X		
Supports EDIF	X		
Test vector generation language	X		
Timing verification			
Typical values	X	X	X
Min/Max	X	X	X
Worst-case	X	X	X
Number of states	9	21	
Number of primitives	N/A	106	
Resolution (min. ps)	1 user-defined unit	100	
Capacity (gates max.)	700,000	IBM PC: 3,000; DEC, SUN no prac. limit	
Speed (gate evaluations/sec)	N/A	DEC: 2-3K; PC: 3-400; SUN: 4-5K	
Link to fault simulator (name)	N/A	CADAT	
ASIC libraries supported	SMOS 2u DLM CMOS arrays, Harris 3u SLM CMOS cells, GE 2u DLM CMOS arrays, GE 1.25u DLM CMOS cells, RCA 1.25u DLM CMOS/SOS cells, etc.	LSI Logic (directly) and others through OEM arrangements.	
Description	<p>Included in Calma's Logic Explorer, TSCAN is a timing verifier used during the design phase of digital IC design. Logic simulation is a very important but time consuming step in the design of integrated circuits. Traditionally, logic simulation is run iteratively until all functional and timing problems are corrected. It is usually more efficient, however, to perform functional and timing verification separately. When working with synchronous designs, a very fast, comprehensive timing verifier like TSCAN may be applied.</p> <p>TSCAN: Reports the cause of timing verification vs. providing simulation output which must be interpreted. Requires little input stimulus, typically only clock assertions. Much faster than full simulation for timing analysis. Useful to characterize devices (for instance to determine max. prop. delays, max. freq.). Performs timing analysis across varying operating conditions (min., max. delays across best, typical and worst case conditions). Identifies critical paths for IC design.</p>	<p>CADAT is an integrated logic, timing, and fault simulator for electronic design and test engineers. CADAT is ideally suited for the design of printed circuit boards and ASICs. SSI and MSI components are modeled with conventional software models, while LSI and VLSI components are modeled using the HHB Systems CATS Dynamic Hardware Modeler. CADAT ASIC model libraries can be used to simulate gate array and standard cell devices. CADAT automatically calculates the effects of fanout loading in networks and updates device timing. For board level work, min/max delay simulation can be used to analyze the circuit's sensitivity to variations in component device timing.</p>	<p>A timing verifier for use on the personal computer has been introduced by Case Technology. The Case Timing Verifier on the IBM PC, the CT2600, is based on the original SCALD timing verifier developed at the Lawrence Livermore Laboratories. In contrast to the min-max timing analysis performed by most simulators, which can check for only one delay condition at a time, the Case Timing Verifier program performs true worst-case timing verification. This involves checking for all timing errors that might occur through the full range of a circuit's delays. The Case Timing Verifier detects setup and hold errors, race conditions, minimum pulse width errors, and clock glitches.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

Clarity Systems MIXIM	Control Data MIDAS	Control Data SALT(see CAD Group, Inc.(CGI))	Daisy Systems DLS Daisy Logic Simulator
APOLLO	APOLLO, CONTROL DATA	DEC VAX, IBM PC/XT/AT	IBM PC/XT/AT, Daisy Logician 386/Personal Logician 386
X	X	X X	X X X
X X X X	X X X	X X X X	X X X X X
X X	X X	X X	X X
X X X X X	X X X X X	X X	X X X X X
X	X		X
	X		X
X X	X X X X	X	X X X X X
A continuum of logic strengths of 2**32	4	36	DLS 12-state, DTV 24-state
55 primitives plus behavioral descript.		3 +	40 +
100 ps	One	Unlimited	Unlimited
Depends on node memory	5 million		32,000
Depends on circuit type	1.1 million gate-clocks/sec	250 eval/sec- PC/XT, 1010 events- VAX	2,000
	Automatic Fault Simulator		MegaFAULT
			Fujitsu, LSI, VTI, TI, Intel, Motorola, GE/RCA, NEC, Matsushita, Fairchild, NCR, Zymos, Gould/AMI, Harris, AMCC, National, IMP, Xilinx, Ferranti, Philips, Plessey, etc.
MIXIM is a true mixed-mode, multi-level simulator, used to verify the functionality and performance of a design. MIXIM simulates behavioral, functional, gate level and switch (transistor) levels of a design. MIXIM is an event-driven, compiled function simulator. MIXIM does not require netlist extraction from the design database. Since the connectivity data for blocks is embedded in the integrated database, explicit description of block interconnections is not required as simulation input. MIXIM recognizes 7 logic levels: 0 (low), 1 (high), X (don't care), U (unknown/indeterminate), R (rising), F (falling) and O (Oscillating). MIXIM replaces the artificial notion of finite strengths by providing a HI Z strength and a continuum of driving strength (2**32 possible values) for wired-OR, wired-AND, and 3-state bus modeling for behavioral, functional, or gate simulation, and true analog RC analysis at switch level simulation. MIXIM allows components with zero delay, unit delay, finite delay, separate rise and fall times, and fan-out dependent delays. The Behavioral Description Language, BDL, is a powerful PASCAL-like high level language for hardware modeling.	The Boolean Evaluator (BEV) portion of Control Data Corp.'s Modular Integrated Design Automation System (MIDAS) performs clock-driven, zero-delay evaluations of synchronous logic designs as large as five million gates and beyond. Networks of logic elements may be described hierarchically and be defined as any combination of, gate, block, procedural or truth table models.  Designed for functional evaluation of multi-chip, multi-board systems, the BEV will improve simulation speeds by 30 to 50 times those of event-driven simulators and perform comparably with hardware-based simulators without the need to purchase special purpose hardware.	DLS analyzes and verifies the logical operation of board level or IC designs. It is an interactive 12-state logic simulator and operates in software (DLS) or hardware accelerated versions (MDLS on the MegaLOGICIAN).  Daisy Timing Verifier (DTV) analyzes circuit timing-related hazards. DTV expands the approach used by batch-oriented timing verifiers to incorporate an interactive interface to evaluate asynchronous design logic as well as synchronous datapath designs. DTV provides 24-state timing analysis.  DLS and DTV are fully integrated with other Daisy verification tools, offering: a common database, common libraries, and single compilation.	

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DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Daisy Systems	Data General	ES2/US2
Tool Name	MDLS MegaLOGICIAN	TEO/Electronics Simulator	SOLO 1000
FOR DETAILED DATA SEE:			
Tool residence	Daisy MegaLOGICIAN	DATA GENERAL	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, VAXstation 2000
Device types supported			
Bipolar	X	X	X
MOS	X	X	
GaAs	X	X	
Hierarchical simulation			
Switch level	X	X	X
Gate level	X	X	X
Functional level	X	X	
Behavioral level	X	X	
Physical model level	X		
Outputs generated			
Truth table	X	X	X
Waveform	X	X	X
Interactivity—During simulation			
Start and restart	X	X	X
Recompile incrementally	X	X	X
View changing waveforms	X	X	
Relocate and add probes	X	X	X
Change stimulus	X	X	X
Supports EDIF	X	X	
Test vector generation language	X		
Timing verification			
Typical values	X	X	X
Min/Max	X	X	X
Worst-case	X		X
Number of states	12	12	5
Number of primitives	40 +	200 +	53
Resolution (min. ps)	Unlimited	100 ps	10 ps
Capacity (gates max.)	64,000	Unlimited	12,000
Speed (gate evaluations/sec)	100,000		N/A- switch level simulator
Link to fault simulator (name)	MegaFAULT		Proprietary, HILO, SILOS, CADAT
ASIC libraries supported	Fujitsu, LSI, VTI, TI, Intel, Motorola, GE/RCA, NEC, Matsushita, Fairchild, NCR, ZyMOS, Gould/AMI, Harris, AMCC, National, IMP, Xilinx, Ferranti, Philips, Plessey, etc.	Fujitsu Microelectronics.	European Silicon Structures, Texas Instruments, Philips, AMI
Description	<p>MDLS analyzes and verifies the logical operation of board level or IC designs. It is an interactive 12-state logic simulator and operates in software (DLS) as well as this hardware accelerated version (MDLS) on the Daisy MEgaLOGICIAN.</p> <p>MDLS is fully integrated with other Daisy verification tools, offering: a common database, common libraries, and single compilation.</p> <p>MDLS accommodates any combination of switch-level, gate-level, functional, behavioral, and physical modeling, providing the means for fast and accurate simulation of any design.</p>	<p>The TEO/Electronics Interactive Logic Simulator provides mixed-mode simulation and timing verification for gate, functional, and behavioral models of a design, and integrates with the TEO/Electronics Logic Design System. Simulation is performed on the data structure created during the design process. This alleviates the need for net list extraction, net list compilation, and output post-processing.</p> <p>In addition to conventional time-domain analysis that accepts vectors from a user or a file, the simulator can operate directly on the schematic drawing. A highlighted wire indicates a "1", a standard display indicates a "0", a dashed line an unknown state. This allows an engineer to check basic logic functionality right in the design domain. Fullhierarchy is supported in this mode. Monitoring and forcing probes can be placed at any level of a design hierarchy and anywhere within a particular level. To ease troubleshooting, sub-circuits can be isolated and independently simulated. Simulation can be halted at event or time breakpoints, and then re-started. Operation can be continuous or single-step. To allow easy interpretation of simulation data, multiple time windows can be displayed.</p>	<p>The SOLO simulator is an integral part of the SOLO package. It is a switch-level simulator for the simulation of MOS logic. Besides allowing both circuit verification and back annotation, it produces test data to run on Sentry testers. SOLO provides links to SILOS, HILO and CADAT.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

ES2/US2 SOLO 1200	EXAR HILO-3 (see Genrad)  page 4222 DEC VAX	Fairchild FAIRCAD  CRAY, DEC VAX, DEC MICROVAX	Ferranti Interdesign Silicon Design Sys. ULASIM  DEC VAX, DEC MICROVAX
X	X X X	X X	X
X X X X	X X X	X	X X X X
X X	X X	X X	X
X X X X X	X X X X 2	X X X X	X X X X
X			
	X	X	X
X X X	X X X	X X X	X X X
5	15	4	4
53	15	20	Full library
10 ps	Femtoseconds	50	100
12,000 gates	Unlimited		10,000
N/A switch-level simulator	1600 on VAX8600		10**6
Proprietary, HILO, SILOS, CADAT		Zycad, FAIRLOGS, PFAULT	
European Silicon Structures, Texas Instruments, Philips, AMI	N2000 a 2-micron N-well standard cell library from EXAR Corp. It combines digital, analog, and EEPROM cells.	Fairchild.	Ferranti Interdesign ULA.
The SOLO Simulator is an integral part of the SOLO package. It is a switch level simulator for the simulation of MOS logic. Besides allowing both circuit verification and back annotation, it produces test data to run on Sentry testers. SOLO provides links to SILOS, HILO and CADAT.	HILO-3 is a very powerful field proven digital design environment. EXAR design automation system uses HILO-3 as part of its FIDS (Flexar Integrated Design System)	Logic, timing and hierarchical simulation, as well as test program generation, are available on FAIRCAD. With hierarchical simulation the designer can simulate any block of a design as if it were an independent design; this hierarchical approach facilitates efficient design partitioning while maintaining consistency and improving the integration of the overall circuit.  First, using typical, automatically calculated propagation delays for all components, logic simulation is performed on FAIRCAD to check the accuracy of the logic. Initially, fault simulation is run to determine whether the input test patterns successfully diagnose the existence of injected faults. Then, after placement and routing are complete, corrected delay times can be computed using actual wiring distances. To speed the computer-intensive task of fault simulation, access to Fairchild's Cray 1-S Supercomputer (located in Milpitas, Calif.) is provided. Next, controllability analysis is run by FAIRCAD at the designer's facility to generate a potentially detectable and undetectable faults listing. Test vectors are produced for automatic test equipment (ATE) with programs that create and edit package-pin files.	

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	FutureNet (Data I/O)	Gateway Design Automation	Gateway Design Automation
Tool Name	DASH CADAT-Plus	VERILOG	VERILOG-XL
FOR DETAILED DATA SEE:	page 4651		
Tool residence	IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN, Silicon Graphics	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN, Silicon Graphics
Device types supported			
Bipolar	X	X	X
MOS	X	X	X
GaAs	X	X	X
Hierarchical simulation			
Switch level	X	X	X
Gate level	X	X	X
Functional level	X	X	X
Behavioral level	X	X	X
Physical model level	X		
Outputs generated			
Truth table	X	X	X
Waveform	X	X	X
Interactivity—During simulation			
Start and restart	X	X	X
Recompile incrementally	X	X	X
View changing waveforms	X	X	X
Relocate and add probes	X	X	X
Change stimulus	X	X	X
Supports EDIF	X		
Test vector generation language	X	X	X
Timing verification			
Typical values	X	X	X
Min/Max	X		
Worst-case	X	X	X
Number of states	21	106	106
Number of primitives	>100	35 standard plus user definable	35 standard plus user-definable
Resolution (min. ps)	100	2*31 user-definable units	2*31 user definable units
Capacity (gates max.)	35,000	200,000 (mainframes w/50MB virtual mem)	100,000*, 1,400,000**
Speed (gate evaluations/sec)	1,000	5,000 on 68020-based workstation	Up to 200,000
Link to fault simulator (name)	DASH-FAULTSIM	TESTGRADE	TESTGRADE
ASIC libraries supported	Gould, National, Fairchild, Motorola.		
Description	<p>DASH-CADAT-Plus provides design engineers with the capability to perform complex logic simulation, timing analysis and testing, and fault simulation-- all on an IBM-AT. DASH-CADAT-Plus uses a library of over 100 primitives, a 32-bit coprocessor with 4 megabytes of memory, logic-analyzer-style waveform displays, and 21 simulation states to let engineers simulate application-specific circuits (ASICs) of up to 30,000 gates. When coupled with the optional CATS hardware modeler, engineers can also accurately model VLSI components and complex printed circuit boards. By using newly devised "interval mathematics" and a new MOS analysis algorithm, DASH-CADAT-Plus also provides increased accuracy for gate level simulations.</p> <p>DASH-CADAT-Plus uses the 32-bit coprocessor to perform simulations at speeds matching those of a VAX 11/750 while running under AT&amp;Ts UNIX System V operating system. The UNIX-based program is wrapped in a color graphics MS-DOS shell to take advantage of easy-to-use pop-up menus and waveform displays that allow the user to view activity on any node in the circuit at 0.1 nanosecond intervals.</p>	<p>VERILOG is a powerful, mixed-level digital design language and interactive simulation system that integrates the capabilities of behavioral level languages, register-transfer level languages, and numerous gate-level and switch-level languages, along with the capability of dynamically interacting with user-written software programs. VERILOG provides advanced interactive debugging facilities and employs a single homogeneous language for circuit description, waveform description, and symbolic debugging. VERILOG combines high-speed compilation of the design description with high-speed simulation thereby providing a truly interactive capability on computers the size of today's workstations.</p> <p>At the behavioral/register level, VERILOG's features include sequential and/or concurrent process execution, dynamic delay expressions, named events, arithmetic/logical/and bit-wise reduction operators, procedural constructs, and dynamic linkup with user programs written in high-level languages allowing for the modeling of D/A and A/D converters, FFT algorithms, etc., in conjunction with the VERILOG models of hardware.</p>	<p>VERILOG-XL is a high performance, mixed-level digital design language and interactive simulation system that supports architectural, functional, behavioral, RTL, gate and switch-level modeling. A single homogeneous language is provided for hierarchical circuit description, waveform description and interactive symbolic debugging. VERILOG-XL uses "significant event simulation" at high design levels. At lower levels, an advanced form of clock suppression, called "adaptive behavior recognition", is employed. As a result, VERILOG-XL simulations at all levels is extremely fast and efficient. VERILOG-XL features include sequential and/or concurrent process execution, dynamic delay expressions, named events, arithmetic/logical/and bit-wise reduction operators, procedural constructs, dynamic link to user-written programs, and a hardware model library. VERILOG-XL accurately models bi-directional pass and resistive devices, dynamic MOS, charge and resistive devices, and signal contention. *on workstations with 4MB virtual memory. ** on mainframes with 50 MB virtual memory.</p>

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DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

GE Solid State Division MIMIC Logic Simulator page 4235	Genrad HILO-3	Gould Semiconductor Division SCEPTRE II page 4244	Harris Semiconductor CADAT (see HHB Systems) page 4246
APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN	APOLLO, DEC VAX, DEC MICROVAX, HEW- LETT-PACKARD, IBM MAINFRAME/MINI, RIDGE, SUN, NEC EWS4800, Intergraph	IBM PC/XT/AT, NEC PC, VICTOR	APOLLO, DATA GENERAL, DEC VAX, ELXSI, IBM MAINFRAME/MINI, IBM PC/XT/AT, MASSCOMP, PYRAMID, SUN
X X X	X X X	X	X X X
X X X X	X X X X X		X X X X X
X X	X X	X X	X X
X X X X X	X X	X	X X X X X
			X
X	X		X
X X X	X X	X	X X X
15 states and 32K resistive depths	15	10	21
34 (approx.) + behavioral level models	30	200 +	99
No limit; uses arbitrary time units	1 ps	100	100
Limited by CPU (32-bit addressing)	Machine-dependent		No defined limit; dynamic memory assign
25,000 on IBM 3083			
MIMIC	HILO-3	Generates node coverage statistics	CATS 9000
GE, LSI Logic, VLSI Technology	Motorola, National, ILS, VTI, Vadic, Cadic, Waferscale, California Devices, NEC, MHS, Thompson CSF, Asea, Ferranti, G.I., Marco- ni, Mietec.	Gould AMI.	LSI Logic, VTI, SMC: supported by HHB Sys- tems. Motorola, NEC: supported by Future- Net
The primary tool for GE/RCA's LSI semicustom logic circuit design system is the powerful simulation and fault-grading program called MIMIC. MIMIC is an acronym for Module Imitating Modern Integrated Circuits. This user friendly software tool enables the logic circuit designer to model and evaluate the logic operation of digital circuits correctly before they are fabricated in silicon. It provides user-definable behavioral modeling plus extensive hazard analysis. MIMIC enables the designer to simulate the circuit elements such as bus connections, wire ties, and bidirectional transmission gates and detect logic design flaws, races, bus conflicts, spike conditions and near-miss timing hazards. MIMIC goes well beyond logic network simulation and functional analysis. It can provide performance analyses, fault grading, stable-state fault simulation, real-time simulation, behavioral modeling, and the detection of timing problems. And it can generate a test pattern file that can serve as an input to ATE and thereby provide the designer with all tests needed to meet the user's original specifications for a logic circuit.	The HILO-3 Universal Logic Simulation System is an integrated set of software tools for logic verification and fault simulation in digital circuit design. The system's hierarchical framework supports today's design methodologies in full-custom and semi-custom integrated circuit, printed circuit board and system design. The HILO-3 system performs rapid effective design and test verification for thorough debugging of logic behavior before the prototype stage.  In HILO-3, circuits in a broad range of technologies can be described at a gate level or higher functional (behavioral) level. The circuit description language is truly hierarchical, permitting an arbitrary mix of gate and functional level constructs and unlimited sub-circuit nesting. A time based, block structured language is provided for specifying circuit stimulus and expected response.  The HILO-3 simulator has a 5 state, 15 valued algorithm for accurate simulation of MOS circuitry. The fault free simulator verifies circuit behavior in either nominal or min/max timing. Adjustments for capacitive loading may be made.  An extensive library of commercial components is available.	Supports complete cell-based ASIC design from schematic capture through physical layout and verification.	CADAT is an integrated logic, timing, and fault simulator. When used in conjunction with CAE schematic capture packages, CADAT allows the engineer to design a network, model its performance in software, debug logic errors, and optimize circuit performance. It is suited for the design of PCB's and ASIC's.

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## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Hewlett-Packard	HHB Systems	IBM
Tool Name	HILO-3 (see Genrad)	CADAT 6.0	CIEDS/Analog-Digital Simulator
FOR DETAILED DATA SEE:			
Tool residence	HEWLETT-PACKARD	APOLLO, DATA GENERAL, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, IBM MAINFRAME/MINI, IBM PC/XT/AT, MASSCOMP, SUN	IBM MAINFRAME/MINI, IBM RT PC
Device types supported			
Bipolar	X	X	X
MOS	X	X	X
GaAs		X	
Hierarchical simulation			
Switch level	X	X	X
Gate level	X	X	X
Functional level	X	X	
Behavioral level	X	X	
Physical model level	X	X	
Outputs generated			
Truth table	X	X	
Waveform	X	X	X
Interactivity—During simulation			
Start and restart		X	
Recompile incrementally			
View changing waveforms	X	X	
Relocate and add probes	X	X	
Change stimulus	X	X	
Supports EDIF		X	
Test vector generation language		X	
Timing verification			
Typical values	X	X	X
Min/Max	X	X	X
Worst-case	X	X	X
Number of states	15 valued	21	N/A voltage = function (time)
Number of primitives	18 gate-level primitives	108 parameterizable	100 + user-defined primitives
Resolution (min. ps)	1 ps	100ps	1 x 10 <sup>-2</sup> -.15 seconds
Capacity (gates max.)	Dependent upon swap space and disk size	Dependent on host machine's memory	Memory dependent
Speed (gate evaluations/sec)	6,300 events per second on HP9000/350	1000 on VAX 750	N/A
Link to fault simulator (name)	HILO-3	(included in CADAT)	
ASIC libraries supported	Fujitsu, NEC, Toshiba, TI	T.I., VTI, LSI Logic	
Description	The Design verification System provides accurate simulation results quickly. Stimulus and results can be either waveform or textual saving the designer time in stimulus creation. System designers have access to a large model library of TTL, ECL, MOS, and microprocessor models. Links from verification to test are also available.	CADAT 6.0 is an integrated simulation environment, supporting logic, fault and worst case timing. The CADAT simulation system is a virtual breadboard that allows a design engineer to debug logic and optimize circuit performance without building a prototype. Test engineers can work with the same CADAT description to develop test vectors. CADAT is ideal for the design of PCBs or ASICs. SSI and MSI components are modeled with CADAT's gate and functional models. LSI and VLSI can be modeled either behaviorally or physically with the CATS modeler. ASIC libraries can be used to simulate gate arrays and standard cell devices. Delay changes caused by fanout loading are automatically calculated by CADAT. Delays can also be calculated from the physical layout and back-annotated into the simulation. Minimum-pulse-width and setup/hold violations are reported to the designer. For PCB design, a worst case timing simulation can be performed to analyze the circuit sensitivity to variations in component device timing.	CIEDS/ANALOG-DIGITAL SIMULATOR is a true mixed-mode analog-digital simulator which can be used to investigate logic circuits without the limitations of an event-driven simulator with a pre-defined set of States. This simulator offers output in the form of voltage as a function of time which accurately represents what the designer would see in actual practice on the workbench. In the logic simulation mode, this product offers: piece-wise linear rise-time and fall-times with linear interpolation used between events; alternatively, R-C time constants can be used to specify rise and fall; critical path investigation and delay warning investigation capability; design verification of interfaces between digital control and analog circuits; and, powerful interactive graphics-based display utility for waveform viewing.



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
IBM CIEDS/Behavioral Simulator	IBM CIEDS/Logic Simulator	IKOS Systems Ikos 800	Intergraph HILO-3 (see Genrad)
IBM MAINFRAME/MINI, IBM RT PC	IBM MAINFRAME/MINI, IBM RT PC	IBM PC/XT/AT	DEC VAX, DEC MICROVAX, Intergraph Inter-Pro, InterAct
X X X	X X	X X X	X X
X X X	X	X X	X X X X
X X	X X	X X	X X
X X X X X	X X X X	X X X X X	X X
		X	X
X X X	X X	X X	X X X
Unlimited; user-defined		16	15 value algorithm
3,000 +	3,000 +	36	18 self generating
1	1	.1 psec	1 ps
Memory dependent	Memory dependent	64,000	Machine dependent- no practical limit
N/A		500,000 to 20,000,000	
		IKOS 800	HILO-3 fault simulation
		Ikos provides generic CMOS and ECL gate array libraries to support virtually any semi-custom vendor.	Fairchild, Fujitsu, Hitachi, Raytheon, S-MOS, Thomson-Mostek, VTI, Waferscale
CIEDS/BEHAVIORAL SIMULATOR is a hierarchical design simulator allowing designers to simulate integrated circuit or printed-circuit board system parameters early in the design process. It allows simulation at all levels of design including the architectural level, the register level, and the gate level. It includes many pre-defined routines to facilitate the creation of models. It also includes: unlimited state simulation (user defines the states); technology independent simulation; concurrent viewing of multiple simulations; breakpoints and dump/restart of simulation; interactive and batch mode; modeling of circuit components not contained in library; common Simulation Control Language with CIEDS/Logic Simulator; and powerful logic analyzer utility that displays circuit topology and waveforms generated during simulation.	CIEDS/Logic Simulator is a gate level simulator with significant throughput performance enhancements over a behavioral simulator. It uses specially designed primitive models (3000 + primitives available) to speed up gate level simulation. In addition, worst-case delay and timing verification checks with design error identification are provided. The product operates in the batch or interactive mode to enable large simulations to be run unattended. The following are also features of this simulator: library management tools for creating custom libraries for efficient simulation; concurrent viewing of multiple simulations; breakpoints and dump/restart of simulation; interactive and batch mode; back annotation module that customizes the effects of net capacitance and fan-in/fan-out loading; and, a logic analyzer utility that displays circuit topology and waveforms generated during simulation.	The IKOS 800 is claimed to be the first true turn-key solution for the logic validation of complex semi-custom circuits. The IKOS 800 complements existing CAE workstations by providing powerful stimulus entry, simulation and stimulus interpretation capability to allow simulation of seconds or minutes or even hours of system operation. The vast simulation resources of the IKOS 800 make it possible, before committing to mask tooling, to find the subtle design errors which inevitably result in semi-custom design iterations. The IKOS 800 consists of dedicated hardware accelerators linked together and controlled by powerful user-interface software running on a host computer. Complex hierarchical stimulus programs incorporating sophisticated programmatic constructs such as data substitution, looping and synchronization, can be entered graphically on the host computer. These stimulus programs are interpreted by the Stimulus Processing Hardware Accelerator at simulation run-time and fed directly into the Logic Simulation Hardware Accelerator.	The HILO Universal Logic Simulation System includes a hierarchical Hardware Description Language (HDL) for specifying logic designs, a Waveform Description Language (WDL) for describing circuit stimuli, a fault-free logic simulator, a fault simulator, a test generator, and a component library that contains over 3000 devices.  The HILO event-driven selective-trace simulator includes a 5-strength, 15-value logic state algorithm for accurate modeling of a wide range of device technologies such as TTL, ECL, Schottky, CMOS, NMOS, PMOS, STL, IIL. In fault simulation, a new Parallel Value List(PVL) algorithm combines the advantages of concurrent and parallel algorithms, providing fast execution and low memory overhead.  HILO outputs can be post processed to various pieces of automatic test equipment.

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DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	LSI Logic	Matra Design Systems	Mentor Graphics
Tool Name	LSIM/LDEL	ARCIS	QuickSim, QuickTime
FOR DETAILED DATA SEE:	page 4653		
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PYRAMID, SUN, Am-dahl	DEC VAX, IBM PC/XT/AT	APOLLO
Device types supported			
Bipolar		X	X
MOS	X	X	X
GaAs			X
Hierarchical simulation			
Switch level			X
Gate level	X	X	X
Functional level		X	X
Behavioral level	X		X
Physical model level			X
Outputs generated			
Truth table	X	X	X
Waveform	X	X	X
Interactivity—During simulation			
Start and restart	X		X
Recompile incrementally	X		X
View changing waveforms		X	X
Relocate and add probes			X
Change stimulus			X
Supports EDIF			X
Test vector generation language	X		X
Timing verification			
Typical values	X	X	X
Min/Max		X	X
Worst-case	X	X	X
Number of states	12 total states (3 logic, 4 strengths)	18	12
Number of primitives	31		95 + QuickParts
Resolution (min. ps)		1ns.	unlimited
Capacity (gates max.)	1,000,000 gates	IBM PC/AT = 3000, DEC VAX = 10,000	100,000
Speed (gate evaluations/sec)	N/A		6,000
Link to fault simulator (name)	Zycad	COFIS	QuickFault
ASIC libraries supported	All LSI Logic Corp. ASIC products.	Matra Harris Semiconductor.	
Description	Delay calculations and simulation are key to LSI Logic's design methodology. LDEL calculates the design's delay values for use in simulation. LSIM simulates the design, generates design performance data for other LDS programs and generates user-formatted simulation reports. These modules use design-specific network descriptions, simulation vectors and environmental specifications, plus LSI Logic's cell specifications, technology data, delay calculation algorithms and package specifications. As a result, the LDS model, its behavior and performance directly reflect those of the ASIC itself.	The relationship between propagation delay, fanout, loading, and parasitic delays as affects timing calculations is within 2% of SPICE simulations.	The QuickSim logic simulator provides full simulation interactivity. This means that simulations can be started and stopped at will to modify simulation conditions. These modifications are implemented through graphic "probing" of schematic displays of the circuit being simulated. These graphic probes can be used both for stimulus and acquisition operations.  QuickTime is the worst-case timing simulator member of the QUICKSIM Family. Whereas QuickSim uses either minimum, typical, or maximum timing delays. QuickTime simulates using either minimum and maximum, minimum and typical, or typical and maximum timing delays.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

Meta-Software Circuit Pathfinder	National Semiconductor Design Automation System page 4294	NCR Microelectronics VITA Series	P-CAD PC-LOGS
APOLLO, DEC VAX, DEC MICROVAX, ELXSI, SUN, IBM RT-PC, Edge Computer	IBM MAINFRAME/MINI, IBM PC/XT/AT, Dai- sy, Mentor, FutureNet workstations	Popular workstations	IBM PC/XT/AT
X	X		X X X
X X  X	X X X		X X X
X X	X X		X X
	X		X  X X
X X X	X  X		
	15		12
	18 basic types		50
	Arbitrary; 100ps commonly used		Unlimited
50,000 gates	100,000 + gates		500 on PC/XT, 1200 on PC/AT
15 gates per second	25,000 events/sec with 18MIPS CPU		
	HILO-3		
	National Semiconductor.		Motorola, G.E., T.I.
Circuit PathFinder provides analysis of path delay timings for NMOS and CMOS digital circuits. It quickly locates critical paths in even the largest circuits and generates an HSPICE netlist for full accurate simulation of these paths. This netlist includes all devices affecting the path delay. It can analyze circuits of any size, enabling the engineer to get accurate HSPICE simulation of the relevant portion of circuits too large to be practical for HSPICE analysis.	For the design of National Semiconductor gate arrays and standard cells.  National supplies all data necessary to simulate a gate array or standard cell design on Daisy, FutureNet, Mentor workstations using the simulator installed and supported by the workstation vendor. On its IBM compatible mainframe National uses Genrad's HILO-3 simulator.	Timing analysis CAD software for designing NCR Microelectronics' cell-based designs. VITA calculates delays through each cell in the design as a function of: 1) intrinsic delay; 2) rise/fall time of the input signal; 3) loading on the cell outputs; and, 4) voltage, process and temperature effects (best case, worst case, typical). The load on an individual node is the summation of the input capacitance of all driven elements, output capacitance of all paralleled outputs, and interconnect capacitance. The newest NODE DELAY release available for most supported workstations contains equation sets for each path through the cell such as SET/ to Q and CLOCK to Q. Extracted interconnect RC-tree delays are modeled as input pin delays. PATH DELAY identifies all synchronous paths in the design and adds the rise and fall delays along those paths, then reports all such paths which have a propagation delay greater than a user-specified value. QUICK DELAY finds a path between the user-specified start and end points and adds the rise and fall delays along the paths. PLUG DELAY transfers the delays calculated by NODE DELAY to the applicable simulation models.	

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DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Plessey	Praxis Systems	Racal-Redac
Tool Name	CLASSIC	ELLA	REDSIM CADAT
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX	APOLLO, DEC VAX, DEC MICROVAX, SUN	IBM PC/XT/AT, with co-processor
Device types supported			
Bipolar	X		X
MOS	X		X
GaAs			
Hierarchical simulation			
Switch level			X
Gate level	X	X	X
Functional level	X	X	X
Behavioral level		X	X
Physical model level			
Outputs generated			
Truth table	X		X
Waveform	X		X
Interactivity—During simulation			
Start and restart	X	X	X
Recompile incrementally	X	X	
View changing waveforms	X		
Relocate and add probes	X	X	
Change stimulus		X	X
Supports EDIF			
Test vector generation language	X	X	X
Timing verification			
Typical values	X	X	X
Min/Max	X	X	X
Worst-case	X	X	X
Number of states	8	User defined	21
Number of primitives		User defined	95
Resolution (min. ps)		Depends on abstraction	100
Capacity (gates max.)	100,000	Depends on abstraction	Unlimited
Speed (gate evaluations/sec)	6200 on VAX 11/780	Depends on abstraction	600 events/sec
Link to fault simulator (name)			REDSIM CADAT
ASIC libraries supported	Plessey CLAXXX.	A number of UK vendor's cells libraries have been coded in ELLA.	
Description		<p>The ELLA Design System is a VLSI design system based upon a behavioral hardware description language, a simulator and comprehensive design support environment. ELLA is unique among behavioral languages in that it has a common notation for behavior and structure. This means that the decomposition of behavior to structure is very efficient, significantly speeding up the design process. Additionally, ELLA is a succinct, yet very powerful, language and is easy to learn and use. A procedural interface is provided to the ELLA database which allows translations of designs to lower-level tools.</p> <p>The ELLA system is now in use in many of the UK's major electronics companies significantly reducing design time and cost and increasing design quality. ELLA is marketed in the US by ECAD, Inc.</p>	



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

Racal-Redac VISULA CADAT	Royal Digital Systems AutoMate Logic Simulator	Scientific Calculations SCISIM	SDA Systems SILOS Interface
APOLLO, DEC MICROVAX	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, PRIME, SUN	DEC VAX, IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, MAS- SCOMP, SUN
X X	X X X	X X X	X X X
X X X X X	X  X X	X X X X	X X X
X X	X X	X	X X
X  X		X X X X X	X
			X
X	X	X	X
X X X	X X	X	X X X
21	12	36	12
95 configurable		25 (approx.)	
100		1 ps	Unlimited
Unlimited	5,000 on PC/AT	4000 on PC/AT; 200,000 on VAX	Machine dependent
600		100 on PC/AT	6,000 events/sec
VISULA CADAT	Built-in		SILOS Fault Simulator
	A member of the AutoMate system's comprehensive set of simulation tools, the Automate Logic Simulator employs the industry standard SILOS simulator to assist in verifying digital semicustom IC designs. This simulator supports the systems designer at the logic and switch levels and the VLSI designer at the transistor level. SILOS models high-level functions such as registers, ROMs, RAMs, and PLAs, as well as primitives such as transistors, bidirectional transfer gates, and capacitors. To minimize simulation time, SILOS processes only the parts of a circuit that are active at each point in time. Simulation can proceed either interactively or in batch mode and the designer can view results with a logic-analyzer-like facility.	SCISIM is an advanced 36-state logic simulator integrated with the SCIDESIGN program for schematic capture. SCISIM is offered both on the IBM PC and the VAX. This allows desk-top use for medium size simulations and mainframe performance when desired.	The SDA design automation environment integrates SDA's own tools with some of the industry's best known simulation packages. The system's unique framework architecture allows for the easy and quick integration of new tools. The HILO and SILOS interfaces consist of the following components: 1) the netlist tool which automatically creates netlists formatted appropriately for the simulators, 2) the waveform display tool which automatically converts into waveforms and displays the simulators' outputs, and 3) the simulation and test language which creates the stimulus required to drive the simulation. Through the HILO and SILOS interfaces the user gains access to these simulators without having to learn the details of their user interface, netlist and output formats. The SDA environment maintains the integrity of the databases, and a uniform user interface.

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DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	SDA Systems	Sierra Semiconductor	Silicon Compiler Systems
Tool Name	Timing Analyzer	MIXsim	GENESIL Functional Simulator
FOR DETAILED DATA SEE:			
Tool residence	MASSCOMP	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN, TEK-TRONIX	APOLLO, DEC VAX, DEC MICROVAX
Device types supported			
Bipolar	X		
MOS	X	X	X
GaAs	X		
Hierarchical simulation			
Switch level	X	X	X
Gate level	X	X	X
Functional level	X	X	X
Behavioral level		X	
Physical model level			
Outputs generated			
Truth table		X	X
Waveform	X	X	X
Interactivity—During simulation			
Start and restart	X	X	X
Recompile incrementally		X	X
View changing waveforms		X	X
Relocate and add probes		X	X
Change stimulus		X	X
Supports EDIF	X		
Test vector generation language		X	X
Timing verification			
Typical values	X	X	
Min/Max	X	X	
Worst-case	X	X	
Number of states	12	5	14
Number of primitives	60	27	36
Resolution (min. ps)	Unlimited	100 ps	
Capacity (gates max.)	Machine Dependent	Unlimited	CPU memory dependent
Speed (gate evaluations/sec)			
Link to fault simulator (name)	SILOS	Zycad Mach 1000 accelerator	HILO-3
ASIC libraries supported		Sierra Semiconductor 2-micron silicon gate triple metal CMOS technology.	
Description	Unlike many traditional timing analyzers (TA's), SDA's requires no input stimuli to analyze the timing of a design and pinpoint signal paths that may cause timing problems. SDA's employs advanced algorithms to automatically analyze all cases of input patterns and find critical paths. Because TA is integrated into SDA's schematic editor, critical paths and delay values can be displayed on a schematic diagram as well as conventional timing diagrams. Standard analysis can be run and viewed without leaving the graphical environment of the schematic editor. TA also features mixed-level modeling and a high-level language that allows the designer to write timing tests in procedural terms.	MIXsim is a behavioral, event driven, mixed analog digital simulator. Unlike other mixed analog digital simulators MIXsim is not a hybrid of SPICE and a digital simulator. It is ideal for debugging system errors and generating test programs. The behavioral models allow for highly accurate representation of both digital and analog functions, while computer time and usage is similar to digital simulators.	Works with GENESIL and GENESIS silicon compilers.



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Silicon Compiler Systems GENESIL Timing Analyzer	Silicon Compiler Systems Lsim	Silvar-Lisco HELIX	Silvar-Lisco LOGIX-SL
APOLLO, DEC VAX, DEC MICROVAX	APOLLO, DEC VAX, DEC MICROVAX, SUN	APOLLO, DEC VAX, IBM MAINFRAME/MINI	
	X	X X X	
X	X X X X	X X X	
	X X	X X	
	X X X X	X X X X X	
	X		
X X X		X X X	
	192	User defined	
	User expandable	User defined	
	0.1	Unlimited	
	Unlimited	110,000	
	10,000	1,500	
	Lsim	(see Design Tool Interfaces)	
	Process independent standard cells. Library is user-expandable.		
Works with GENESIL and GENESIS silicon compilers. Data sheet results as a function of voltage and temperature.	Lsim is an interactive mixed logic/circuit mixed mode simulator providing mixed degrees of freedom in both the functional and the timing domain. Lsim accepts as input a hierarchical circuit description consisting of functional modules of circuit elements and their connections. Functional modules can range in complexity from transistors to microprocessors. Module development parallels generator development performed by SDL's Generator Development Tools, providing the same degree of flexibility in the simulation domain that generators provide in the layout. Users have the option of simulating their generator layouts at the transistor level or writing their own functional module for the generator using the functional module compiler language- Mc.	Helix is a behavioral simulator.	The LOGIX-SL software optimizes simulation of standard logic components. LOGIX-SL provides printed circuit board designers and users of ASIC foundry libraries a rapid, easy-to-use and highly efficient simulator. The LOGIX-SL software comes with a large assortment of behavioral models, which provides users with a large library of efficient, behavioral models that also perform self-contained setup, hold, and pulse-width error checking. The result is highly efficient debugging of designs.  The LOGIX-SL simulator is the first Silvar-Lisco simulator that is tightly coupled with the company's ASIC products, including Silvar-Lisco's GARDS, for gate array design, and CAL-MP, for standard cell design. LOGIX-SL uses parasitic layout capacitances as calculated by GARDS and CAL-MP. This refinement in simulation ensures a high degree of probability that the actual design will match the simulated results.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Silvar-Lisco	Simucad	Simucad
Tool Name	LOGSIM	P-SILOS	SILOS
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, DEC VAX, IBM MAINFRAME/MINI	IBM PC/XT/AT	APOLLO, DATA GENERAL, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, MASSCOMP, SUN, Daisy, Chromatics, Metheus, Valid
Device types supported			
Bipolar	X	X	X
MOS	X	X	X
GaAs	X	X	X
Hierarchical simulation			
Switch level	X	X	X
Gate level	X	X	X
Functional level		X	X
Behavioral level		X	X
Physical model level			
Outputs generated			
Truth table	X	X	X
Waveform	X	X	X
Interactivity—During simulation			
Start and restart	X	X	X
Recompile incrementally	X	X	X
View changing waveforms	X	X	X
Relocate and add probes	X	X	X
Change stimulus		X	
Supports EDIF			
Test vector generation language			
Timing verification			
Typical values	X	X	X
Min/Max	X	X	X
Worst-case	X	X	X
Number of states	15	12 + 5	12 + 5
Number of primitives	3,000	92	92
Resolution (min. ps)	Unlimited	Unlimited	Unlimited
Capacity (gates max.)	30,000	5,000	16,000,000
Speed (gate evaluations/sec)	1,500	1,200 on IBM PC/AT	4,000 on VAX 11/780
Link to fault simulator (name)	(see Design Tool Interfaces)		SILOS Fault Simulator (included)
ASIC libraries supported		Fairchild LS74 Series.	Fairchild LS74.
Description	Companion to Helix and layout with back annotation.	P-SILOS is virtually identical to its mainframe counterpart SILOS with the exception that current memory limitations of the IBM PC make fault simulation impractical. PSILOS' 12 + 5 State Modeling concept provides accurate modeling of MOS circuit behavior including bi-directional signal flow, charge storage and decay. In addition to the 12 logic states, P-SILOS provides models for: SWITCH LEVEL: unidirectional and bidirectional transistors, resistors and capacitors; GATE LEVEL: simple gate, wired-AND, wired-OR, flip flops and user defined gates; MEMORY MODELS: PLA, RAM, ROM and FUNCTIONAL/ BEHAVIORAL MODELS. Data created for the PC version can be uploaded and run on the mainframe version of SILOS. Data files created for the mainframe version of SILOS can also be run on the PC version.	SILOS is a combined logic/switch level simulator for electronic circuits. It performs logic and fault simulation in both interactive and batch mode. Data primitives include network-level devices, logic-level gates, as well as high-level functions. Inputs to network may be specified as individual clocks or as binary/hexadecimal tables. SILOS uses a unique 12 + 5 state concept which allows accurate modeling of bidirectional logic, wired-ORs, charge charing and node charge delay.  Event-driven logic simulation can be performed with zero or finite delays. SILOS allows users to simulate up to a timepoint, look at arbitrary output, then continue the simulation. It can generate summary tables of all node states, node spikes, unknown states and activity levels. Automatic network error checking and intialization, complete report generation facilities for both logic and fault simulation, and graphical output of simulation waveforms are provided. Sentry tester interface outputs can be requested.



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Spectrum Software MICRO-LOGIC II	Standard Microsystems Corp. STANSIM, STANTIME page 4310	Tatum Labs LSS-2	Tektronix CAE Systems HILO-3 (see Genrad) page 4658
IBM PC/XT/AT	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, Mentor, Daisy, Valid	IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX
	X	X X X	X X X
X	X X X X	X X X X	X X X X
X X	X X	X	X X
X X X X X	X X X X X	X X X X X	X  X X
	X		
	X		
X X	X X X	X X	X X X
3	Workstation dependent	4	5 states, 15 values
11		20	18
User-defined		Unlimited	1 ps
10,000		4,000	Limited only by disk space
1,200 events/sec		2,000	2000 to 4000
			HILO-3
	Standard Microsystems, NCR		NEC, Fujitsu, LSI, TriQuint, Chesapeake Group, Fairchild, Plessey, Matra Harris, ES2, Mar- coni Electronic Devices (MED), Westing- house
MICRO-LOGIC II is an integrated, in- teractive electronic drafting and simulation system featuring a fast event-driven timing and logic sim- ulator that lets you simulate net- works containing up to 10000 gates. Using a built-in schematic editor, an engineer can quickly create a logic diagram using basic boolean primitives, flip-flops or one of the hundreds of macros provided. A timing simulation can be done directly on the schematic. Results are plotted during simula- tion providing quick graphic feed- back. Built-in schematic editor and shape editor. Library of com- mercial devices.	Timing analysis software for verifying SMC cell-based designs. STAN- TIME calculates and displays propagation delays throughout a design. NODE shows delays through any element based on loading (both estimated and real) as well as electrical, temperature and process variations. PATH shows cumulative node delays along any path, a path being a se- ries of elements between two clocked elements or a clocked ele- ment and an I/O. PATH identifies all delays greater than a user- specified value.	Built-in editor.	HILO-3 Logic Simulation System inte- grates logic simulation, fault simu- lation and test pattern generation of digital logic designs. Applica- tions area ranges from detailed logic analysis to diagnostic test as- sessment of designs implemented as full-custom, semi-custom inte- grated circuits, printed circuit boards or complete systems. Addi- tionally, HILO-3 Logic Simulation System includes the Graphic Dis- play Formatter, a menu-driven vir- tual logic analyzer. Actual physical parts may be incorporated through the HICHP Hardware Modeler.

## DESIGN AUTOMATION—Design Tools

Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Teradyne	The Western Design Center	Thomson/Mostek
Tool Name	LASAR Version 6	LOGIC	SIM
FOR DETAILED DATA SEE:			page 4321
Tool residence	DEC VAX, DEC MICROVAX, Valid, Teradyne DATAServer Sim. Engine	APPLE, DEC VAX, IBM PC/XT/AT, PRIME, AP- PLE IIgs	DEC VAX
Device types supported			
Bipolar	X	X	
MOS	X	X	X
GaAs	X	X	
Hierarchical simulation			
Switch level	X	X	
Gate level	X	X	X
Functional level	X	X	X
Behavioral level	X		
Physical model level	X		
Outputs generated			
Truth table	X	X	X
Waveform	X		X
Interactivity—During simulation			
Start and restart	X		X
Recompile incrementally	X		X
View changing waveforms	X		
Relocate and add probes	X		
Change stimulus	X		
Supports EDIF			X
Test vector generation language	X	X	X
Timing verification			
Typical values	X		X
Min/Max	X		X
Worst-case	X		X
Number of states	15*	3	
Number of primitives	25 + unlimited behavioral	15	
Resolution (min. ps)	1		100
Capacity (gates max.)	2,000,000**	10,000 standard, unlimited w/recompile	40,000 +
Speed (gate evaluations/sec)	20,000	1000	Hardware dependent
Link to fault simulator (name)	Lasar Version 6		FSIM
ASIC libraries supported	AMCC, AMD, Motorola, Fujitsu, LSI Logic.	The Western Design Center	Mostek.
Description	Fifteen logic values combine with precise current drive strength to give the equivalent of 1 billion states. **No software size limit; only practical time constraints.	LOGIC simulates the logical operation of a digital network. Allowed modeling elements are input clocks (generators), standard and clocked logic gates (AND, OR, etc.) and ROMs, RAMs, and PLAs. Standard logic levels are low, high and indeterminate, with checking for spike conditions. To simplify data entry, groups of logic elements may be first defined and later repeated with selected changes.	Part of Highland 2 uses either Tegas or Silos.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

Trimeter Technologies Logic Consultant	Valid Logic Systems Inc. ValidSIM page 4660	Valid Logic Systems Inc. ValidTIME page 4660	Vamp Logicsim
APOLLO	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, Valid SCALDSsystem	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, Valid SCALDSsystem	APPLE
	X X	X X	X X
	X X X X	X X X	X X X
	X X	X X	X X
	X X X X X	X X	X X X X
	X	X	
	X X	X X X	X X X
	20	24	
	41	40	
		ps	
	7,000 to 1,000 std simulation primitives	Unlimited	
	1,000 to 250,000		
	LASAR 6	LASAR 6	
Mentor Graphics' Gen Lib, LSI Logic	AMCC, AMD, AMI, ASEA HAFO, AT&T, Control Data, Digital Equipment, Fairchild, Ferranti, Fujitsu, Harris, Hitachi, Hughes, IMP, IMSC, Intel, LSI Logic, Matra Harris, MEDL, etc.		
Trimeter's Logic Consultant is an expert system-based, complementary CAE tool for ASIC logic design optimization. It allows you to create ASIC logic designs that use fewer gates and/or run faster without changing your current design methodology.	The ValidSIM Logic Simulator is an advanced functional and timing analysis tool designed to help digital engineers produce quality products. Using either engineering workstations or mainframe computers, ValidSIM accelerates design verification, provides powerful debugging tools, and automatically flags timing errors during simulation.	ValidTIME is a timing verifier that automatically checks the timing correctness of digital circuits by performing an exhaustive timing analysis of all signal paths without user input stimuli. ValidTIME automatically verifies every signal path, unlike logic simulators that check only those paths that have been exercised by stimuli.	
The Logic Consultant accepts input logic designs as netlists from Mentor Graphics systems with generic or foundry-specific symbols, as boolean equations or in PLD format.	For complex board designs, ValidSIM takes advantage of Valid's patented ReaChip and RealModel hardware modeling systems. For large designs, Valid offers the Realfast Simulation Accelerator system. Additionally, for ASIC designs, it supports a wide range of pre-lace and route delay estimation features including load dependent delays, process, voltage, and temperature variable delays, and ASIC vendor supplied delay equations.	ValidTIME analyzes the circuit to verify timing restrictions for memory devices, such as latches, registers and RAMs and for any input/output pins. These restrictions include minimum setup and hold times on the data lines, minimum pulse width on clock lines, and maximum skew between edges of a two-phase clock. These are included as part of each library, and you can change these constraints to match your specific IC vendor and add other constraints. * Performs timing analysis without test vectors * Performs reconvergent fan-out analysis * User definable clocks * Models "glitchy" and "glitchless" registers * Documents signal history and case analysis * Lists detected timing violations and circuit behaviors * Fully integrated with all Valid analysis tools	
The Logic Consultant first minimizes the design's logic and evaluates timing constraints. Then, using the expert system technology, the Logic Consultant selects the optimal combination of cells and macrocells from the targeted ASIC library which provide the required logic functionality with the highest performance and/or the least area possible.			
The Logic Consultant's Schematic Analyzer allows you to then quickly estimate propagation delays through selected signal paths, find the longest and shortest delay paths and calculate the associated timing delays of both the high-to-low and low-to-high signal changes.	Post-layout delays can be fed back into ValidSIM. ValidSIM allows selection among minimum, typical and maximum component delays. ValidSIM also provides all of the tools necessary to perform advanced timing analysis with an automatic timing checker built into the libraries. It is supported by extensive model libraries, operates in batch/interactive mode, and does mixed mode simulation.		

Bold face indicates data is provided in the page noted

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)			
Source	Viewlogic Systems	VLSI Technology	Xerox
Tool Name	ViewSim	VTIsim	Expert Logic Simulator
FOR DETAILED DATA SEE:		page 4665	
Tool residence	DEC VAX, IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN	XEROX
Device types supported			
Bipolar	X		X
MOS	X	X	X
GaAs	X		
Hierarchical simulation			
Switch level	X	X	X
Gate level	X	X	X
Functional level	X	X	X
Behavioral level		X	X
Physical model level		X	
Outputs generated			
Truth table	X	X	X
Waveform	X	X	X
Interactivity—During simulation			
Start and restart	X	X	X
Recompile incrementally	X		X
View changing waveforms	X	X	X
Relocate and add probes	X	X	X
Change stimulus	X	X	X
Supports EDIF	X		
Test vector generation language		X	X
Timing verification			
Typical values	X	X	X
Min/Max	X	X	X
Worst-case		X	X
Number of states	28	Infinite	9-logic, 27-timing
Number of primitives	60	Complete VLSI library	50
Resolution (min. ps)	100	0.1 nanosecond	Unlimited
Capacity (gates max.)	2000 primitives	Unknown	250,000
Speed (gate evaluations/sec)	800		1,000
Link to fault simulator (name)		HILO-3	LASAR Version 6
ASIC libraries supported	LSI Logic, Gould AMI.	VLSI Technology Inc.	Intel, Motorola.
Description		VTIsim is a mixed-mode, multi-state simulator which is capable of simulating a mixture of gate-level, behavioral-level and transistor-level models, thus enabling the user to simplify the verification of his design against pre-defined specifications. With VTIsim the user can simulate interactively with immediate textual and graphical feedback, or simulate in the batch mode. Waveforms can be displayed graphically during the simulation and/or plotted from a trace file produced by the simulation.	The Expert Logic Simulator is a verification tool for the logic designs created with Expert Schematics. It is an event driven simulator and supports a range of primitives including gates, MUXs, registers, RAMs, ROMs, PALs, etc. Provided with it is the XDDL design description language for the description of simulation models. It provides a rich set of features for control and debugging. Its direct link with Expert Schematics eliminates the compilation of designs into simulator net lists.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Logic Simulators and Timing Verifiers (Cont'd)

ZyMOS ZyPSIM-AT			
IBM PC/XT/AT			
X			
X			
X X			
X			
X X X			
64			
32			
100			
40,000			
3,000			
Zycad Mach 1000			
ZyMOS SuperCell Standard Cell Library			
<p>ZyPSIM-AT is an IBM PC AT hosted simulated developed for ASIC design. IT is a mainframe-based simulator ported to PCs. By specifying a "guardband" of circuit operating conditions, timing modules within standard cell models can be adjusted for voltage, temperature and processing effects. ZyPSIM-AT also aids in predicting the final die size of a chip based on the network cell list, number of cells in the design, and the process technology selected.</p>			

## DESIGN AUTOMATION—Design Tools

Generic Function	Design Tool Capability		
Front End Design Tools—Fault Simulators			
Source	Aida	Aida	Aldec
Tool Name	Aida Fault Inferencer	Aida Fault Simulator	HASS
FOR DETAILED DATA SEE:			
Tool residence	APOLLO	APOLLO	IBM PC/XT/AT
Fault simulation technique			
Serial	*	X	
Parallel	*		
Concurrent	*		X
Statistical/probabilistic	*	X	
Fault grading			X
Graphic display of undetected faults			X
Display on non-fault-propagating nets			X
Automatic fault collapsing		X	
Automatic test pattern generation	X	X	X
Test pattern conversion for A.T.E.			X
Link to logic simulator	AIDA Logic Simulator	Aida Logic Simulator	Slav
Capacity (max. gates)		1 million gates	40,000
Speed (fault evaluations/sec)			5,000
Description	The Aida Fault Inferencer supports scan design and uses a fast algorithm that performs backward trace inferencing to analyze faults. Th AIDA Fault Inferencer runs a good machine simulation using the AIDA simulation accelerators and determines the state of all nodes for each vector. Fault coverage is found by back-tracing all critical paths from the primary outputs to primary inputs and latch outputs. Any single stuck-at fault that is opposite the good machine state along this path is detected. Based on research this approach has proven to be up to 10 times faster than concurrent fault simulation. * Critical Path Back-tracing	The workstation-based Aida Fault Simulator deterministically evaluates single stuck-at faults for designs that mix scan & non-scan storage elements in either synchronous and asynchronously clocked chips. Using the Aida Co-Simulator Processor, the Fault Simulator can be accelerated up to 5 million gate evaluations per second with a capacity of 1 million gates.	HASS is based on a proprietary logic RISC processor network.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Fault Simulators (Cont'd)

Applicon Logic Analysis	Cadam Digital Fault Simulation	Cadnetix Fault Simulation	Caedent Probabalistic Fault Grading
	IBM MAINFRAME/MINI	Servers, workstations, Analysis Engine	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN
	X	X	X
		X	X
	X		X
	X		
	X	X	
		X	
	CADAT		
	125,000	50,000 Gates	Same as simulator
	Function of CPU	10,000	
Logic Analysis is an integrated logic, timing, and fault simulator for electronic designers. It enables the engineer to perform failure analysis by inserting "stuck-at-0" and "stuck-at-1" faults into the network model. Concurrent fault simulation may be performed to evaluate test vectors and the effects on primary outputs. Logic Analysis may also be used to generate actual test vectors for popular automatic test equipment, ATE, systems.	Cadam offers Digital Fault Simulation, a product which applies sophisticated, computer modeling techniques to the task of testing and analyzing electrical and electronic designs. Digital Circuit Simulation integrates CADAT, a high function integrated, logic, timing and fault simulation package, into the Cadam interactive graphics environment. It allows printed circuit boards and integrated circuits to be tested and debugged in software, providing a fast, cost-effective alternative to prototyping with physical devices.	Cadnetix fault simulation capability is embedded in the Cadnetix Digital Design Environment (Logic Simulator)	PFG is an accurate and cost effective alternate to deterministic fault simulation. Working interactively with any CAE design system via its logic simulator, PFG calculates the overall fault detection probabilities based on how a test vector set affects the controllability and observability of the circuit nodes in a design. PFG requires only a fault-free (good circuit) simulation, from which it produces an estimate of the overall level of fault coverage and an explicit list of undetected faults. PFG uses existing simulator model libraries without modification and supports hierarchical macro-level analysis. Statistical accuracy improves with larger circuits. By supporting behavioral models PFG provides test vector development and fault grading for PCBs and systems. The support of transistor-level models allows PFG to be used with silicon compilation or for full custom design. PFG supports hardware modeling. Design for Testability (DFTA) Analysis further allows the designer to improve circuit testability during the design phase.

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools--Fault Simulators (Cont'd)			
Source	Calma	Case Technology	Control Data
Tool Name	TCAT	CADAT (see HHB Systems)	MIDAS
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, DEC VAX, DEC MICROVAX	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN	CONTROL DATA
Fault simulation technique			
Serial			X
Parallel	X		
Concurrent		X	
Statistical/probabilistic		X	X
Fault grading	X	X	X
Graphic display of undetected faults	X		
Display on non-fault-propagating nets	X	X	
Automatic fault collapsing	X	X	X
Automatic test pattern generation	X	X	X
Test pattern conversion for A.T.E.	X	X	
Link to logic simulator	Texsim/B	CADAT	
Capacity (max. gates)	Circuit dependent	PC: 3000; DEC, SUN: no practical limit	5,000 gates
Speed (fault evaluations/sec)	20,000-30,000	VAX: 2-3K; SUN: 4-5K; PC: 3-400	
Description	<p>TCAT (TEGAS Computer Assisted Testing) is an option to TEX-SIM/B. TCAT has capabilities for testability analysis, fault generation, automatic test generation, and fault simulation. Testability analysis provides a measure of the difficulty of identifying manufacturing defects of an IC during testing. The measure is determined by examining the topology of the circuit and calculating values for controllability, predictability and observability. Fault generation provides stuck-at-one and stuck-at-zero information for fault simulation of the circuit. Equivalent faults are collapsed.</p> <p>Automatic test pattern generation utilizes information produced during the testability analysis to develop input patterns which can detect faults. Fast fault simulation is possible using a multi-word parallel algorithm. Faults detected and undetected are recorded. The simulation can be controlled using detected faults as the control.</p>	<p>CADAT is an integrated logic, timing, and fault simulator for electronic design and test engineers. CADAT is ideally suited for the design of printed circuit boards and ASICs. SSI and MSI components are modeled with conventional software models, while LSI and VLSI components are modeled using the HHB Systems CATS Dynamic Hardware Modeler. CADAT ASIC model libraries can be used to simulate gate array and standard cell devices. CADAT automatically calculates the effects of fanout loading in networks and updates device timing. For board level work, min/max delay simulation can be used to analyze the circuit's sensitivity to variations in component device timing.</p>	Modular Integrated Design Automation System.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Fault Simulators (Cont'd)

Daisy Systems MegaFAULT	ES2/US2 SOLO 1000/SOLO 1200	EXAR HILO-3 (see Genrad)  page 4222	Fairchild FAIRCAD/PFault
Daisy MegaLOGICIAN	APOLLO, DEC VAX, DEC MICROVAX, VAXstation 2000	DEC VAX	CRAY, DEC VAX, DEC MICROVAX, Zycad
	X		X
X	X	X	X
X	X		X
X	X	X	X
X			X
			X
X		X	X
	X	X	
X	X		X
MegaLOGICIAN, Daisy Logic Simulator	Proprietary, SILOS, HILO, CADAT	HILO-3	FAIRCAD (FAIRLOGS)
64,000	12,000	Unlimited	10,000
100,000			
MegaFAULT grades the effectiveness of test patterns in detecting potential manufacturing defects. It provides full function technology independent fault simulation and is hardware accelerated on the Daisy MegaLOGICIAN.	The SOLO fault simulator is an integral part of the SOLO package. It applies faults at user determined levels in the hierarchy. It applies the "stuck-at" class to each transistor node. It also links to powerful fault simulation tools within SILOS, HILO and CADAT.	HILO-3 as a digital design environment embraces a very powerful fault simulator. HILO3 is an integral part of EXAR design automation system.	Fault simulation informs the designer if, by inspecting the design's output pins, manufacturing faults modeled as "stuck-at" faults can be detected. To ensure test vectors screen potential manufacturing defects (short, open, pin hole, etc.) Fairchild provides access to a Cray 1-S Supercomputer and a powerful fault simulation program. In FAIRCAD, fault simulation is divided into two steps: controllability and observability. Controllability, invoked by a single command in the test sequence, determines the percent of internal nodes being toggled by the vectors provided. In short, this analysis shows how effective the test vectors are in controlling the faults. Observability, which is accomplished using the parallel fault simulator on the Cray 1-S Supercomputer, propagates the faults to primary outputs; this determines if the faults are detectable.
MegaFAULT provides fast, convergent simulation that includes statistical coverage analysis, incremental and exhaustive modes. Users can analyze MegaFAULT results with a series of reports including both histograms and tabular reports.			
MegaFAULT and MDLS (logic simulation) share a common database. No model or netlist conversion is required, thereby saving user time.			

Bold face indicates data is provided in the page noted

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Fault Simulators (Cont'd)			
Source	FutureNet (Data I/O)	FutureNet (Data I/O)	Gateway Design Automation
Tool Name	DASH-FAULTSIM	PLDtest	BITGRADE
FOR DETAILED DATA SEE:	page 4651	page 4651	
Tool residence	IBM PC/XT/AT	DEC VAX, IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN
Fault simulation technique Serial Parallel Concurrent Statistical/probabilistic	X	X	X
Fault grading	X	X	X
Graphic display of undetected faults	X		
Display on non-fault-propagating nets	X		
Automatic fault collapsing	X	X	X
Automatic test pattern generation	X	X	
Test pattern conversion for A.T.E.	X	X	
Link to logic simulator	DASH-CADAT-Plus		
Capacity (max. gates)	12,500 w/Design Kits; board level unlim.	Programmable logic devices only	200,000 w/ 50 MB virtual memory
Speed (fault evaluations/sec)	1,000	Seconds to minutes per device	
Description	DASH-FAULTSIM uses a mathematical "stuck-at-one/stuck-at-zero" fault model to determine how well test programs detect all possible circuit faults. It identifies the percentage of the errors covered by the test programs and identifies any areas that are not covered. DASH-FAULTSIM's full concurrent functional simulation technique is one of the fastest available. It follows the chain reaction through the circuit that is caused by any particular fault. DASH-FAULTSIM also includes a statistical sampling feature that gives the user the ability to quickly grade a random cross-section of possible faults.	PLDtest is an automatic test vector generator for programmable logic which also performs fault grading to test the logical function of a device. It examines user-supplied test vectors along with device information to determine how many potential faults the test vectors will detect. The inputs for each test vector are applied to the design, then PLDtest records the state of each fuse, AND gate, OR gate, and register output. After this simulation, PLDtest traces a path backward from each output pin to determine which faults are detectable from that pin. The designer can use this information to write additional test vectors, or he can let PLDtest generate additional test vectors to check for all stuck-at-one and stuck-at-zero faults.	BITGRADE is a high performance fault-simulator designed specifically for evaluating the effectiveness of self-testing digital circuits. BITGRADE provides a high level description language that allows the user's self-test scheme to be specified in terms of stimulus generators and response accumulators. BITGRADE grades the test patterns generated by built-in self-test logic, generates diagnostic information, and allows the user to select points in time at which the response is externally observed.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Fault Simulators (Cont'd)

Gateway Design Automation STATGRADE	Gateway Design Automation TESTGRADE	GE Solid State Division MIMIC Fault Simulator page 4235	Genrad HILO-3
APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN	APOLLO, CONTROL DATA, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/ MINI, Alliant	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN	APOLLO, DEC VAX, DEC MICROVAX, HEW- LETT-PACKARD, IBM MAINFRAME/MINI, RIDGE, NEC EWS4800
X	X	X	X X
X	X	X	X
X	X	X	X
	X	X	X
		X	X
Simulator inc., also VERILOG/ VERILOG XL	Simulator inc., also VERILOG/ VERILOG XL	MIMIC	HILO-3
200,000 with 50 MB virtual memory	200,000 w/ 50 MB virtual memory	Limited by CPU 11,000 on IBM 3083	Machine dependent
STATGRADE is a statistical fault analysis software package that provides complete digital circuit fault coverage as well as a powerful logic simulator. STATGRADE covers all potential circuit faults, including those that occur at the inputs of circuit elements. With STATGRADE, it is now possible to estimate very quickly the total fault coverage of a test vector set. In addition to providing total fault coverage, STATGRADE offers interactive logic simulation that can be used with one of the most comprehensive IC model libraries. STATGRADE is a mixed-mode simulator that provides primitives for functional, gate and switch-level simulations. Designed to be machine independent, STATGRADE runs on virtually all major computers used in circuit design: from workstations to mainframes.	TESTGRADE is a very high performance interactive logic and concurrent fault simulator that combines gate and switch level simulations and is targeted for VLSI complexity random sequential digital logic. TESTGRADE has been benchmarked at speeds of over two orders of magnitude faster than competitive products. TESTGRADE employs the latest simulation techniques, including many proprietary algorithms, to provide a highly efficient and powerful fault simulation capability for single stuck faults as well as for CMOS stuck-open faults. It simulates random sequential logic networks composed of TTL and/or MOS primitives, including the bi-directional pass devices and resistive MOS devices. TESTGRADE also provides very efficient simulation for random sequential logic networks containing such high-level primitives as multi-port RAMs and multi-port ROMs. The 15-value simulator provides the resolution needed for effective simulation of dynamic MOS.  Fault simulation can be performed in an incremental manner with no loss of data between incremental steps. Fault sampling is provided to facilitate quick experimentation. A powerful functional language is provided for the designer to concisely specify highly complex test programs for fault simulation. TESTGRADE includes an automatic test pattern generation capability that generates effective tests under user guidance.	GE's Comprehensive Network Simulator, MIMIC, has fault simulation capabilities. During fault simulation, MIMIC compares the response of the good-logic circuit with the response of the faulty circuit. A fault is detected if at least one output of the faulty circuit differs in a known manner from the corresponding output of the good-logic circuit, when the logic outputs of the network have stabilized. That is, the good output is 0 and the fault output is 1, or vice versa. Also, a fault is potentially detected when at least one fault output is unknown (X), while the corresponding good output has a known value.	The HILO-3 Universal Logic Simulation System is an integrated set of software tools for logic verification and fault simulation in digital circuit design. The system's hierarchical framework supports today's design methodologies in full-custom and semi-custom integrated circuit, printed circuit board and system design. The HILO-3 system performs rapid, effective design and test verification for thorough debugging of logic behavior before the prototype stage.  The HILO-3 fault simulator uses the proprietary Parallel Value List (PVL) technique for fast, efficient fault simulation of circuits modeled at the gate or functional (behavioral) level. Numerous fault structures, including stuck, open, drive and short are available to accurately model technology dependent fault modes.  The HILO-3 fault simulator allows the engineer to take an incremental approach to test development, utilizing only previously undetected faults as new stimulus is added. A statistical fault selection is available for quick evaluation of test data.  A diagnostic fault dictionary offers a wide variety of fault reporting options.

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Front End Design Tools—Fault Simulators (Cont'd)			
Source	Harris Semiconductor	Hewlett-Packard	HHB Systems
Tool Name	CADAT (see HHB Systems)	HILO-3 (see Genrad)	CADAT 6.0
FOR DETAILED DATA SEE:	page 4246		
Tool residence	APOLLO, DATA GENERAL, DEC VAX, ELXSI, IBM MAINFRAME/MINI, IBM PC/XT/AT, MASSCOMP, PYRAMID	HEWLETT-PACKARD	APOLLO, DATA GENERAL, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, IBM MAINFRAME/MINI, IBM PC/XT/AT, MASSCOMP
Fault simulation technique			
Serial	X		
Parallel		X	
Concurrent	X	X	X
Statistical/probabilistic	X		X
Fault grading	X	X	X
Graphic display of undetected faults			
Display on non-fault-propagating nets			
Automatic fault collapsing	X	X	X
Automatic test pattern generation	X		X
Test pattern conversion for A.T.E.	X	X	X
Link to logic simulator	CADAT	HILO-3	CADAT
Capacity (max. gates)	No defined limit; dynamic allocation	Depends upon swap space and disc space	Dependent on host machine's memory
Speed (fault evaluations/sec)			1000 on VAX 750
Description	The CADAT fault simulator identifies potential failure modes of the network by inserting "stuck-at-1" and "stuck-at-0" faults into the network model. The faulty network is re-simulated and its outputs are compared to the fault-free model. If different behavior is observed, the fault is considered "detected", meaning that a bad device would be caught and identified by production test equipment. A concurrent algorithm is used.	Uses parallel value list.	CADAT 6.0 is an integrated simulation environment, supporting logic, fault and worst case timing. The CADAT simulation system is a virtual breadboard that allows a design engineer to debug logic and optimize circuit performance without building a prototype. Test engineers can work with the same CADAT description to develop test vectors. CADAT is ideal for the design of PCBs or ASICs. SSI and MSI components are modeled with CADAT's gate and functional models. LSI and VLSI can be modeled either behaviorally or physically with the CATS modeler. ASIC libraries can be used to simulate gate arrays and standard cell devices. Delay changes caused by fanout loading are automatically calculated by CADAT. Delays can also be calculated from the physical layout and back-annotated into the simulation. Minimum-pulse-width and setup/hold violations are reported to the designer. For PCB design, a worst case timing simulation can be performed to analyze the circuit sensitivity to variations in component device timing.



DESIGN AUTOMATION—Design Tools

Design Tool Capability			
Front End Design Tools—Fault Simulators (Cont'd)			
IKOS Systems IKOS 800	Intergraph HILO-3 (see Genrad)	Matra Design Systems COFIS	Mentor Graphics QuickFault
IBM PC/XT/AT	DEC VAX, DEC MICROVAX, Intergraph Inter- Pro 32C, InterAct 32C	IBM MAINFRAME/MINI	APOLLO
X	X X	X	X
X	X	X	X
	X		X
	X	X	X
	X		
	X	X	X
IKOS 800	HILO-3	ARCIS	QuickSim
64,000	No practical limit	2,500 on PC/AT, 10,000 on VAX 11/785	100,000
			2,000
	<p>The HILO Universal Logic Simulation System includes a hierarchical Hardware Description Language (HDL) for specifying logic designs, a Waveform Description Language (WDL) for describing circuit stimuli, a fault-free logic simulator, a fault simulator, a test generator, and a component library that contains over 3000 devices.</p> <p>The HILO event-driven selective-trace simulator includes a 5-strength, 15-value logic state algorithm for accurate modeling of a wide range of device technologies such as TTL, ECL, Schottky, CMOS, NMOS, PMOS, STL, IIL. In fault simulation, a new Parallel Value List (PVL) algorithm combines the advantages of concurrent and parallel algorithms, providing fast execution and low memory overhead.</p> <p>HILO outputs can be post-processed to various pieces of automatic test equipment.</p>		<p>QuickFault is a concurrent fault simulator. It is used to analyze the effectiveness of test patterns in detecting simulated faults. Like all members of the QUICKSIM family of simulators, QuickFault shares a common user interface and a feature set including mixed-mode, hierarchical, 12-state simulation.</p>

DESIGN AUTOMATION

# IC MASTER

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Fault Simulators (Cont'd)			
Source	National Semiconductor	Plessey	Racal-Redac
Tool Name	Design Automation System	CLASSIC/FAULTS	REDSIM CADAT
FOR DETAILED DATA SEE:	page 4294		
Tool residence	IBM MAINFRAME/MINI	DEC VAX	IBM PC/XT/AT, with co-processor board
Fault simualtion technique			
Serial		X	
Parallel		X	
Concurrent	X		X
Statistical/probabalistic			
Fault grading	X	X	X
Graphic display of undetected faults		X	X
Display on non-fault-propagating nets			
Automatic fault collapsing	X		X
Automatic test pattern generation			
Test pattern conversion for A.T.E.	X	X	X
Link to logic simulator	HILO-3	Classic	Redsim Cadat
Capacity (max. gates)	Up to 100,000	100,000	Unlimited
Speed (fault evaluations/sec)	Complexity dependent	Design dependent	600 events/sec
Description	For the design of National Semiconductor gate arrays and standard cells. National uses Genrad's HILO-3 for fault simulation.		



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Fault Simulators (Cont'd)

Racal-Redac VISULA CADAT	SDA Systems SILOS Interface	SDA Systems TestEdge	Silicon Compiler Systems Lsim
APOLLO, DEC MICROVAX	APOLLO, DEC VAX, DEC MICROVAX, MASSCOMP	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC MICROVAX, SUN
X	X X	X X	X X
X	X	X	X
X	X	X	
		X	X
X	X	X	
X			
X	X	X	X
VISULA CADAT	SILOS	SILOS	Lsim
Unlimited	Machine dependent	Unlimited	Unlimited
600 events/sec	N/A		
	<p>SILOS Fault Simulator available with SDA's Graphics Interface offers access to SILOS, the production-proven fault simulator from SimuCad, via its own friendly graphical fault-simulation interface. SILOS uses state-of-the-art algorithms that can simulate a circuit at the switch, logic and functional levels. It employs 12 logic states to accurately model bi-directional MOS transistors. SILOS and SDA's graphical interface allow engineers to develop test vectors and grade fault coverage on workstations, without tying up expensive time on mainframes.</p>		<p>Lsim is an interactive mixed mode simulator providing mixed degrees of freedom in both the functional and the timing domain. Lsim accepts as input a hierarchical circuit description consisting of functional modules of circuit elements and their connections. Functional modules can range in complexity from transistors to microprocessors. Module development parallels generator development performed by SDL's Generator Development Tools, providing the same degree of flexibility in the simulation domain that generators provide in the layout. Users have the option of simulating their generator layouts at the transistor level or writing their own functional module for the generator using the functional module compiler language- Mc.</p>

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Front End Design Tools—Fault Simulators (Cont'd)			
Source Tool Name FOR DETAILED DATA SEE:	Simucad SILOS	Tangent Systems TANTEST	Tektronix CAE Systems HILO-3 (see Genrad) page 4658
Tool residence	APOLLO, DATA GENERAL, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/ MINI, MASSCOMP	APOLLO, DEC VAX, DEC MICROVAX, Intergraph InterPro 32	APOLLO, DEC VAX, DEC MICROVAX
Fault simulation technique Serial Parallel Concurrent Statistical/probabilistic	X	X	X
Fault grading	X	X	
Graphic display of undetected faults			X
Display on non-fault-propagating nets			X
Automatic fault collapsing	X	X	X
Automatic test pattern generation		X	X
Test pattern conversion for A.T.E.			
Link to logic simulator	SILOS Logic Simulator (included)	HILO-3	HILO-3
Capacity (max. gates)			Limited only by disk size
Speed (fault evaluations/sec)			
Description	<p>SILOS features a combined logic/switch level simulator for electronic circuits. It performs logic and fault simulation in both interactive and batch mode. Data primitives include network-level devices, logic-level gates, as well as high-level functions. Inputs to a network may be specified as individual clocks or as binary/hexadecimal tables. SILOS uses a unique 12 + 5 state concept which allows accurate modeling of bidirectional logic, wired-ORs, charge sharing and node charge decay.</p> <p>SILOS event-driven logic simulation can be performed with zero or finite delays. Users can simulate up to a timepoint, look at arbitrary output, then continue the simulation. SILOS can generate summary tables of all node states, node spikes, unknown states and activity levels. Automatic network error checking and initialization, complete report generation facilities for both logic and fault simulation, and graphical output of simulation waveforms are provided. Sentry tester interface outputs can be requested.</p>	<p>Automatic synthesis of circuitry for serial-scan testing and automatic test pattern generation software. Solves testability problem for standard cell and gate array application specific IC design.</p>	<p>HILO-3 Fault Simulator is an option of HILO-3 Logic Simulation System. The fault simulator allows an engineer to evaluate how effectively a given set of test patterns can detect specific types of manufacturing defects within the design. The simulator's Parallel Value List (PVL) algorithm provides fast, memory-efficient simulation. The fault simulator induces faults, then traces the effect of each throughout the circuit to determine if it is detectable on the output. Knowing precisely which faults have not been detected, the engineer revises the test pattern set until it produces the fault coverage desired. New fault classes and other enhancements for accurate simulation of technology-dependent and functional models are included.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Front End Design Tools—Fault Simulators (Cont'd)

Teradyne LASAR Version 6	Valid Logic Systems Inc. LASAR 6 (see Teradyne) page 4660	Viewlogic Systems PFG	
DEC VAX, DEC MICROVAX, Valid, Teradyne DATAServer Sim. Engine	DEC VAX, DEC MICROVAX, Valid SCALD- system	DEC VAX, IBM PC/XT/AT	
X	X	X	
X	X	X	
X	X		
X	X		
X	X		
Lasar Version 6	ValidSIM		
500,000			
20,000			
	LASAR 6, developed by Teradyne, Inc. is an advanced fault simula- tion system for digital circuits. It is used for test pattern grading and test program generation for de- vices and boards. It is fully inte- grated with Valid's design analysis tools, with netlister interface and Realchip support on VAX and MicroVAX II.		

DESIGN AUTOMATION—Design Tools

Generic Function

Design Tool Capability

Physical Layout Tools—Circuit Board

Source	Applicon	Aptos Systems	Augat
Tool Name	Interactive/Automatic Layout	AUTOTOOLS	QWIKCHECK
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, DEC MICROVAX	AT&T, HEWLETT-PACKARD, IBM PC/XT/AT, Compaq 386	IBM MAINFRAME/MINI
Device technologies			
Through hole mount	X	X	X
Surface mount	X	X	X
Hybrid	X	X	
ECL		X	X
Double sided boards	X	X	X
Related interconnect technologies			
Multiwire/Microwire	X		
Wire wrap		X	X
Strip line			
Placement			
Manual	X	X	X
Interactive	X	X	
Fully automatic	X		
Routing			
Manual	X	X	
Interactive	X	X	
Fully automatic	X	X	
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)			
Electrical rule checking			
Batch mode	X	X	
On-line (Interactive)			
Via minimization	X	X	
Priority routing of critical nets	X	X	
Layout parameter extraction			
PC board physical parameters			
Board size (max. in. x in.)	No limit	60 x 60	24" X 24"
Board density (max. components)			.3125 sq.in.
Nets (max.)		2000	No limit
Min. trace pitch (mils)	1	1 mil	6
Number of layers (max.)	32	50	10
Links to CAM	Gerber photoplotter, drill, profile.		
Description	<p>Applicon provides both an Interactive Layout Editor and a fully Automatic Layout package for PCB design. The capabilities include handling multi-layer boards, handling a variety of technologies including surface mount, providing rats nest connections with line-of-sight aids, gate or pin level swapping, rip up and reroute, shove aside, and a comprehensive set of electrical and design rules checks.</p> <p>The layout packages are integrated with a complete set of manufacturing capabilities including documentation, photoplotting, and NC drilling. In addition, the layout packages are integrated with a complete set of mechanical design, analysis, and manufacturing packages. This allows the PCB designer to use finite element modeling techniques to analyze stress characteristics of the board, use a solids model of both the board and its packaging for visualization or interference checking, or use an NC machining package to manufacture a mold for an injection-molded enclosure.</p>	<p>Aptos Systems now offers a new three-pass auto router, AUTOTOOLS. Running on the IBM-AT, this system operates with data bases for single or multi-layer designs created by RGRAPH, Aptos' front-to-back CAE software. Ported from a mini-computer to run under MS-DOS, this system does not require an expensive co-processor card or UNIX to provide big-system results.</p> <p>Aptos has selected three algorithms for use in its router: a memory router, a strategy or pattern router, and an exhaustive maze router. The engineer can use these three simultaneously or in succession to achieve a final design that combines economy, functionality, and manufacturability.</p>	<p>QWIKCHECK checks for errors in a FutureNet Schematic Database and extracts the Pin One positions for all components placed by QUIKDRAW. WRAPID also supports Unilayer II.</p>



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Physical Layout Tools—Circuit Board (Cont'd)**

Augat QWIKDRAW	Augat WRAPID	Automated Systems PRANCE	Automated Systems PRANCE/SIGMA REMOTE
IBM PC/XT/AT	IBM PC/XT/AT	IBM MAINFRAME/MINI	IBM PC/XT/AT, Or via IBM 5000 or Megatek 3344 wksta.
X X X X	X X X X	X X X X	X X X
X	X	X	X
X	X	X X X	X X
X X		X X X	X
		X X X	X
X	X	X X	X X
		X X	X X
		X	X
		X	X
		X	X
24"x24" .3125 sq.in./ICE No limit 6 10	24"x24" .3125 sq.in./ICE No limit 6 10	No limit No limit No limit 1 20	No limit No limit No limit 1 20
		Plotters: HP, Gerber, Optrotech, Eocomm, Benson, Calcomp. NC Drill: Trndril, Excellon. NC Test: Mania, Circuit-Line, DITMCO, Custom.	Plotters: HP, Gerber, Optrotech, Eocomm, Benson, Calcomp. NC Drill: Trndril, Excellon. NC Test: Mania, Circuit-Line, DITMCO, Custom.
QWIKDRAW augments the Case Technology schematic design system or Control Data's CYBER-NET*EXPRESS Electronic Designer workstation to allow for component placing and the transfer of databases from the engineer's workstation to Augat's PWB manufacturing facility. The engineer may then choose from five manufacturing technologies: 1) wire-wrap, 2) Unilayer II, 3) stitch-wire, 4) Multilayer, or 5) Augat Microtec's fine-line polyimide multilayer. The designer starts with the schematic drawing created under the schematic editor. The designer then uses the Augat-supplied symbols of boards and components to make an assembly drawing. Augat's VAX extracts the physical interconnection data for manufacturing. QWIKDRAW can now be used to implement in printed wiring board technology designs captured on workstations from P-CAD, Case Technology, FutureNet, and Control Data's CYBER-NET*EXPRESS. QWIKDRAW also includes their own unique form of interconnection technology, Unilayer II.	Engineers use WRAPID to make assembly drawings on their FutureNet DASH workstations and to quickly analyze the data from their schematic drawing and assembly drawing for errors. The package also includes Augat's databases of PWB geometries. WRAPID databases are transmitted to Augat's VAX where they are further analyzed and converted to CAD/CAM databases necessary for manufacturing PWB's. WRAPID also includes their own unique form of interconnection technology, Unilayer II.	PRANCE (Placement, Routing and Numerical Control Editing) is ASI's proprietary PWB design software. PRANCE also resides on IBM mainframe computers in ASI's east coast and west coast design centers. ASI also fabricates multilayer boards in its corporate offices. ASI is Mil 55110-D certified. CAE inputs to Prance: Daisy, Valid, Mentor, EDMS, Tegas. Prance/PCDI offers CAE back annotation.	Allows remote users to interactively access PRANCE on IBM Mainframe over telecommunications lines.

# IC MASTER

## DESIGN AUTOMATION—Design Tools

### Generic Function

### Design Tool Capability

### Physical Layout Tools—Circuit Board (Cont'd)

Source	B&C Microsystems	Bishop Graphics	Bishop Graphics
Tool Name	PCB/DE	Pathfinder	Quik Circuit Version 4.2
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	IBM PC/XT/AT	APPLE
Device technologies			
Through hole mount	X	X	X
Surface mount	X	X	X
Hybrid	X	X	X
ECL		X	X
Double sided boards	X	X	X
Related interconnect technologies			
Multiwire/Microwire		X	X
Wire wrap	X	X	X
Strip line		X	
Placement			
Manual	X	X	X
Interactive	X		
Fully automatic			
Routing			
Manual	X	X	X
Interactive	X	X	
Fully automatic		X	
Design rule checking			
Batch mode	X		
On-line (Interactive)			
Electrical rule checking			
Batch mode	X		
On-line (Interactive)			
Via minimization			
Priority routing of critical nets		X	
Layout parameter extraction	X		
PC board physical parameters			
Board size (max. in. x in.)	Unlimited	Unlimited board size-interactively	32" x 32"
Board density (max. components)	Unlimited	Unlimited	Board size limit
Nets (max.)	Unlimited	Unlimited	
Min. trace pitch (mils)	Unlimited	.001" interactively, .00625" Autorouter	1
Number of layers (max.)	Unlimited	Unlimited interact., 16 layers Autoroute	No limit
Links to CAM	Gerber format output capability. Drill tape schedule generation.	Gerber Photoplotter, or pen plotter	Gerber photoplot. Information can be transmitted over modem to Bishop.
Description	<p>Running on the IBM XT-AT and compatibles, the PCB design package from B&amp;C Microsystems is a customized printed circuit layout environment for Autodesk's AutoCAD system. PCB/DE facilitates efficient and high quality printed circuit board layout designs of boards with up to 15 internal layers. (Additional layers can be added to the environment manually). Layout takes place on assigned layers (FABDRAWING, PAD-MASTER, COMPONENT SIDE, NONCOMPONENT SIDE, INTERNAL1-5, SILKSCREEN). Each layer has its own menu dedicated to the specific tasks associated with it. Size A, B and C frames are offered for each layer for proper artwork documentation.</p> <p>An extensive shape library containing virtually all pad patterns and silkscreen shapes is provided (DIPs, SIPs, TOs, DB connectors, analog devices, discretes, etc.). Pad patterns and associated silkscreen shapes are picked from the menu and placed (dragged) with the mouse. Feedthroughs are inserted automatically on the PAD-MASTER.</p>		
		A powerful CAE/CAD software package for PCB design and layout (end-to-end solution) including schematic capture and an optional autorouter with mainframe performance (32-bit) featuring unlimited layers, top/bottom views for SMT, Gerber output, fineline routing, mirroring, sophisticated routing algorithms for less than \$5,000.	<p>With Quik Circuit, a designer enters the PCB layout on the Apple Macintosh computer CRT screen using a mouse as the primary input device. The PCB layout can be used, edited and modified as many times as required until the desired result is obtained. Check prints and final drawings can be made on either Apple's Image-writer printer or in color on an optional Bishop-supplied pen plotter. To facilitate board fabrication, Bishop has a CAM network of printed circuit board fabricators equipped to produce boards from designs generated on Quik Circuit systems.</p> <p>Quik Circuit's upgraded version 4.2 includes the addition of two additional font sizes and 14 more storage locations, (palette items), bringing the total to 35 each of pads and pattern locations. Quik Circuit now supports the 1024 x 1024 pixel high resolution monitors, and allows the designer to pick new menu selections while redraws are occurring. Three versions of the program are now available: layout only \$95; layout &amp; print \$395; and layout, print and pen plot \$525.</p>

Bold face indicates data is provided in the page noted



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Circuit Board (Cont'd)

Cadcam Interactive PRANCE	Cadcam IPC	Cadnetix CDX-75000XP Route Engine III	Cadnetix Route Editor
IBM MAINFRAME/MINI	IBM MAINFRAME/MINI	Cadnetix proprietary hardware	Cadnetix CDX Series Workstations
X X X X	X X X X	X X X X	X X X X
X	X	X	X
X	X		X X X
X X X	X X X		X X X
X X	X X	X	X X X
X X	X X	X	X X
X X	X X	X	X X
X	X	X	X
X	X	X	X
X	X		X
Unlimited, bounded by grid	Unlimited, bounded by grid 2,000 20,000,000 .0001 (.0000001 inches) 20 wiring + power & ground planes	34" x 24" No limit No limit 1 mil 24	24" X 34" No limit No limit 1.0 24 trace, 24 drafting
	Auto insertion, drill output, auto test equipment, photoplotting, CIM database, N/C routing.		Universal Axial Lead VCD Insert and Sequencer; Universal DIP Insert; Panasonic Pick and Place; HP 3065 Tester; Genrad 2270; Dynapert Pick and Place; Dynapert, etc.
A comprehensive package of high function Design Automation tools providing the truly automatic solution to printed circuit board design and manufacturing. Ideal for dense two-layer or multilayer boards, or in situations where PCB design occurs alongside mechanical design. Features: IBM Mainframe power plus color; optimally places all components, sets the industry standard for automatic routing; highly interactive placement and routing aids; on-line/off-line design rule checking; large supplied library may be interactively expanded or modified; and, extensive automatic manufacturing outputs.	ECL router. Variable routing. Place at any grid. Auto generation of assemblies, silk screens, solder masks, drill planes, etc. Off grid router. Geometric tolerance check. Common database with mechanical design.	The CDX-75000XP Route Engine III is 100% automatic router using a true multilayer rip-up and reroute algorithm. The Route Engine III is based on the MC68020 processor, operating in parallel with high speed bipolar processors and can address up to 16 MB of dual-port RAM, accomodating extremely large boards of 700 ICs and greater. Using a microcoded multilayer routing algorithm, Route Engine's performance is significantly improved over "layer-pair" routers in general use. The Route Engine III includes Cadnetix' software-selectable Flexible Field routing algorithm. It addresses a variety of new PCB layout problems that are appearing more frequently as boards become denser, and surface-mount devices, PGAs and other high pin-count technologies become more commonplace.  A network resource (via Ethernet), the Route Engine III also routes multiple trace widths simultaneously, routes high-speed signals in proper daisy-chain order without stubs, and allows the user to set signal routing priority attributes.	

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Circuit Board (Cont'd)			
Source	Calay Systems	Calma	Case Technology
Tool Name	Design Automation Series	BOARD Series	CT2400
FOR DETAILED DATA SEE:			
Tool residence	DEC LSI-11	APOLLO	DEC VAX, IBM PC/XT/AT
Device technologies			
Through hole mount	X	X	X
Surface mount	X	X	
Hybrid			
ECL	X		
Double sided boards	X	X	X
Related interconnect technologies			
Multiwire/Microwire	X	X	X
Wire wrap		X	X
Strip line			
Placement			
Manual	X	X	
Interactive	X	X	X
Fully automatic	X	X	
Routing			
Manual	X	X	
Interactive	X	X	X
Fully automatic	X	X	
Design rule checking			
Batch mode	X	X	
On-line (Interactive)	X	X	
Electrical rule checking			
Batch mode	X	X	
On-line (Interactive)	X	X	
Via minimization	X	X	
Priority routing of critical nets	X	X	
Layout parameter extraction			X
PC board physical parameters			
Board size (max. in. x in.)	32 X 32	24" x 24"	D-size drawing
Board density (max. components)	62,000	750 equiv. ICs	200 + depending on memory
Nets (max.)	32,000	5000	200 depending on memory
Min. trace pitch (mils)	8	2	
Number of layers (max.)	8 plus 8 document. Unlim. power/ground.	32	128
Links to CAM	All Gerber photoplotters. Most drilling machines. Most insertion machines. Bareboard testers. In-circuit testers.	Standard aperture or laser photoplotter, NC Drills, NC insertion, bare board test, line and raster plotters.	
Description	The Calay DA Series of workstations for PCB design are full capability and high performance systems. Running on a standard hardware platform with proprietary hardware accelerators, they provide fast, efficient PCB layout design and routing capability. The systems' features include hardware autorouters, which can achieve a 100 percent routing solution, component placement tools, specially designed software to handle Surface Mounted Devices, on-line design rule check, parts library, automatic design optimization for enhanced manufacturability, and interactive editing with high resolution color graphics, a hardware pan and zoom. Also offered in the systems is complete output documentation and postprocessing capabilities for manufacturing. Th DA series handles large, complex, dense, multi-layer board designs that can include a mix of surface mount and through-hole mounted components, and analog, digital, and ECL circuitry.	The BOARD Series consists of three packages: BOARD Designer, BOARD Editor Plus, and BOARD Expediter. BOARD Designer, the hub of the Series, provides full functionality required for PCB design. This includes schematic capture; board geometry; packaging and pin assignment; autoplacement; interactive and autorouting; interactive editing, and correct-by-construction methodology. In addition, BOARD Designer has a parameter-driven constructive router, a local ripup and retry router, and photoplotter and NC Drill output capability. The Designer can function as a stand alone design system, or as a master node supporting several BOARD Editor nodes.  BOARD Editor Plus provides the same design and layout capabilities found in the BOARD Designer, with the exceptions of routing and CAM capabilities. It is designed for use as a low-cost Apollo DN3000C node. BOARD Expediter is a high-performance routing node. The operator can offload computing intensive tasks from either the BOARD Designer or BOARD Editor, freeing them for interactive work.	Case Technology's CT2400 Layout system works as an integral part of the company's CAE products for the IBM PC. The PCB Layout program provides autoplacement, autoplacement and rats nest capabilities. Users can employ features such as intellignet rubberbanding of thick and 45-degree lines to route traces to the appropriate physical location. Any number of routing layers can be used, limited only to the amount of memory available on the IBM PC. During PCB layout, the program's interactive design rule checker points out any rules violations, unlike layout systems which perform this function only after the layout is completed.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Circuit Board (Cont'd)

Case Technology CT2500	Case Technology Vanguard Stellar System	Compact Software AUTOART	Computervision AUTOBOARD
DEC VAX, IBM MAINFRAME/MINI	AT&T, CONTROL DATA, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, NEC PC, SUN	APOLLO, DEC VAX, DEC MICROVAX, HEW-LETT-PACKARD, IBM MAINFRAME/MINI, IBM PC/XT/AT, RIDGE, SUN	Computervision
X	X X		X X X
X	X		X
X X			
X	X X X		X X
X X	X X		X X
	X		X X
	X		
	X		X
X			
D-size drawing 200 + depending on memory 200 depending on memory 128	64 x 64 2500 unlimited 1 256		39" x 39"  30
			Gerber and Quest photoplots as well as plots from Benson, Calcomp, Versatec, and H-P. Marconi Auto-Check tester. CNC for Excellon, Posalux, Sted & Mey, Siemens.
Case Technology has added an automatic PCB router to the company's Vanguard Design System of CAE/CAD tools for the IBM PC, MicroVAX and VAX. Unlike most other auto routers, the Case CT2500 router allows users to deal easily with special technologies by utilizing an interactive command and menu structure. This avoids many of the drawbacks of completely batch-oriented systems. The CT2500 gridless auto router also assures use of the shortest point-to-point connections by allowing traces to connect to vias along the route. Further, most routing programs consider only pairs of PCB layers when assigning vias; however, the CT2500 considers as many as 20 layers at once to create a more uniform layout. Forty-five degree line routing also helps the router achieve cleaner and more complete layouts compared to strictly orthogonal routing.	Comprehensive layout system with auto packaging, auto placement, auto routing, pin and gate swapping, on-line and post processor DRC, Gerber and Excellon options.	AUTOART is an interactive graphics program for designing hybrid layouts. AUTOART can be used in conjunction with its companion program, SUPERCOMPACT, to provide automatic mask generation from an electrical design as specified in SUPERCOMPACT's design language. AUTOART automates the production of artwork and drives many kinds of CAD mask-making machines. The designer can use NODE control commands to edit the design using microwave terminology. The displayed layout is redrawn as changes are requested. Final adjustments, including the addition of registration targets, circles, lettering vias, and bias lines, can be made before sending the design to mask-making hardware.	Autoboard is a UNIX-based software application program developed for CADDStation, Computervision's 68020-based, 32-bit workstation. Autoboard addresses the back-end of the PCB design process—PCB layout—but is tightly integrated with Schematic Design, Computervision's schematic capture tool. Accepting netlist data transferred automatically from Computervision's Schematic Design software, Autoboard provides tools for automatic creation of board outlines (board designs as large as 39" x 39"); automatic and interactive placement; automatic and interactive routing; interactive editing; and post-processing for ECAM. Especially notable is a router based upon a repositioning algorithm. Autoboard's router will actually push-aside completed traces to make new connections. A design rules checking function is active to ensure design criteria are adhered to. Autoboard supports advanced PCB technologies including: surface mount technology, and high-density digital and analog designs.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Circuit Board (Cont'd)			
Source	Computervision	Control Data	Daisy Systems
Tool Name	CADDS 4X	PEPPER	BOARDMASTER
FOR DETAILED DATA SEE:			
Tool residence	Computervision	CONTROL DATA, CRAY, IBM PC/XT/AT	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, Daisy LOGICIAN 386/Personal LOGICIAN 386
Device technologies			
Through hole mount	X	X	X
Surface mount	X	X	X
Hybrid	X	X	
ECL		X	X
Double sided boards	X	X	X
Related interconnect technologies			
Multiwire/Microwire	X		X
Wire wrap	X		X
Strip line	X		
Placement			
Manual			X
Interactive	X	X	X
Fully automatic		X	X
Routing			
Manual			X
Interactive		X	X
Fully automatic	X	X	X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Via minimization	X	X	X
Priority routing of critical nets	X	X	X
Layout parameter extraction		X	X
PC board physical parameters			
Board size (max. in. x in.)	50 X 50	59" X 38.75"	32" X 32"
Board density (max. components)	1500 ICs, 800 discretes	512	14,000
Nets (max.)	32,000 +	1,000	14,000
Min. trace pitch (mils.)		Not limited	
Number of layers (max.)	20	20 +	255
Links to CAM	Photoplotters, dot matrix printers, pen plotters, NC drilling, NC insertion.	Gerber photoplot, Excellon NC drill, others.	Gerber Photoplotters, Excellon CNC drill, Universal auto insertion, Calcomp and H-P pen plotters, Versatec electrostatic plotters.
Description		The PEPPER (PCB Enhanced Packaging, Placement and Routing) system is an extremely user-friendly printed circuit board package, place, and route code. The user interface resides on an IBM-PC and is integrated with the optimal schematic capture system, ED-SCHEMATICS. Full back annotation of both physical as well as electrical parameters is provided for. The package and placement tools are fully automatic and return a placement that minimizes routing difficulties by considering congestion, thermal build-up, and critical parts placement. The router utilizes bus, maze, strategy and pattern routing algorithms to achieve the highest percent completion possible. The layout editor is restricted to the IBM-PC while the CPU-intensive portions of PEPPER are available on CYBER mainframes and Cray supercomputers as well as the PC.	The Daisy BOARDMASTER family offers integration of PCB functions with CAE tools, allowing engineering involvement throughout the design cycle and insuring design integrity. Automatic and interactive placement and routing tools support complex electronic technologies and achieve the maximum board area utilization needed to route high-density PCBs. BOARDMASTER provides enhanced PCB manufacturability due to intelligent use of board area.  The Mechanical Documentation Program allows users to specify the board's geometric dimensions and generate all required manufacturing drawings and documentation, as well as perform general purpose drafting.  A choice of platforms is available to meet the cost/performance requirements of all organizations.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Circuit Board (Cont'd)

Dasoft Design Systems Dasoft-16	Datacon WRAPID 2	Design Computation DC/AUTOROUTER II	Design Computation DC/CHECK +
AT&T, IBM PC/XT/AT, NEC PC	IBM PC/XT/AT	AT&T, IBM PC/XT/AT	AT&T, IBM PC/XT/AT
X X X		X X X	X X X
X		X	X
	X		
X	X	X X	X X
X		X X X	X X
		X	X
		X	X
X		X	
X		X	
160 sq. in. 700 7,000		32" x 32" Over 4000 pins and vias 2500 1 32	32" x 32" Over 4000 pins and vias 2500 1 32
		Gerber photoplotter, Hewlett-Packard and Houston Instruments plotters, Epson dot matrix printers. Drill hole list.	Gerber photoplotter, Hewlett-Packard and Houston Instruments plotters, Epson dot matrix printers. Drill hole list.
	Wrapid 2 software runs with Future-net DASH 2 and DASH 3 software to enable users to turn schematic circuit files into databases to drive dataCon's automatic and semi-automatic wire wrap machines. dataCon's prototype service, based on Wrapid software, enables Futurenet CAE users to get hardware prototypes of their schematic designs in 4 to 6 days. Database processing and error-checking capabilities enable Wrapid users to generate error-free, formatted, load-and-go WRAP files to drive wire wrap machines. Wrapid displays an image of a selected prototype panel on a CRT screen. The user then places the components. When component placement is completed, the user then runs Wrapid to merge, process and error-check the netlist file with the component placement file. When the design/layout is free of errors, a WRAP file is generated to send to dataCon for quick turn-around prototype service. WRAPID is a trademark of Compion, Inc.	DC/AUTOROUTER II is a high-performance, full-feature, diagonal printed circuit board autorouter combining large board capability and user flexibility. Extensive use with commercial quality boards has yielded routing completion rates of 93% to 98%. In addition to its high completion rate, DC/AUTOROUTER II keeps the number of through-holes to a minimum by carefully planning via placement. The autorouter is interruptable and totally re-entrant: manual routing (using DRAFTSMAN-EE) may be done before, during, or after running the autorouter. For manually added routes, DC/CHECK, the design rule checker and netlist comparator, flags invalid or missing connections, checks for minimum trace and pad spacing, and verifies that all routes and vias are part of a connection from one pad to another.	DC/CHECK + consists of manual routing tools to be used in conjunction with DRAFTSMAN-EE. It includes DC/NETLIST netlist generator, DC/NETREAD, rat's nest generator, DC/CHECK design rule checker and netlist comparator, and DC/LAYER art master and drill hole list generator. DC/CHECK, the design rules checker and netlist comparator, flags invalid or missing connections, checks for minimum trace and pad spacing, and verifies that all routes and vias are part of a connection from one pad to another. DC/LAYER automatically generates art master files for silk screens, solder masks, and command layers, and it also produces a drill hole list.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Circuit Board (Cont'd)			
Source	Drafting Dynamics	EEsof	FutureNet (Data I/O)
Tool Name	PC	MiCAD	DASH-PCB
FOR DETAILED DATA SEE:			page 4651
Tool residence	COMPUTER AUTOMATION, MOTOROLA	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN	IBM PC/XT/AT
Device technologies			
Through hole mount	X	X	X
Surface mount	X	X	X
Hybrid	X	X	
ECL			X
Double sided boards		X	X
Related interconnect technologies			
Multiwire/Microwire	X		X
Wire wrap	X		X
Strip line	X	X	
Placement			
Manual	X	X	X
Interactive		X	X
Fully automatic			
Routing			
Manual	X	X	X
Interactive		X	X
Fully automatic			X
Design rule checking			
Batch mode	X		X
On-line (Interactive)			
Electrical rule checking			
Batch mode	X		X
On-line (Interactive)			X
Via minimization	X		X
Priority routing of critical nets			X
Layout parameter extraction			
PC board physical parameters			
Board size (max. in. x in.)	36 X 36	No limit	32" X 32"
Board density (max. components)	No limit	N/A	Unlimited
Nets (max.)	No limit	N/A	Unlimited
Min. trace pitch (mils)			1
Number of layers (max.)	8191	300	18
Links to CAM		Supports several plotters, rubylith cutters and photoplotters.	Gerber Photoplotter, Excellon CNC, Pen Plotter.
Description		For creating, editing, and producing drawings for microstrip and stripline circuits. MiCAD, completely compatible with Touchstone, automatically converts a Touchstone circuit into a physical layout. Includes interactive graphics editor for modifying physical layouts, and interactive "tuner" for changing circuit dimensions and seeing how the entire layout is affected. Hierarchical database provides layered view of circuits. Multi-level masks are easily created.	DASH-PCB deals with every aspect of printed circuit board design through a responsive user interface. Switched screens, mouse control, hierarchical menus, and command files contribute to the ease of using DASH-PCB. Component placement is interactive, with rubber-banding techniques assisting the designer in finding optimal placement. FutureNet's Expert Multi-Strategy router provides automatic trace routing options implementing multiple software strategies for "pattern fit" routing and maze routing. With reentrant routing, a designer can identify and manually route a critical part in his layout and allow DASH-PCB to complete the layout using autorouting. Built-in back-annotation allows schematic reference designers to be updated if individual gates or packages have been reassigned during layout. DASH-PCB automatically performs design rule checks for proper trace spacing and connectivity.  DASH-PCB uses the same 32-bit co-processor board used by DASH-CADAT Logic and Fault Simulation package.



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Physical Layout Tools—Circuit Board (Cont'd)			
Gerber Scientific Instrument PC800 Model 4	Hewlett-Packard Printed Circuit Design System	IBM CIEDS/CBDS	Intergraph Intergraph Hybrid Design
HEWLETT-PACKARD, MOTOROLA	HEWLETT-PACKARD	IBM MAINFRAME/MINI	DEC VAX, DEC MICROVAX, Intergraph Inter-Pro, InterAct
X X X	X X X	X X X	X X X
X	X	X	X
			X
X X	X X X	X X X	X X X
X X		X X X	X X X
X	X X	X X	X X
X	X X	X x	X X
	X	X	X
	X	X	X
		X	X
32" X 32" 25,000 + 25,000 + 8 per disk/multiple disks	50 X 50 Unlimited Unlimited 1 mil 99 layers	64" x 64" No hard limit No hard limit 1 99 (copper)	10" x 10" No limit 32,000 .01 mils 16 signal layers + 2080 other layers
Gerber photoplotter, Excellon CNC drill, Excellon CNC router, TruDrill CNC drill, TruDrill CNC router, Universal CNC insertion equipment.	HP3065, Gerber, NC Drill, Trudrill, Programatic outputs to ACI, and Manufacturing Reports.	Gerber, Excellon, Truedril, Genrad & Fairchild Testers, Auto insertion, neutral drill file	Links to probe testers, wire bonders, laser-trimmers, pattern generators.
The PC800 produces artwork negatives or positives typically used in the manufacture of printed circuit boards. It can also produce component lists, N/C machine tapes, drill drawings, component layout drawings, and silkscreen mask and solder mask negatives or positives. The PC800 Model 4 is claimed to be a perfect tool for surface mounted device (SMD) design because it is the perfect vehicle for interaction between computer and designer. A unique floating variable grid makes it easy to design SMD boards right on screen. It accepts components of any size and shape, whether metric or English standards. The PC800 Model 4 provides a large and flexible symbol storage library enabling designers to build in any number of SMD's for recall and positioning as needed. It provides for stacking of components to allow for maximum use of space. It delivers new levels of precision for timing and shielding tolerances. With four-decimal place accuracy, the PC800 Model 4 is ideal for spacing between components, traces and registration. It even designs curved traces.	The Printed Circuit Design System couples computer-aided-design to electrical engineering design, manufacturing and test to produce highly manufacturable boards that perform as intended. HP Printed Circuit Design System is part of the HP DesignCenter, an integrated solution for electronic, mechanical and software engineering teams. HP DesignCenter automates individual product design activities, while linking these activities to increase productivity and improve quality. Tight coupling to HP Electronic Design System automatically brings in netlist and part information, and communicates engineering changes and back annotation.  HP Printed Circuit Design System packing, placing and routing features can automatically lay out digital, analog and mixed digital/analog boards with through-hole and surface-mount technologies, and contain extensive facilities for thick-film hybrid design. To assure that the design is accurately transferred to manufacturing, the system automatically generates a spectrum of reports and files.	IBM's Computer-Integrated Electrical Design Series/Circuit Board Design System (CIEDS/CBDS) is an integrated set of applications that support all phases in the design of digital and analog printed circuit boards and thick-film hybrid substrates. CIEDS/CBDS features a powerful, easy-to-use, schematic capture and design entry module using interactive, graphical editing features for schematics and symbols. Full back and forward annotation capabilities with the CIEDS/CBDS physical layout tool in addition to automatic cross-page references are provided. The object-oriented, menu-driven physical layout system provides a wide range of automatic and interactive functions, supporting both surface mount and thick-film hybrid technology and automatic dual-sided placement. Powerful optimization algorithms allow the user to refine assignment and placement; whereas, highly efficient automatic routers coupled with strategy files produce excellent routing completion rates. The capability exists to improve board reliability and manufacturability by means of an automatic TIDY function.	Intergraph's hybrid microelectronics module is netlist-driven and supports both thick and thin film technologies. Automatic Resistor shape generation can place screened resistors on any level and on both sides of the substrate. Routing (interactive and automatic) can easily handle single and multilayer designs placing blind, buried, and staggered vias where necessary. The software can handle a mixture of chip and wire bond and double-sided surface mounted parts. Dielectric masks are automatically created and manufacturing interfaces to automate production are available.



# DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability		
Physical Layout Tools—Circuit Board (Cont'd)				
Source	Intergraph	Kontron	Mentor Graphics	
Tool Name	Printed Circuit Board Design	KAD System	PATHLINK/AUTOLINK	
FOR DETAILED DATA SEE:				
Tool residence	DEC VAX, DEC MICROVAX, Intergraph Inter-Pro, InterAct	IBM PC/XT/AT, Kontron AT compatible	APOLLO	
Device technologies				
Through hole mount	X	X	X	
Surface mount	X	X	X	
Hybrid	X	X	X	
ECL	X	X		
Double sided boards	X	X	X	
Related interconnect technologies				
Multiwire/Microwire	X	X	X	
Wire wrap	X	X	X	
Strip line		X	X	
Placement				
Manual	X	X	X	
Interactive	X	X	X	
Fully automatic	X		X	
Routing				
Manual	X	X	X	
Interactive	X	X	X	
Fully automatic	X	X	X	
Design rule checking				
Batch mode	X	X	X	
On-line (Interactive)	X	X	X	
Electrical rule checking				
Batch mode	X	X	X	
On-line (Interactive)	X	X	X	
Via minimization	X	X	X	
Priority routing of critical nets	X	X	X	
Layout parameter extraction	X	X		
PC board physical parameters				
Board size (max. in. x in.)	64" X 64"	64 x 64 (at 1 mil resolution)	1,000 X 1,000	
Board density (max. components)	10,000	No limit	1,000 +	
Nets (max.)	32,000	No limit	10,000 +	
Min. trace pitch (mils)	.01 mils	No limit		
Number of layers (max.)	16	255	255	
Links to CAM	Plotting, auto insertion, NC drill, Multiwire, Stitchweld, ATE, wirewrap. Optimization software creates efficient manufacturing files in machine format.	IGES interface, NC-output (Gerber, Drill, HPGL, DMPGL Generators)	Gerber photoplotter, Excellon CNC drill, ASCII database and EBCDIC and EIA output formats, panel layout.	
Description	Intergraph's PCB software provides automatic and interactive tools with the flexibility to use them in any combination to design and manufacture analog and/or digital boards. Recent enhancements include expanded support for drill, insertion and ATE equipment as well as a direct interface for the Optronics L2420 laser photoplotter. Polygon fill and cross hatching provide the visual feedback and artwork generation necessary for intelligent power-ground planes design. Cutouts that allow routing on the plane layer are automatically generated. This is accompanied by on-line Design Rule Checking that highlights and marks circuit violations as they occur. Finally, a forward/backward 2D-3D interface allows for a closer link into mechanical packaging.	The Kontron KAD System Circuit Board Layout Package uses Kontron's Graphics Editor and the full system includes an airline generator, interactive rule-driven layout generator, online design rule checker, auto-router, back annotation, and postprocessors for photo-plot, pen-plot, drill tape generation, etc.	PATHLINK PCB layout tools are combined with the CAE capabilities of the Mentor Graphics Design Station, resulting in a fully integrated design system called Board Station. Manual placement and routing functions can be used in conjunction with the constructive placement and automatic routing routines for optimum design results. Automatic T-junctions, segmented vias and buried vias are supported. Optional SMARTPART libraries provide automatic association of logic symbols to physical components by pin mappings. Manufacturing outputs include Bills of Materials, manufacturing drawings, photoplotter and drill files. Film and drill data can be viewed prior to output for verification. Board Station's open ASCII databases provides the capability to interface with other tools.	

Bold face indicates data is provided in the page noted



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Circuit Board (Cont'd)

Multiwire East Design Master on VAX	Multiwire East Design Master with Intergraph	Optima Technology OPTIMATE Place and Route	P-CAD PC-CARDS (PCB-1 and PCB-2)
DEC VAX	DEC VAX, + Intergraph EDS workstation.	APOLLO, DEC VAX, DEC MICROVAX	IBM PC/XT/AT
X X X	X X X	X X X X	X
X	X	X	X
X	X		X X X
X	X	X X X	X X
X	X	X X X	X X
X	X X	X X	X X
X	X X	X X	
		X	X
X	X	X	X
		X	
24" X 24" 2,000 28,000	24" X 24" 2,000 28,000	32" x 32" 1,000 3,900 1 16 plus power planes	64" X 64" 500 1,000 1 50
Gerber photoplotter, CNC drill, CNC Multiwire machine, electrical test.	Gerber photoplotter, CNC drill, CNC Multiwire machine.	Gerber photoplotter, Excellon drill, Calcomp, Hewlett-Packard and Benson pen plotters, Versatec and Benson electrostatic plotters.	Gerber & GTCO photoplotters, CNC drill, Flash-scan photoplotters.
Layout system for Multiwire boards.		Optimate is a sophisticated PCB layout system for the design of large, high density printed circuit boards. Optimate currently supports standard VLSI devices, surface mount devices, pin-grid arrays, and ECL technology. The system features true multilayer routing (up to 16 layers), correct-by-construction real time design rule checking, reentrant routing and placement, interactive reroute and, automatic and interactive gate, pin and component swapping. This highly interactive program offers ZAP-ROUTE, an industry unique capability where alternate routing solutions are presented to the designer for his selection. Input to the system is in the form of a net list and part list which can be automatically extracted from the OPTIMATE schematic, manually entered, or automatically derived from Silvar-Lisco, Valid Logic, or Mentor schematics.	Basic PCB CAD System. Fully integrated software provides printed circuit board layout and design, logic and component packaging, design rules checking, netlist extraction and formatting, bill of materials, printer/plotter support, and back annotation. Package includes software, users manuals, and PCB-1 security device.

## DESIGN AUTOMATION—Design Tools

Generic Function	Design Tool Capability		
Physical Layout Tools—Circuit Board (Cont'd)			
Source	P-CAD	Racal-Redac	Racal-Redac
Tool Name	PC-CARDS,-PLACE,-ROUTE (PCB-3)	REDBOARD	VISULA
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	IBM PC/XT/AT	APOLLO, DEC MICROVAX
Device technologies			
Through hole mount	X	X	X
Surface mount		X	X
Hybrid		X	X
ECL			
Double sided boards	X	X	X
Related interconnect technologies			
Multiwire/Microwire	X	X	X
Wire wrap	X	X	X
Strip line	X	X	X
Placement			
Manual	X		
Interactive	X	X	X
Fully automatic	X		X
Routing			
Manual	X		
Interactive	X		
Fully automatic	X	X	X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)	X		X
Electrical rule checking			
Batch mode		X	X
On-line (Interactive)			X
Via minimization	X	X	X
Priority routing of critical nets	X	X	X
Layout parameter extraction		X	X
PC board physical parameters			
Board size (max. in. x in.)	50 X 50 (1 mil grid)	25.575 x 25.575	180" X 180"
Board density (max. components)	500	511	1000 equivalent 14-pin components
Nets (max.)	6,000	1,900	Unlimited
Min. trace pitch (mils)		.01 mil	1/100 micron
Number of layers (max.)	50	16	50 electrical, 200 documentation
Links to CAM	Gerber and GTCO photoplotters.	Gerber, HP, Houston Inst. Pen Plotters	General purpose editor for interfacing to any machine. (see Description).
Description	VISULA approaches the problem of computer aided output with use of a generic post processing interface using machine description files. This means that output to virtually all post processing equipment including photo/pen/raster plotters, NC Drill and auto assembly machines can be achieved very easily. If a full link is not actually in place (there are links to most of the popular machines), then the user will only be required to carry out a minor amount of programming.		



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Circuit Board (Cont'd)

Royal Digital Systems AutoMate Physical Design Sys.	Scientific Calculations SCICARDS	Shared Resources Crystal Router	Shared Resources KOLOA PCB Design System
CONTROL DATA, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, PRIME, SUN, TEKTRONIX	DEC VAX, DEC MICROVAX, Scientific Calculations MC68020 worksta.	APOLLO, DEC VAX, ELXSI, IBM MAINFRAME/ MINI, PRIME, SUN, Gould, Multiflow	APOLLO, DEC VAX, ELXSI, IBM MAINFRAME/ MINI, SUN, Gould, Magnuson, Amdahl
X X X X	X X X X	X X X	X X X
X	X		
X X	X	X X	X
X X X	X X X	X X	X
X X	X X X	X	X
X X	X	X	X
X X	X	X	X
X	X	X	X
X	X		
30" x 30" 1,000 5,000 + .001 20 signal plus power and ground	60" X 60" 2,500 10,000 .0001 32	No practical limit No practical limit No practical limit No practical limit No practical limit	No practical limitation No practical limitation No practical limitation No practical limitation No practical limitation
Interface to Gerber, Excellon, Universal Instruments, Fairchild, and others.	GenRad tester, autoinsertion, drill machines, plotters, bareboard testers.	Gerber, Excellon, Zehntel	Gerber, Excellon.
The AutoMate Design System's physical design program is a sophisticated software package for physical electronic design automation; to provide maximum design accuracy regardless of board complexity or design technology. It interfaces with the Design Creation Tools and the Design Analysis Tools facilitating the exchange of information and improving productivity. Designed in a service bureau environment, AutoMate ensures fast, error-free turnaround and enables designers to make changes quickly and automatically. The Physical Design System features: automated placement and routing facilities; powerful interactive automated design for analog and digital printed circuit boards, and thick-film hybrid microcircuits; diagnostic and circuit validity checks to ensure error-free net lists; accuracy and assurance of board completion assured through three major, automatic routing algorithms; interfaces to CAE tools and Prime Medusa design software; and, provides comprehensive reports to augment released drawings.	A new routing technology, called LOOK OUT, an enhancement to the SCICARDS pcb layout program, is said to offer unparalleled speed and optimum manufacturability of circuit boards. Initial testing of LOOK OUT resulted in the complete routing of a six-layer, 11" x 7.7" board with 429 components, 1669 connections and a .33 density in just over 10 minutes. Unlike any other existing routing techniques, LOOK OUT revises completely the manner in which the computer views routing commands. It explores the routes, analyzes the channels and determines the best via locations before it places any traces.	The Koloa PCB Design System is a series of engineering productivity tools for electronic design. It integrates engineering tasks such as design packaging, design entry, checking, manufacturing and testing. The Koloa PCB Design System also provides a fast, economical, and accurate method of packaging high density, multi-layer PCB designs. Design inputs can come from a variety of engineering design systems.  The Koloa Design System exhibits the following characteristics: a) can allow the user to define the routing strategy resulting in 100% automatic routing of all signals; b) can handle both TTL and ECL technologies; also has the ability to handle multiple impedances in the same board; c) has extensive component libraries; d) has the ability to automatically "tune" critical nets to a fixed or equal length; e) has the ability to route "differential pair" signals; f) has extremely flexible routing surface definition; g) has the ability to handle irregular structures such as end connectors, flat packs, built-in delay lines, buried resistors, tooling holes, etc.	The Koloa PCB Design System is a series of engineering productivity tools for electronic design. It integrates engineering tasks such as design packaging, design entry, checking, manufacturing and testing. The Koloa PCB Design System also provides a fast, economical, and accurate method of packaging high density, multi-layer PCB designs. Design inputs can come from a variety of engineering design systems.  The Koloa Design System exhibits the following characteristics: a) can allow the user to define the routing strategy resulting in 100% automatic routing of all signals; b) can handle both TTL and ECL technologies; also has the ability to handle multiple impedances in the same board; c) has extensive component libraries; d) has the ability to automatically "tune" critical nets to a fixed or equal length; e) has the ability to route "differential pair" signals; f) has extremely flexible routing surface definition; g) has the ability to handle irregular structures such as edge connectors, flat packs, built-in delay lines, buried resistors, tooling holes, etc.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Circuit Board (Cont'd)			
Source	Silvar-Lisco	Silvar-Lisco	Tektronix CAE Systems
Tool Name	Cal-PC	OPTIMATE	MERLYN-P
FOR DETAILED DATA SEE:			page 4658
Tool residence		APOLLO, DEC VAX	APOLLO, DEC VAX, DEC MICROVAX
Device technologies Through hole mount Surface mount Hybrid ECL		X X	X X
Double sided boards		X	X
Related interconnect technologies Multiwire/Microwire Wire wrap Strip line		X X X	X
Placement Manual Interactive Fully automatic		X	X
Routing Manual Interactive Fully automatic		X	X X
Design rule checking Batch mode On-line (Interactive)		X	X X
Electrical rule checking Batch mode On-line (Interactive)			
Via minimization		X	X
Priority routing of critical nets		X	X
Layout parameter extraction			
PC board physical parameters Board size (max. in. x in.) Board density (max. components) Nets (max.) Min. trace pitch (mils) Number of layers (max.)		20 X 20 (20 mil grid); 50 x 50 (50 mil) 1,000 10,000  16 plus power and ground	32" X 32" 2,560 3,200 1.0 16
Links to CAM		Gerber, Benson photoplotters, Excellon, drill mask, silk screen, solder mask, HP, Versatec and Calcomp plotters.	Gerber photo, Excellon drill machines
Description	<p>The CAL-PC (Computer-Aided Layout for Printed Circuit Boards) software is highly interactive and offers state-of-the-art placement and routing that works closely with Silvar-Lisco's SDS Schematic Design System software, and the LOGIX-SL Logic Simulator. The CAL-PC software provides powerful editing and layout. CAL-PC operates on Apollo DN660 and DN560 workstations, and on the DEC MicroVAX II, and offers a command set that is specifically tailored to the PCB layout application. This feature provides ease of use and reduces training.</p> <p>CAL-PC's interactive environment enables users to choose between automatic, semi-automatic or manual routing, and allows input of design criteria outside algorithmic parameters. During the design process, there is ongoing real-time design rule checking which flags rule violations. CAL-PC's true multilayer router handles up to sixteen layers. True pad and track vias eliminates confusion.</p>		<p>MERLYN-P is a physical design system for automatic and interactive component placement and routing of printed circuit boards. This system provides full surface mount technology support for two-sided boards, including support for blind and buried vias. MERLYN-P is menu-driven, has an on-line help feature for all commands and features user-defined layout design rules that can be customized to meet special requirements. A standard parts library consisting of thousands of parts is supplied. A standard package of printed reports, diagnostic messages, assembly drawing and check plots are also provided.</p>



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Physical Layout Tools—Circuit Board (Cont'd)			
Valid Logic Systems Inc. Allegro page 4660	Valid Logic Systems Inc. Valid Route/Board Designer page 4660	Vamp Autorouter	Vamp CPlace
DEC MICROVAX, SUN	DEC VAX, DEC MICROVAX	APPLE	APPLE
X X X	X X X	X X X	X X X
X	X	X	
X	X		
X X X	X	X	X
X X X	X	X	X
X X	X	X	
X X	X	X	X
X	X	X	
X	X	X	
8 miles square at 1 mil resolution Unlimited Unlimited .00001 mil Fifty signal layers/256 database classes	32" X 32" 1,000 3900, 1,000 pins per net 16 plus power and user-defined layers	30 X 30 * (see Description) * (see Description) 16 signal, 16 power and ground	30" X 30"
Interfaces to NC drill & profile equipment are available. Gerber photoplot artwork. Automatic insertion interfaces and ATE interfaces are also supported.	Gerber photoplotter, NC drill.	Gerber Photoplotter, Excellon CNC drill.	
<p>The first rules-driven PCB design system that allows design engineers to control the physical implementation of their designs. Designers use ValidGED to attach properties to components and wires, and Allegro interprets those properties as design rules that must be followed during physical design of the PCB.</p> <p>Supports the front-to-back layout process for digital, analog, and high-frequency circuit technologies. Offering an icon-oriented user interface, Allegro provides almost unlimited design capacity, with no constraints on number of components, pins, or nets supported in a single design.</p> <p>Netlists may be transferred directly from Valid and other CAE systems. Automatic gate assignment tools work exceptionally fast.</p> <p>Component placement is supported by floorplanning capability, which helps the designer logically segment and place components. The Allegro router, called INSIGHT, supports simultaneous routing of up to eight layers at a time (with a maximum of 50 signal layers) and includes rip-up/re-route and glossing algorithms.</p>	<p>Available as network resource. Capability of interaction &amp; control of automatic tools adapts package to expertise &amp; creativity level of user. Unique semi-automatic capability.</p>	<p>* The board density and number of interconnections is determined by the hardware configuration. The more RAM on-line the greater the capability.</p>	

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Physical Layout Tools—Circuit Board (Cont'd)			
Source	Vamp	Vectron Graphics	Wintek
Tool Name	PCB Design	PCB Design	smARTWORK
FOR DETAILED DATA SEE:			
Tool residence	APPLE	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, MASSCOMP	IBM PC/XT/AT
Device technologies			
Through hole mount	X	X	X
Surface mount	X	X	
Hybrid	X	X	
ECL			
Double sided boards	X	X	X
Related interconnect technologies			
Multiwire/Microwire			
Wire wrap			
Strip line			
Placement			
Manual	X		X
Interactive	X	X	
Fully automatic			
Routing			
Manual	X		X
Interactive	X		X
Fully automatic		X	X
Design rule checking			
Batch mode		X	
On-line (Interactive)		X	X
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)		X	
Via minimization		X	
Priority routing of critical nets		X	
Layout parameter extraction		X	X
PC board physical parameters			
Board size (max. in. x in.)	30" X 30"	32" x 32"	10" x 16"
Board density (max. components)	*	10,000	1000
Nets (max.)	*	No limit	3000
Min. trace pitch (mils)			Maintains 19-mil minimum spacing
Number of layers (max.)	9	21	2 conductor, silkscreen, solder masks
Links to CAM	Gerber photoplotter, Excellon CNC drill.	Gerber photoplotter, Excellon CNC drill.	CNC drill tape generation utility, Gerber photoplotter driver.
Description	*The board density and number of interconnections is determined by the hardware configuration. The more RAM on-line the greater the capability.		
	Vectron Graphics has combined a MicroVAX II with a Ramtek high-resolution 1280 x 1024 pixel display to create a new workstation for printed circuit design. This new configuration includes Vectron Graphic's PCB layout software. The software features an open system architecture which enables users to add other software programs to the new workstation, including the entire library of programs available for VAX and MicroVAX computers.	smARTWORK is a computer-aided-design package that aids electrical engineers and technicians in the creation and revision of printed-circuit-board artwork on an IBM Personal Computer. The software handles single- and double-sided boards up to 10-by-16 inches. Clean, clear graphics show one layer of the board in black and white or all layers in color. The interactive router finds the shortest route between two electrical networks, speeding the layout process. smARTWORK also includes an autorouter. Production-quality 2X artwork can be produced using a pen-and-ink plotter; prototype-quality 2X artwork and checkplots can be produced using a dot-matrix printer. Padmaster and soldermask plots are created automatically.	
		Pad sizes and shapes, as well as trace widths, are selectable. A silkscreen (component-designation) layer is supported, along with text on any layer. Footprints for DIP's and SIP's are built-in; a custom library can be created easily.	
		Used by thousands of engineers around the world to design their printed-circuit boards. Price \$895.00.	



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Physical Layout Tools—Circuit Board (Cont'd)			
Xerox Expert PCB			
XEROX			
X X X			
X			
X			
X X X			
X X X			
X X			
X X			
X			
32" x 32" 250 Unlimited 0.001 16			
Drill tape output, Gerber photoplotter, wire graphics, wire wrap list.			
Expert Placement and Routing (PCB) allows PC board designers to place parts on the PC board and route the connections between parts. The direct link between Expert Schematics and Expert PCB allows full interaction between the two tools. Simultaneous views of schematic design and PC board encourages this interactivity. The designer selects symbols on the schematic design and places them on the board, or instructs the system to do automatic placement. Expert PCB uses a three phase gridless router, with minimal space etch routing capabilities.			

# IC MASTER

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Gate Array			
Source	Control Data	Daisy Systems	Daisy Systems
Tool Name	MIDAS	MegaGATEMASTER	Personal GATEMASTER
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, Orcatech	Daisy MegaLOGICIAN	IBM PC/XT/AT, Daisy Personal LOGICIAN 386
Placement			
Manual	X	X	X
Interactive	X	X	X
Fully automatic		X	X
Routing			
Manual		X	X
Interactive	X	X	X
Fully automatic	X	X	X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Priority routing of critical nets	X	X	X
Capacity (max. gates)	20,000	10,000 +	3,000
Interconnect layers (max.)	2 routing layers + 1 via layer	2	2
Gate array manufacturers who certify physical layout using this tool	Honeywell, National Semiconductor, Rockwell International, VTC.	RCA, Motorola, Siliconix, MHS, NEC, TI Europe	RCA, Motorola, Siliconix, MHS, NEC, TI Europe.
Description	Modular Integrated Design Automation System.	<p>The MegaGATEMASTER speeds gate array design with a proprietary hardware accelerator. Logic and fault simulation are also accelerated. When linked as part of an Ethernet-based network, MegaGATEMASTER's hardware accelerator can be remotely accessed from other Daisy workstations on the network.</p> <p>MegaGATEMASTER's automatic placement is speeded up to 15 times faster than other workstations performing the same task. Using the simulated annealing algorithm in performance benchmarks, MegaGATEMASTER has completed 100% autoroutable placement of a 95% utilized, 4800-gate CMOS array in less than 20 minutes. This compares to typical simulated annealing times on a VAX 11/780 of 10 hours plus.</p> <p>This system offers a wide range of vendor support, with design kits for over 150 array and standard cell families from more than 70 semicustom vendors.</p>	<p>Personal GATEMASTER is a full-function workstation that offers a complete turnkey solution to low-cost gate array design. It provides physical layout, schematic entry, pre- and post-layout simulation, timing analysis, and test development.</p> <p>Personal GATEMASTER's automatic placement and route tools include advanced simulated annealing that produces improved placement efficiency for 100% autoroutable placements on arrays. Automatic place and route in combination with flexible manual editing capabilities result in high-utilization, high-density arrays for a variety of technologies.</p> <p>This system offers a wide range of vendor support, with design kits for over 150 array and standard cell families from more than 70 semicustom vendors.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Gate Array (Cont'd)

EXAR GATEMASTER (see Daisy Systems) page 4222	Fairchild FAIRCAD	Ferranti Interdesign Silicon Design Sys. ULASILCOM	LSI Logic LDSIII Layout page 4653
Daisy GATEMASTER	DEC VAX, DEC MICROVAX	DEC VAX, DEC MICROVAX	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PYRAMID, RAMTEK, Amdahl
X X X	X X X	X X X	X X X
X X X	X X X	X X X	X X X
X X	X X	X X	X X
X X	X X	X X	X X
X	X	X	X
6,000	Depending on array	10,000	LCA 10000 to 50K gates; w/channels 10K
2	Two to three layers	2	2
EXAR Corp.	Fairchild.	Ferranti Interdesign.	LSI Logic Corp. and approved second sources.
GATEMASTER is a powerful gate array layout system that resides on Daisy equipment. EXAR design automation system uses the GATEMASTER. It has been in use since 1983.	FAIRCAD's powerful placement program allows random, manual, or automatic placement of components. FAIRCAD provides the ability to interactively place I/Os and/or critical path components in minutes. Automatic placement programs are available to help achieve the optimum placement of the design. Placement, like all other interactive FAIRCAD programs, is menu-driven with extensive "help" features that list all possible user options.  Like placement, FAIRCAD's routing program has both manual and automatic features and is completely interactive. Critical nets may be pre-routed and the automatic router invoked to finish routing the design. Manual routing, completely menu driven, is available for specifying critical paths and editing disconnects. FAIRCAD's program for viewing the design reads information from the design file and allows viewing of unconnected nets; "airlines"—diagonal lines—are drawn between unconnected pins. As an additional safeguard against errors, FAIRCAD employs the automatic Design Rule Checker.		

# IC MASTER

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Gate Array (Cont'd)			
Source	Matra Design Systems	Matra Design Systems	Mentor Graphics
Tool Name	ALGA	KLGA	GATEGRAPH/PLACE/ROUTE
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, IBM PC/XT/AT	DEC VAX, IBM PC/XT/AT	APOLLO
Placement			
Manual			X
Interactive		X	X
Fully automatic	X		X
Routing			
Manual			X
Interactive		X	X
Fully automatic	X		X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)			X
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)			X
Priority routing of critical nets	X	X	X
Capacity (max. gates)	1200	1,200	10,000 +
Interconnect layers (max.)	1	1	2
Gate array manufacturers who certify physical layout using this tool	Matra Design Systems.	Matra Design Systems.	NEC, Gould, Honeywell, Motorola, Thomson-Mostek, Laserpath.
Description			Automatic and interactive gate array placement and routing.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Gate Array (Cont'd)

National Semiconductor Design Automation System page 4294	Plessey CLAMP/SCARP	Plessey CLASSIC	Scientific Calculations MEDS
IBM MAINFRAME/MINI	DEC VAX		DEC VAX, DEC MICROVAX
X X X	X X		X X X
X X X	X		X X X
X			X X
X	X		
X	X		X
No practical limit	100,000		20,000 +
2	2		4
National Semiconductor.	Plessey, Array Logic.		California Devices, Raytheon, GTE.
For the design of National Semiconductor gate arrays. National implements Tektronix's MERLYN-G place and route software for gate arrays. This channel-router consistently routes even highly utilized arrays automatically. It allows the user to define fixed placement of circuit elements and keeps interconnect wirelength to a minimum according to weight factors specified.		Plessey now offers a software package that allows Daisy, Mentor, Valid and Futurenet workstations to interface with Plessey's CLASSIC IC design package. CLASSIC (Custom Logic Analysis Simulation System for Integrated Circuits) is a VAX-based system used for gate array and MEGACELL designs. Plessey's new software package allows an engineer to do his preliminary design on one of the workstations and then transfer his net list to his VAX for fault analysis, place, auto route and final simulation. The designer also has the alternative of giving the net list to Plessey for completion.	The MEDS System is a hierarchical IC layout system that supports, in a single system, the full spectrum of IC design methodologies including gate array, standard cell and full custom designs. It is a netlist-guided and design-rule constrained physical design system that assures correct-by-construction placement and routing results. Advanced layout algorithms, together with powerful interactive graphics facilities and extensive user control, enable the IC designer to tackle the largest and toughest layout problems. The placement capability includes an automatic placement algorithm based on a unique simulated annealing implementation and a "force-directed" constructive placement algorithm with manual seeding. An optional iterative placement improvement phase is provided. Intelligent routers are able to "see" the internal geometries of the cells and route over, around or through a cell without violating design rules. The system will support both channelled and channelless (sea of gates) architectures.

**DESIGN AUTOMATION—Design Tools****Generic Function****Design Tool Capability****Physical Layout Tools—Gate Array (Cont'd)**

Source	Silvar-Lisco	Tektronix CAE Systems	
Tool Name	GARDS	MERLYN-G	
FOR DETAILED DATA SEE:		page 4658	
Tool residence	APOLLO, DEC VAX, IBM MAINFRAME/MINI	APOLLO, CRAY, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI	
Placement			
Manual		X	
Interactive	X	X	
Fully automatic	X	X	
Routing			
Manual			
Interactive	X	X	
Fully automatic	X	X	
Design rule checking			
Batch mode	X	X	
On-line (Interactive)	X	X	
Electrical rule checking			
Batch mode	X	X	
On-line (Interactive)	X	X	
Priority routing of critical nets	X	X	
Capacity (max. gates)	30,000	No system limit	
Interconnect layers (max.)	3	2-3	
Gate array manufacturers who certify physical layout using this tool	Fairchild, Gould, AMCC, MMI.		
Description		Provides 100% automatic placement and routing for a variety of array family designs. MERLYN-G's powerful algorithms permit higher population density, achieving a larger percentage of populated gates per array, ensuring automatic completion. The system's configurable modular architecture lets you expand the capabilities of your system in step with your needs and expanding computer power. MERLYN-G adapts easily to your changing technologies, unrestricted by number of gates. A Graphical Database manager is provided. Routing tools include global, maze, and rip-up and retry. Interactive graphical placement and wire editors are also featured.	



DESIGN AUTOMATION—Design Tools

Generic Function	Design Tool Capability		
Physical Layout Tools—Standard Cell			
Source	Applicon	Daisy Systems	ECAD
Tool Name	VLSI Design Editor	CELLMASTER	Symbad/BPR
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, DEC MICROVAX, SUN	IBM PC/XT/AT, Daisy LOGICIAN 386/Personal LOGICIAN 386	APOLLO, DEC VAX, DEC MICROVAX, SUN, TEKTRONIX
Placement			
Manual	X	X	X
Interactive	X	X	X
Fully automatic	X	X	X
Placement features			
Automatic placement of VLSI cells	X	X	X
Locate I/O pins anywhere on cell	X	X	X
Automatic compaction	X	X	X
Routing			
Manual	X	X	X
Interactive	X	X	X
Fully automatic	X	X	X
Routing features			
Priority routing of critical nets	X	X	X
Route on top of cells	X	X	X
Route through cells	X	X	X
Automatic power/ground buss rte.	X	X	X
Cell dimensioning parameters			
Fixed height/fixed width	X	X	X
Fixed height/variable width	X	X	X
Variable height/variable width	X	X	X
Variable size I/O buffers	X	X	X
Design rule checking			
Batch mode	X	X	
On-line (Interactive)	X	X	X
Electrical rule checking			
Batch mode	X	X	
On-line (Interactive)	X	X	X
Layout parameter extraction	X	X	X
Capacity (max. moveable blocks)	No limit	Limited by system resources	100 blocks per level
Interconnect layers (max.)	3	2.5	255 layers allowed
Standard cell manufacturers who certify physical layout using this tool		MOSIS and NCR	List provided upon request.
Description	The Applicon VLSI Design Editor is a knowledge-based design system that effectively integrates the design, layout, and analysis phases of VLSI design. The logic design and layout editor is based on electrical connectivity, with an internal knowledge of process technologies. Using the technology base, the editor monitors circuit designs for design rule compliance and reports violations in both graphics and textual formats. Users can describe new technologies, and each technology function may contain an unlimited number of materials or functional primitives. The technologies contain electrical as well as physical modeling information.	CELLMASTER software is optimized for cell-based IC layout and runs on the Daisy LOGICIAN 386. With CELLMASTER's constraint-free layout, both blocks and cells can be used.  CELLMASTER provides 100 percent power routing, regardless of the chip topology created.  CELLMASTER also: optimizes for minimum die size, is both automatic and highly interactive, adheres to correct-by-construction design methodology, and provides an integrated tool set.	ECAD's SYMBAD/BPR is an interactive block place and route system for IC design. The system includes an automatic placer and router, a block compactor, and a symbolic editor and checker. The system offers designers complete control over block layout and connection through its interactive interface. SYMBAD BPR is the first component of ECAD's symbolic automated IC design system, SYMBAD. SYMBAD uses a fully symbolic approach to IC design. With it, engineers can choose pre-drawn transistors or entire functional cell blocks, for example, from a design library and simply connect them. SYMBAD is based on highly structured, intelligent data base that all SYMBAD tools share. The SYMBAD systems' interactive user interface provides designers complete control over layout at all steps of the process.  SYMBAD software places and routes the blocks using netlist connection data in the SYMBAD data base. The SYMBAD router implements the physical connections using the shortest possible wire lengths and the smallest routing area. It works with rectangular blocks of any shape and size.

**DESIGN AUTOMATION—Design Tools****Generic Function****Design Tool Capability****Physical Layout Tools—Standard Cell (Cont'd)**

Source	ECAD	ECAD	ES2/US2
Tool Name	Symbad/OED	Symbad/PED	SOLO 1000/SOLO 1200
<b>FOR DETAILED DATA SEE:</b>			
<b>Tool residence</b>	APOLLO, DEC VAX, DEC MICROVAX, SUN	APOLLO, DEC MICROVAX, SUN	APOLLO, DEC VAX, DEC MICROVAX, SUN, VAXstation 2000
<b>Placement</b> Manual Interactive Fully automatic	X	X	X
<b>Placement features</b> Automatic placement of VLSI cells Locate I/O pins anywhere on cell Automatic compaction	X		X
<b>Routing</b> Manual Interactive Fully automatic	X	X	X
<b>Routing features</b> Priority routing of critical nets Route on top of cells Route through cells Automatic power/ground buss rte.			X X
<b>Cell dimensioning parameters</b> Fixed height/fixed width Fixed height/variable width Variable height/variable width Variable size I/O buffers	X X X X	X X X X	
<b>Design rule checking</b> Batch mode On-line (Interactive)	X X	X X	
<b>Electrical rule checking</b> Batch mode On-line (Interactive)	X X	X X	
<b>Layout parameter extraction</b>	X	X	X
<b>Capacity (max. moveable blocks)</b>	200 for autoplacement, 1000 for non-auto	No practical limit	
<b>Interconnect layers (max.)</b>	No limit, 2 1/2 at a time	No practical limit	
<b>Standard cell manufacturers who certify physical layout using this tool</b>			
<b>Description</b>	Symbad/OED (Object-Based Editor) allows users to manipulate high-level objects (such as parameterizable transistors, contacts or wires), rather than individual polygons. The tool embodies automatic compaction algorithms that compact IC designs and allow manual intervention at any time. Symbad/OED integrates the user's design-rule specifications, which frees layout designers from design-rule concerns, thus reducing errors and layout time. Because of design-rule independence, users can transfer designs among different technologies.	Symbad/PED is a polygon-based editor for integrated circuit layout design. Designed to augment Symbad/OED and Symbad/BPR, cells manually created with Symbad/PED can be mixed with cells created with Symbad/OED with no data conversion. Advanced commands supported include Boolean and sizing operations.	In addition to the capabilities of the SOLO package, it has the ability to combine standard cell blocks for integration at the highest level.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Standard Cell (Cont'd)

EXAR CAL-MP (see Silvar-Lisco) page 4222	Fairchild FAIRCAD	Gould Semiconductor Division SCEPTRE II page 4244	Harris Semiconductor Harris/SDA Workstation page 4246
DEC VAX	DEC VAX, DEC MICROVAX	IBM PC/XT/AT, NEC PC, VICTOR	APOLLO, DEC MICROVAX, MASSCOMP, SUN
X X X	X X X	X	X X X
X X X	X X X		X X X
X	X X X	X	X X X
X X X X	X X X X	X X	X X X X
X X	X X	X X X	X X X X
X	X X	X	X X
X	X X	X	X X
X	X		X
3	Two to three	2	3
EXAR	Fairchild.	Gould Semiconductors.	Hughes, GE, ES2, Toshiba, SGS, LSI (Canada)
CAL-MP is a powerful layout system for standard cells. It is an integral part of the EXAR Design Automation System for N2000 and P3000 standard cell libraries.	FAIRCAD's powerful placement program allows random, manual, or automatic placement of components. FAIRCAD provides the ability to interactively place I/Os and/or critical path components in minutes. Automatic placement programs are available to help achieve the optimum placement for the design. Placement, like all other interactive FAIRCAD programs, is menu-driven with extensive "help" features that list all possible user options. Many important display features such as cell and component outlines are also provided.  Like placement, FAIRCAD's routing program has both manual and automatic features and is completely interactive. Critical nets may be pre-routed and the automatic router invoked to finish routing the design. Manual routing, completely menu-driven, is available for specifying critical paths and editing disconnects. FAIRCAD's program for viewing the design reads information from the design file and allows viewing of unconnected nets; "airlines"—diagonal lines—are drawn between unconnected pins. As an additional safeguard against errors, FAIRCAD employs the automatic DRC.	Supports complete cell-based ASIC design from schematic capture through physical layout and verification.	Harris supplies the state-of-the-art SDA place and route system. Most circuits can be routed automatically using a Harris devised user shell requiring the designer only to pick from several options on a single form. For advanced users or highly specialized designs the full power of the SDA software is available. Both flat and hierarchical design styles are supported. The system includes a rich set of standard cells and allows the introduction of custom cells and macro blocks. For CMOS designs Harris' configurable ROM and RAM compilers generate route-ready macro blocks. In GaAs, Harris has developed a knowledge-based design system to aid the circuit designer in dealing with the strengths and constraints of GaAs standard cell design. All tools are built on SDA's unified Framework allowing a quick and easy design flow from design to layout to verification.

Bold face indicates data is provided in the page noted

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Standard Cell (Cont'd)			
Source Tool Name FOR DETAILED DATA SEE:	Intergraph TANCELL	LSI Logic LDSIII Cell Layout page 4653	Mentor Graphics CELLGRAPH/PLACE/ROUTE
Tool residence	DEC VAX, DEC MICROVAX, Intergraph Inter-Pro, InterAct	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PYRAMID, SUN, Am-dahl	APOLLO
Placement Manual Interactive Fully automatic	  X  	  X X X	  X X X
Placement features Automatic placement of VLSI cells Locate I/O pins anywhere on cell Automatic compaction	 X X	 X	 X X X
Routing Manual Interactive Fully automatic	  X X	  X X X	  X X X
Routing features Priority routing of critical nets Route on top of cells Route through cells Automatic power/ground buss rte.	 X X X X	 X X X X	 X X X X
Cell dimensioning parameters Fixed height/fixed width Fixed height/variable width Variable height/variable width Variable size I/O buffers	 X X X	  X	 X X X
Design rule checking Batch mode On-line (Interactive)	 X X	 X X	 X X
Electrical rule checking Batch mode On-line (Interactive)	 X X	 X X	 X X
Layout parameter extraction	X	X	X
Capacity (max. moveable blocks)	10,000	14,800 eq. gates (51,800 cell units)	5,000
Interconnect layers (max.)	2	2	2
Standard cell manufacturers who certify physical layout using this tool		LSI Logic Corp. and LSI Logic approved second sources.	NCR 2 micron library, MOSIS 3 micron library.
Description	The TANCELL cell-based IC design system now provides a new level of design performance and flexibility for layouts incorporating large Macro Blocks. These new automatic routing tools produce Macro Block design with minimal die size. TANCELL also supports block placement anywhere in the chip core area, and arbitrary spacing of ports on all four sides of blocks. Full automatic routing and interactive wire editing of three interconnect layers in cell-based IC's have been added to the TANCELL IC design. Designers wishing to use three layer IC process technologies can now benefit from the die size improvements, design flexibility and timing correct-by-construction design capabilities available through TANCELL.		Auto and interactive floorplanning. Auto and interactive power routing. Auto and interactive size reduction. Technology entry tool. Auto and interactive placement. Auto and interactive signal routing.



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Physical Layout Tools—Standard Cell (Cont'd)**

National Semiconductor Design Automation System page 4294	Plessey CLASSIC	Plessey Megacell Layout Editor	Scientific Calculations MEDS
DEC VAX, DEC MICROVAX, IBM MAINFRAME/ MINI		DEC VAX	DEC VAX, DEC MICROVAX
X X X		X	X X X
X X X			X X
X X X		X X	X X X
X X X X			X X X X
X X X		X X X	X X X
X		X	X X
X		X	X
No practical limit			20,000 +
2 at present, 3 by mid 1988		2	4
National Semiconductor		Plessey	California Devices, Raytheon, GTE.
For the design of National Semiconductor standard cells. National integrates Tektronix's Merlyn-S place and route software for standard cells in its design system. This block-router with its open architecture allows National to fully integrate it in the design system. Placement of a design is package driven. It automatically places and routes designs and utilizes silicon area very efficiently. Merlyn-S can be used interactively as well.	Plessey now offers a software package that allows Daisy, Mentor, Valid and Futurenet workstations to interface with Plessey's CLASSIC IC design package. CLASSIC (Custom Logic Analysis Simulation System for Integrated Circuits) is a VAX-based system used for gate array and MEGACELL designs. Plessey's new software package allows an engineer to do his preliminary design and documentation on one of the workstations and then transfer his net list to his VAX for fault analysis, place, auto route and final simulation. The designer also has the alternative of giving the net list to Plessey for completion.		

DESIGN AUTOMATION—Design Tools			
Generic Function		Design Tool Capability	
Physical Layout Tools—Standard Cell (Cont'd)			
Source	SDA Systems	Silicon Compiler Systems	Silvar-Lisco
Tool Name	Place and Route	Generator Development Tools	CAL-MP
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC MICROVAX, SUN	APOLLO, DEC VAX, IBM MAINFRAME/MINI
Placement			
Manual	X	X	
Interactive	X		X
Fully automatic	X	X	
Placement features			
Automatic placement of VLSI cells	X	X	X
Locate I/O pins anywhere on cell	X	X	X
Automatic compaction	X	X	X
Routing			
Manual	X	X	
Interactive	X		X
Fully automatic	X	X	X
Routing features			
Priority routing of critical nets	X	X	X
Route on top of cells	X	X	X
Route through cells	X	X	X
Automatic power/ground buss rte.	X	X	X
Cell dimensioning parameters			
Fixed height/fixed width	X	X	X
Fixed height/variable width	X	X	X
Variable height/variable width	X	X	X
Variable size I/O buffers	X	X	
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Layout parameter extraction	X	X	X
Capacity (max. moveable blocks)	Over 15,000 cells on workstation	2,000- 3,000 cells	4,000
Interconnect layers (max.)	2 or 3; supports multiple technologies	3	3 (typically 2 metal, 1 poly)
Standard cell manufacturers who certify physical layout using this tool			TI, Motorola, NCR, Fairchild, IMI, Thompson CSF, Torric, Gould AMI.
Description	<p>Place and Route is a powerful, general purpose tool for the automatic layout of compact, high-performance cell-based IC. It supports a variety of chip and block topologies including: row-type standard cell, mixed macro cell/standard cell, and pure rectangular macro cell ICs. Hierarchical design is also supported. Place and Route handles the layout of the largest ICs common today; designs can contain just a few cells to more than 10 thousand cells on a single design level. Most common technologies, including CMOS, NMOS, bipolar, and gallium arsenide are supported. Place and Route features advanced capabilities in floor planning, placement, channel generation, global routing, detailed routing, and design verification.</p> <p>Automatic Macro Cell Placement is provided as an option to SDA's Place and Route package. Macro Cell Placement features an advanced, automatic placement algorithm that places rectilinearly shaped macro cells within SDA's general purpose Place and Route environment.</p>	<p>The Generator Development Tools (GDT) can be used by IC designers to create their own silicon compilers. The power of the GDT is based on a new language, L, developed by SDL. Generators, produced using L, can accept parameters from a user and develop completely custom layouts. GDT can also be used by logic designers to create larger functional blocks or complete chips using their own or Silicon Design Lab's basic functions. GDT features a Macintosh-like user interface, on-line design rule checking and an integrated hierarchical mixed-mode functional/circuit/fault simulator. GDT also includes a complete standard cell library and automatic place and route as well as PLA generation tools.</p>	



## DESIGN AUTOMATION—Design Tools

## Design Tool Capability

## Physical Layout Tools—Standard Cell (Cont'd)

Tangent Systems TANCELL	Tektronix CAE Systems MERLYN-S page 4658	Valid Logic Systems Inc. ValidBLOCKS page 4660	VIA Systems BuildingBLOCKS
APOLLO, DEC VAX, DEC MICROVAX, Intergraph Interpro-32C	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI	DEC MICROVAX, SUN, Valid SCALDSsystem	APOLLO, DEC MICROVAX, SUN
X X	X X X	X X X	X X X
X X X	X X X	X X X	X X X
X X	X X	X X X	X
* X X	X X X X	X X X X	X X X X
X X X X	X X X X	X X	X X X X
X X	X X	X	
X X	X X	X	
X	X	X	
10,000	No system limit	Unlimited	
3	2-3	3	3
<p>*Uses Timing Assurance to produce circuits with timing-correct layouts.</p> <p>Provides 100% automatic placement and routing for a variety of cell family designs with standard cells, blocks or a mix of both. Interactive graphical placement and routing tools provided. Tektronix' Quadratic Plotter utilizes a proprietary algorithm to optimally place devices, achieving results superior to traditional iterative methods. A Graphical Database Manager is also provided. Automatic routing tools support well-space, compaction, and tapered power/ground routing, as well as enabling you to break the cyclic routing trap.</p> <p>ValidBLOCKS is an advanced layout tool for the interactive placement and automatic routing of complex integrated circuits. ValidBLOCKS is an excellent semi-custom place and route tool for in-house use. Its fast, complete routing makes interactive design possible.</p> <p>Designs can be realized using standard cell libraries, full custom blocks, or a combination of the two thereby making it an ideal tool for system designers, IC engineers, and layout designers. With ValidBLOCKS you can achieve the same density as that produced by manual routing in a fraction of the time.</p> <p>* Provides fast routing performance * Performs automatic sizing and routing of power busses * Supports three interconnect layers * Unconstrained gridless routing for maximum density * Supports hierarchical design methodology * Integrated with Valid's family of design tools</p> <p>BuildingBLOCKS is a hierarchical automatic placement and routing package which accelerates the physical layout of all-level application specific integrated circuits. By combining automatic placement and routing with interactive editing functions, BuildingBLOCKS provides a flexible, open-ended design environment. BuildingBLOCKS is available for the UNIX-based Sun Microsystem products, and the ULTRIX-based VAXstation II/GPX.</p> <p>Features: 100% complete, gridless automatic placement and routing; two- or three-layer interconnect; irregularly shaped blocks; interactive editors for placement, geometry and connectivity; sized power and ground busses; floorplanning; graphical block builder; and, hierarchy.</p>			

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Physical Layout Tools—Standard Cell (Cont'd)			
Source	VLSI Technology		
Tool Name	VTIlogicComp		
FOR DETAILED DATA SEE:	page 4665		
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN		
Placement			
Manual			
Interactive	X		
Fully automatic	X		
Placement features			
Automatic placement of VLSI cells	X		
Locate I/O pins anywhere on cell	X		
Automatic compaction	X		
Routing			
Manual			
Interactive	X		
Fully automatic	X		
Routing features			
Priority routing of critical nets	X		
Route on top of cells	X		
Route through cells	X		
Automatic power/ground buss rte.	X		
Cell dimensioning parameters			
Fixed height/fixed width			
Fixed height/variable width	X		
Variable height/variable width	X		
Variable size I/O buffers	X		
Design rule checking			
Batch mode			
On-line (Interactive)	X		
Electrical rule checking			
Batch mode			
On-line (Interactive)	X		
Layout parameter extraction	X		
Capacity (max. moveable blocks)	Unknown		
Interconnect layers (max.)	3		
Standard cell manufacturers who certify physical layout using this tool	VLSI Technology Inc.		
Description	<p>This logic compiler package provides a simple, efficient method for automatically converting schematics, composed of standard cells, into layout. The schematic is loaded into the LogicComp window where it is automatically placed and routed. The logic compiler can either generate an entire chip (with I/O pads) or a functional block that can be used with other functional blocks (i.e., compiled or custom cells) to generate a larger chip. Using the logic compiler, the user can control the placement of critical paths by weighting nets or seed-placing cells. The user can also control I/O placement and the shape of the chip of functional block.</p> <p>VTIlogicComp is optimized for double-metal routing. Second layer metal is routed over the cell, based on automatically generated blockage masks. VLSI's 2-micron CMOS standard cell library has been carefully designed to maximize the number of vertical metal two routing tracks allowed over the cell so that this over-routing is fully exploited. The Logic Compiler routes as many signals as possible in the metal two layer to improve chip yield and performance.</p>		



DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Full Custom			
Source	Applicon	Caeco	Calma
Tool Name	VLSI Custom Design Editor	Layout Design System	CustomPlus
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, DEC MICROVAX, SUN	APOLLO, SUN	DATA GENERAL
Hierarchical design			
Starting with floor plan		X	X
Starting with macros		X	X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)	X		X
Layout parameter extraction	X	X	X
Editing features			
Like cells all graphically updated	X	X	X
Boolean shapes editing			X
Edge editing	X	X	X
Angles supported			
Orthogonal		X	X
Octagonal		X	X
All	X	X	X
Number of layers (max.)	(2 <sup>32</sup> )-1	264	64
Output format	ECAD internal, NCA, Apple, PG, EBEAM.	GDSII.	GDSII, CIF, PG tape, E-Beam.
Description	The Applicon VLSI Design Editor is a knowledge-based design system that effectively integrates the design, layout, and analysis phases of VLSI design. The logic design and layout editor is based on electrical connectivity, with an internal knowledge of process technologies. Using the technology base, the editor monitors circuit designs for design rule compliance and reports violations in both graphics and textual formats. Users can describe new technologies, and each technology function may contain an unlimited number of materials or functional primitives. The technologies may contain electrical as well as physical modeling information.	Component layout 3X-6X over conventional layout. Parametric MACROS. On-line DRCs.	The system has all the features of GDSII plus additional capabilities. It is a symbolic design system but will also display full mask geometries. It maintains connectivity between wires and cells. It has a special type of programmable cell called PCELLS which can be specified and programmed by the user to automatically generate specific modules. Since these cells can work off a design rule file, they will automatically adjust to reflect changes in the design rules. The layout can be controlled by a schematic generated netlist, preventing design errors before they happen. It will also perform automatic compaction of the design. The system works off a user specified technology base which makes it easy to change resulting designs to new design rules.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Full Custom (Cont'd)			
Source	Calma	Clarity Systems	Computervision
Tool Name	GDSII	TopSet and GeoSet	CADD5 2/VLSI
FOR DETAILED DATA SEE:			
Tool residence	DATA GENERAL	APOLLO	Proprietary
Hierarchical design			
Starting with floor plan	X	X	X
Starting with macros	X	X	X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	
Layout parameter extraction	X	X	X
Editing features			
Like cells all graphically updated	X	X	X
Boolean shapes editing	X	X	X
Edge editing	X	X	X
Angles supported			
Orthogonal	X	X	X
Octagonal	X	X	X
All	X		X
Number of layers (max.)	64	Unlimited	64
Output format	GDSII, CIF, PG tape, E-beam.	GDSII Stream and CIF.	GDSI, GDSII, Applicon PG tape, Gerber, E-beam.
Description		<p>TEDI, TopSet's topological symbolic editor, is a tool for creating dense transistor level layouts as well as a tool for floor planning and chip composition. Transistor level designs are created using symbolic or "stick" notation, reducing the information on the screen to the minimum needed while still permitting the designer to quickly design dense, error-free cells. Since TEDI utilizes technology files, the designer need not worry about the intricacies of the process design rules and can instead concentrate on topological issues such as maximizing layout efficiency. The automatic COMPACTOR utility can be invoked and directed from the TEDI environment.</p> <p>GEDI, GeoSet's geometric editor, is used to produce libraries of dense, hand crafted leaf cells and functional blocks that require area and performance optimization. GEDI is an area-based polygon editor whose creation and editing commands allow blocks to be produced from polygons, boxes, and wires. CHECKER is used for design rules checking, circuit extraction, and computation of circuit parameters. Design rule checking and circuit extraction use edge-based scan-line algorithms driven by user-defined technology files.</p>	<p>MACRO language and basic-like programming language available for creation of proprietary commands and procedures. Database access through programming language.</p>



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Physical Layout Tools—Full Custom (Cont'd)**

Daisy Systems CHIPMASTER	Harris Semiconductor Harris/SDA Workstation page 4246	Mentor Graphics CHIPGRAPH	Racal-Redac ISIS
IBM PC/XT/AT, Daisy LOGICIAN 386/Personal LOGICIAN 386	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO	DEC VAX
X X		X X	X X
X X	X X	X X	X X
X	X X	X X	X X
X	X	X	X
X X X	X X X	X X X	X X
X X X	X X X	X X X	X
256	128	256	
GDSII, CIF, Applicon, Daisy Chipmaster Workstation.	Layout information is stored in SDA's database format. translation is provided to Calma STREAM format.	GDSII, CIF, E-Beam, PG tape, Chiplotter.	See Description.
<p>CHIPMASTER software is optimized for all aspects of VLSI design. It offers numerous design features including: built-in design rule checking and a graphics system optimized for IC layout. An open architecture that allows users to customize CHIPMASTER to their individual work environment. And, a choice of platforms to meet the cost/performance requirements of any organization.</p> <p>CHIPMASTER's mask editor, MAX, is a high performance polygon editor optimized for mask layout. This all-angle editor supports all geometric structures including circular geometries. Daisy's graphics subsystem makes editing polygons fast and easy. Algorithms for 45-degree and 90-degree angles are coded into hardware. MAX's intelligent repaint capability is also built into hardware: it only redraws where it has to, saving time.</p> <p>An online design rule checking (IRC) program runs inside of MAX. This catches and corrects errors quickly. IRC's locator function helps locate errors through a forms interface.</p>	<p>Harris supports full custom through the SDA tools LAYOUT, PDcheck, and PDextract fully integrated into the SDA Framework. LAYOUT provides the designer with full hierarchical design capability, multiple-windows, multiple circuit editing, and an extensive set of commands and options. A LISP/C-like graphical programming language is available for the development of personalized auto-layout procedures. PDcheck, coupled with Harris' design rule packages, give flat, or full hierarchical physical design rule checks either on-line or in batch mode. An incremental checking procedure and integrated graphical display of errors allow quick feedback to the designer during layout. PDextract is provided for extraction of complete device (real and parasitic) and connectivity information for use in ERC's and layout to schematic comparison.</p>	<p>Full custom IC design system. Supports MOS, bipolar, GaAs, etc. Supports linear and digital design.</p>	<p>A plot of all types of graphical data can be produced by simply creating a plotting window. ISIS can output to multi-color pen plotters or to electrostatic plotters, or, if required, plot files can be stored on magnetic tape.</p>

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Physical Layout Tools—Full Custom (Cont'd)			
Source	Scientific Calculations	SDA Systems	Silicon Compiler Systems
Tool Name	MEDS	LAYOUT	Generator Development Tools
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, DEC MICROVAX	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC MICROVAX, SUN
Hierarchical design			
Starting with floor plan	X		X
Starting with macros	X	X	X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Electrical rule checking			
Batch mode		X	X
On-line (Interactive)		X	X
Layout parameter extraction	X	X	X
Editing features			
Like cells all graphically updated	X	X	X
Boolean shapes editing		X	
Edge editing	X	X	
Angles supported			
Orthogonal	X	X	
Octagonal		X	
All		X	X
Number of layers (max.)	4095	128	User defined
Output format	Calma DC, LU, STREAM.	STREAM, EDIF, Versatec.	GDSII, EDIF
Description	<p>The MEDS System is a hierarchical IC layout system that supports, in a single system, the full spectrum of IC design methodologies including gate array, standard cell and full custom designs. It is a netlist-guided and design-rule constrained physical design system that assures correct-by-construction placement and routing results. Advanced layout algorithms, together with powerful interactive graphics facilities and extensive user control, enable the IC designer to tackle the largest and toughest layout problems. The placement capability includes an automatic placement algorithm based on a unique simulated annealing implementation and a "force-directed" constructive placement algorithm with manual seeding. An optional iterative placement improvement phase is provided. Intelligent routers are able to "see" the internal geometries of cells and route over, around or through a cell without violating design rules. The system will support both channelled and channelless (sea-of-gates) architectures.</p>	<p>SDA's Graphics Editor, LAYOUT, is a powerful physical design tool for implementing VLSI integrated circuits. Full hierarchical design capability, multiple-window, multiple-circuit editing, and a rich set of commands and options provide the designer with a state-of-the-art layout design environment. LAYOUT is fully integrated SDA's full suite of engineering, design, and verification tools.</p> <p>LAYOUT's flexibility accommodates the diverse requirements of full custom, structured custom, standard cell, and macro cell design methodologies. Optionally available is a structure compiler to build complex circuit blocks such as PLAs, ROMs, RAMs and datapaths within the layout environment. Many user-configurable features and setup options allow LAYOUT's human interface to be tailored to the designer's exact needs. A powerful graphics programming language allows the user to develop custom command macros for increased layout productivity. Built-in interfaces allow data translation between LAYOUT and other physical design systems providing for easy integration of LAYOUT into existing environments.</p>	<p>The Generator Development Tools (GDT) can be used by IC designers to create their own silicon compilers. The power of the GDT is based on a new language, L, developed by SDL. Generators, produced using L, can accept parameters from a user and develop completely custom layouts. GDT can also be used by logic designers and system designers to create larger functional blocks or complete chips using their own or Silicon Design Labs' basic functions. GDT features a Macintosh-like user interface, on-line design rule checking and an integrated hierarchical mixed-mode functional/circuit/fault simulator. GDT also includes a complete standard cell library and automatic place and route tools as well as PLA generation tools.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Physical Layout Tools—Full Custom (Cont'd)

Silvar-Lisco PRINCESS	Tektronix CAE Systems LEIA page 4658	Valid Logic Systems Inc. ValidBLOCKS page 4660	Valid Logic Systems Inc. ValidCOMPOSE page 4660
APOLLO, DEC VAX, IBM MAINFRAME/MINI	DEC VAX, DEC MICROVAX, TEKTRONIX	DEC MICROVAX, SUN, Valid SCALDsystem	DEC MICROVAX, SUN
X X	X	X X	X X
X X	X	X	X
X X	X	X	X
X	X		
X X X	X X X	X	X
X X X	X X X	X X	X
limited by CPU	255	3	Unlimited
EDIF, GDSII, CIF, E-Beam, Applicon, Computer-vision.	LEIA Binary, Calma GDSII.	GDSII, CIF, EDIF	GDSII, CIF, EDIF
	LEIA is a layout editor designed primarily for full custom integrated circuit design. LEIA's flexible user interface provides the designer with multiple windows, pop-up menus and the ability to customize a real-time user configurable menu environment to promote ease of use in layout for even the most complex VLSI circuits.	ValidBLOCKS is an advanced layout tool for the interactive placement and automatic routing of complex integrated circuits. ValidBLOCKS is an excellent semi-custom place and route tool for in-house use. Its fast, complete routing makes interactive design practical.  Designs can be realized using standard cell libraries, full custom blocks, or a combination of the two thereby making it an ideal tool for systems designers, IC engineers, and layout designers. With ValidBLOCKS you can achieve the same density as that produced by manual routing in a fraction of the time.  * Provides fast routing performance * Performs automatic sizing * Performs automatic sizing and routing of power busses * Supports three interconnect layers * Unconstrained gridless routing for maximum density * Supports hierarchical design methodology * Integrated with Valid's family of design tools	ValidCOMPOSE is a chip design tool that allows chip designers to construct new chips out of existing cells (from a cell library, compiled cells from a silicon compiler, or hand-crafted full-custom cells). With it, the designer can manipulate cell placement and routing, and can automatically compact the chip to minimum size while automatically following all design rules.  ValidCOMPOSE shares a common database with the ValidGED schematic editor and ValidLED IC layout editor. ValidCOMPOSE reads the functional schematic, accesses symbolic representations of the geometric cells from the cell library, and displays their connectivity. The chip designer employs its editing capabilities to optimize cell placement.  ValidCOMPOSE can be rules-driven, by specifying rules on the original schematic with ValidGED. These rules can drive both placement and routing (e.g. critical paths, wire width). Once cells are placed, ValidCOMPOSE automatically compacts the chip into the smallest possible space. Both automatic and interactive routing capabilities are provided.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Physical Layout Tools—Full Custom (Cont'd)			
Source	Valid Logic Systems Inc.	VIA Systems	VLSI Technology
Tool Name	ValidLED	ChipTool	VTIcustom
FOR DETAILED DATA SEE:	page 4660		page 4665
Tool residence	DEC MICROVAX, SUN, Valid SCALDsystem	APOLLO, DEC MICROVAX, SUN	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN
Hierarchical design			
Starting with floor plan	X	X	
Starting with macros	X	X	X
Design rule checking			
Batch mode		X	X
On-line (Interactive)			
Electrical rule checking			
Batch mode		X	X
On-line (Interactive)			
Layout parameter extraction		X	X
Editing features			
Like cells all graphically updated	X	X	X
Boolean shapes editing	X	X	
Edge editing	X	X	
Angles supported			
Orthogonal	X	X	
Octagonal	X	X	
All	X	X	X
Number of layers (max.)	255	256	Designs with over 20 layers achieved
Output format	GDSII, CIF, EDIF	GDSI, GDSII, PG tape, E-Beam, CIF, Applicon 860, 870, EDIF, 10 different PG and E-Beam formats.	CIF.
Description	<p>ValidLED is an editor specifically designed for creating custom chip physical layouts. It may also be used to edit the output of the Silicon Design System to optimize chip performance or size, and automatically generates chip geometries for chips assembled using ValidCOMPOSE.</p> <p>ValidLED supports hierarchical design in cell definition; a bounding block description of the circuit initially can be defined as a number of functional cell structures and subsequently expanded into smaller functional cells. The actual cell is created by painting the individual layers with the cursor. Groups of cells then can be combined and interconnected until the entire design is defined by a single cell.</p> <p>ValidLED features an extensive set of high-level commands for cell expansion, replication, and manipulation, available through a cursor selectable menu. ValidLED includes numerous features to support and simplify integrated circuit design.</p>	<p>ChipTool is an interactive physical layout editor for very large scale integrated circuits. Interactive editing features permit design manipulation using cells to facilitate the management of complex geometry in a highly efficient environment. For the layout designer, ChipTool combines all the functions necessary to translate a schematic design into an efficient IC layout, ready for input to a pattern generator. ChipTool is available for the UNIX-based Sun Microsystems product, and the ULTRIX-based VAXstation II/GPX.</p> <p>Features: 250 design layers; viewing by layer; recursive commands; rubberbanding; "ghost" image during edit; multiple windows; cell nesting; GDSII and Via format I/O; VIATools operator environment.</p>	<p>VTIcustom provides the user with the necessary tools to do full-custom or symbolic layout. The hierarchical capabilities of the layout editor allow the user to edit any cell from any level of his design. The user can run design rule checks from the layout editor and then superimpose the errors over the design for easy editing. In addition, there is a rule checker capable of insuring that the layout is compatible with VLSI's standard cells. A companion tool to the layout editor is the symbolic sticks editor allowing rapid transistor-level design by automatically spacing the layout to meet the design rules. The result is a fully compacted, design-rule-correct cell.</p>



DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Programmable Logic Device Development Systems			
Source	Aldec	Altera	Altera
Tool Name	SFLD	A + PLUS	PLCAD-SUPREME
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	IBM PC/XT/AT	IBM PC/XT/AT
Allowed input formats			
Boolean equations	X	X	X
Truth tables	X	X	X
State diagrams	X	X	X
Mixed input formats		X	X
Logic reduction		X	X
Automatic DeMorgan conversion		X	X
Output formats			
JEDEC fuse map	X	X	X
Signetics program table			
Other			
PLD verification			
Functional simulation		X	X
Fault grading		X	X
Automatic test pattern generation			
Read device fuse map		X	X
Accepts net list from:		PCAD PC-Caps, Futurenet DASH-2.	Viewlogic Workview, PCAD CAE1 & PC-CAPS, FutureNet DASH
Links to PLD programmers		Data I/O 29B, Stag ZL30.	Data I/O 29B, Unisite 40, Stag ZL30
PLD manufacturers supported		Altera, Intel.	Altera, Intel
Description	Spike Free Logic Designer (SFLD) allows designers to program PAL and PLD devices in five domains: logic equations, timing diagrams, truth tables, state diagrams and direct fuse blowing. The design development is fully interactive. A user can monitor, via timing diagrams, the internal operation of the programmable logic device and correct the source of spikes. Required: Standard IBM PC w/ color /graphics adapter, 512 kBytes of RAM.	Automatic pin assignments & logic fitting.	PLCAD-SUPREME is a complete hardware and software solution that enables circuit designers to develop and implement custom logic circuits with Altera EPLDs. The system contains A + PLUS, Altera Programmable Logic User Software, which allows a wide variety of design input methods that suite the particular logic design task. These include Netlist, Boolean Equation, Schematic Capture, and State machine design entries. A + PLUS includes a Design Processor which transforms the input format to optimized code used to program the targeted EPLD.  The Design Processor implements logic minimization, automatic EPLD part selection, architecture optimization, and design fitting. A + PLUS also allows MacroFunction design capability and functional simulation. In addition to A + PLUS, the system also contains a programming card and master programming unit used for device programming. The programming card fits into the expansion slot of the PC and connects via ribbon cable to the master programming unit. The programming hardware is fully software controlled via A + PLUS.

Bold face indicates data is provided in the page noted

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Programmable Logic Device Development Systems (Cont'd)			
Source	Altera	Case Technology	Daisy Systems
Tool Name	PLDS-SAM	CUPL (see P-CAD)	PLDMASTER
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	APOLLO, AT&T, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN	IBM PC/XT/AT, Daisy LOGICIAN 386/Personal LOGICIAN 386
Allowed input formats			
Boolean equations		X	X
Truth tables		X	
State diagrams	X	X	X
Mixed input formats	X	X	
Logic reduction	X		X
Automatic DeMorgan conversion		X	X
Output formats			
JEDEC fuse map	X	X	X
Signetics program table			X
Other			
PLD verification			
Functional simulation	X	X	X
Fault grading			X
Automatic test pattern generation			
Read device fuse map	X	X	X
Accepts net list from:		Case Technology	Daisy's ACE schematic capture system
Links to PLD programmers		ABL	Data I/O 29B-LOGI, Data I/O 29B-UNI, DIGILEC-860, DIGILEC-803-FAM-12, DIGILEC-803-FAM-52, DIGILEC-824, DIGILEC-825
PLD manufacturers supported	Altera, Waferscale Integration	AMD, Altera, Fairchild, Harris, Intel, Lattice, MMI, National Semiconductor, Signetics, TI, VLSI Technology	MMI, Signetics, Altera, Intel, AMD
Description	<p>The Altera PLDS-SAM (Programmable Logic Development System) represents a complete software and hardware solution to implementing State Machine and Microcoded applications into Altera's SAM family of Function-Specific EPLDs. PLDS-SAM is a comprehensive, easy to use system that encompasses design entry with SAM + PLUS, design debugging with SAMSIM, and device programming with the Altera programming hardware.</p> <p>The SAM + PLUS processing software accepts two forms of design entry, State Machine and assembly language, and automatically generates an industry standard JEDEC file. SAMSIM is an interactive functional simulator created specifically for verification of State Machine and Microcoded designs implemented in SAM EPLDs. The programming hardware consists of an Altera programming card, a Master Programming Unit, and programming adapter for programming the SAM EPLDs.</p>	<p>A high level, universal design language that allows logic designs to be expressed as state machines, Boolean equations or function tables. Programmable logic can be designed for any target device.</p>	<p>Daisy Systems' new software lets users design, test and simulate programmable logic devices (PLDs) as part of an entire system. Daisy's PLD Master offers a significant improvement over traditional methods of design, which allow PLDs to be created only as stand-alone components. With Daisy's new software, users can enter logic in a number of different forms, compile the logic patterns or fuse maps in a convenient language, and then simulate the behavior of the device in a system. Modifying the design during the creation process dramatically reduces debugging time, and ensures that the design will work right the first time. Design entry methods range from graphic state machine and schematics to high-level languages. PLD Master supports any logic compiler that generates a standard JEDEC file. Three universal design compilers come standard: Monolithic Memories' PALASM, Data I/O's ABEL and Signetics' AMAZE. The variety of design methods and compilers that can be used with PLD Master enables designers to use the methods, devices and compilers with which they are most familiar.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Programmable Logic Device Development Systems (Cont'd)

Data I/O (FutureNet) ABEL page 4651 APOLLO, DEC VAX, IBM PC/XT/AT, SUN	FutureNet (Data I/O) Personal Silicon Foundry page 4651 IBM PC/XT/AT	Intel iPLDSII page 4257 IBM PC/XT/AT	International CMOS Technology PDS-1 PEEL page 4259 IBM PC/XT/AT
X X X X	X X X X	X X X X	X
X	X	X	
X	X	X	
X X	X	X	X
X X X	X X X	X	X X X
X	X	X	X
FutureNet DASH.	DASH (FutureNet).	Viewlogic, Omation SCHEMAll, P-CAD, Future-Net, and OrCad	N/A
Data I/O.	All that accept JEDEC format (standard #3); Data I/O.	Intel iUP200A/iUP201A, Intel iUP-PC, Data I/O, Stag, Oliver Advanced Engineering, Kontron, Digelec	All programmers that accept JEDEC files
MMI, AMD, Signetics, TI, Lattice, VTI, Ricoh, National, Sprague, Harris, Altera, Cypress.	All.	Intel, Altera	International CMOS Technology
ABEL is a complete logic-design software tool for programmable logic. ABEL combines a natural, high-level design language with logic reduction, simulation, and error checking in an integrated package to help a logic designer throughout the design process. The ABEL design language lets you describe logic with Boolean equations, truth tables, or state diagrams, or with any of these. Meaningful names can be assigned to signals, signals can be grouped into sets, and macros can be used to simplify logic descriptions- all making the logic design easy to read and understand.	Claimed to be the first complete programmable logic development system on the market, the Personal Silicon Foundry provides complete design, programming and testing for virtually every PLD and PROM available. Design description for the PLD can be entered using any combination of schematics, Boolean equations, thruth tables, or state diagrams. Once the description is entered, The Personal Silicon Foundry automatically performs logic reduction, simulation, fault analysis, and test vector generation, leaving the designer free to concentrate on the design. Once the files have been tested and verified, a JEDEC-standard load file is sent to a Data I/O programmer where a device is programmed. Finally, the device is tested once again by using testing routines provided to the programmer. Automatic documentation of the entire process is performed throughout the design and testing cycle.	Intel's Programmable Logic Development System II (iPLDSII) comprises a complete desktop EPLD development environment including a variety of design entry formats, logic minimization, and desktop programming. Design entry includes Boolean logic entry, state machine design language, and schematic capture. Once the design is entered, the netlist is submitted to the Logic Optimizing Compiler for design minimization based on U.C. Berkeley's Espresso minimization algorithms. After minimization, iPLDSII intelligently fits the design into the target device using the industry-standard JEDEC programming file format. iPLDSII includes a PC form factor programmer card andprogramming adaptors to program the designer's choice of Intel EPLDs. Additional adaptors may be purchased to program other EPLDs as well as EPROMs, E2PROMS, and Intel Mirocontrollers.  In addition to popular, high-end schematic capture packages such as Viewlogic, P-CAD, and FutureNet, Intel offers SCHEMAllPLD, a low-cost full-function schematic capture package that includes a special EPLD design manager. Designs may be entered using familiar TTL macros or user-defined macros which are then automatically converted into equivalent EPLD logic.  Intel also offers an on-line Bulletin Board system for registered users.	The PDS-1 PEEL (Programmable Electrically erasable Logic) development system includes an editor, logic assembler, translator, programmer, and logic tester. It offers several options in designing with PEEL devices. As an example, PLD designs can be automatically translated and programmed into a PEEL device. Thus, users can develop new designs using most logic compiler or assembler software that supports conventional PLDs.  Aside from device translation, the system supplies the tools for designing from concept to silicon. These include a built-in word processor for design entry, APEEL Boolean logic assembler (sum-of-products equation forms), and a complete PEEL device programmer box and enhanced logic tester. In addition, otherthird-party PLD logic compilers can be used, such as ABEL 2.1 from Data I/O.

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Programmable Logic Device Development Systems (Cont'd)			
Source	International CMOS Technology	Kontron	Lattice Semiconductor
Tool Name	PEK-1 PEEL	LOG/ic + EPP-80 PLD Programmer	Design Development Kit
FOR DETAILED DATA SEE:	page 4259		
Tool residence	IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, Kontron AT compatible & Siemens	IBM PC/XT/AT
Allowed input formats			
Boolean equations	X	X	X
Truth tables		X	
State diagrams		X	
Mixed input formats		X	
Logic reduction		X	X
Automatic DeMorgan conversion		X	X
Output formats			
JEDEC fuse map	X	X	X
Signetics program table			
Other			
PLD verification			
Functional simulation	X		
Fault grading			
Automatic test pattern generation	X		
Read device fuse map	X		X
Accepts net list from:		Kontron KAD System	
Links to PLD programmers	All programmers that accept JEDEC files	Kontron EPP-80 Universal Device Programmer	Programmer included as part of development system
PLD manufacturers supported	International CMOS Technology	Advanced Micro Devices, Altera, Cypress Semiconductor, Fairchild, Harris, Intel, Lattice, Monolithic Memories, National, etc.	Supports entire family of Lattice GAL devices (GAL16V8, GAL20V8, GAL39V18, ispGAL16Z8)
Description	PEEL device evaluation system, includes: tutorial software, translator, APEEL assembler, editor, user's manual, data sheets, support information, discount certificate.	LOG/ic is a software design package for PAL/GAL type devices for design workstation host systems. Schematics can be entered using the Kontron KAD schematic capture package, or directly via netlist entry using the Netlist Editor. The system also accepts boolean equation, truth table, or state diagram entry.  The Kontron EPP-80, a universal PROM/PLD device programmer, can also be directly connected into the Kontron KAD System.	The Design Development Kit contains everything needed (hardware and software) to bring a design from concept to completion. The programming fixture interfaces to PC-compatible computers via the RS-232 port. Software included consists of a logic assembler and a menu driven programmer interface. The devices supported by the kit are: GAL39V18, GALV16V8, GAL20V8, ispGAL16Z8. Sample devices are included.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Programmable Logic Device Development Systems (Cont'd)

Monolithic Memories PALASM2	P-CAD CUPL	P-CAD PC-CUPL	Signetics AMAZE page 4300
DEC VAX, DEC MICROVAX, IBM MAINFRAME/ MINI, IBM PC/XT/AT, Daisy Sys.and Valid Logic workstations	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, NEC PC, SUN, Valid	IBM PC/XT/AT	IBM PC/XT/AT
X X X	X X X X		X X X X
X	X	X	
X	X	X	X
X	X X X	X X X	X X X
X	X	X	X X X
X			X
		PCAD PC-CAPS.	AMAZE will convert netlist files generated from FutureNet or OrCad schematic capture packages.
All programmers which accept JEDEC files.	Data I/O 29B, Stag ZL30, PPZ, Valley Data OAE, Structured Design, Digelec, Promac, Kontron, Inlab, Varix, Sunrise, Quantec.	Data I/O, Stag, Valley Data, OAE, Structured Design, Digelec, Promac, Kontron, Inlab, Varix, Sunrise, Quantec.	PC to programmer interface is accomplished through a menu driven module. AMAZE is capable of converting JEDEC files resident on disk to AMAZE files and vice versa.
Monolithic Memories.	MMI, National, AMD, TI, Altera, Lattice, Signe- tics, Cypress, Harris, Intel, VTI, Panatech, Ricoh, Fairchild, Sprague.	MMI, National, AMD, TI, Altera, Lattice, Signe- tics, Cypress, Harris, Intel, VTI, panatech, Ricoh, Fairchild, Sprague.	Signetics entire line of Programmable Array Logic, Programmable Logic Array, Program- mable Logic Sequencer/MacroLogic.
PALASM2 software offers the design- er increased design flexibility with the option of creating a design by supplying Boolean or State equa- tions or data in tabular format. The powerful PAL device Design Specification syntax has the ad- vantage of being flexible enough for complex designs, without com- promising ease-of-use. The basic operators INVERT, AND, OR, and EXCLUSIVE OR can be used to de- scribe any logic function using Boolean equations. The syntax for State equations and Tabular for- mat is equally easy to use. In addi- tion, the new PALASM2 software accepts inputs from the original PALASM program. Old designs may be brought up to date quickly and easily by calling up PALASM2 software's conversion program.	CUPL is a universal logic compiler for PLD design. Its high level capabili- ty allows logic descriptions to be written in truth table, state ma- chine, or high level equations. Uni- versal capability allows design por- tability among different PLD fami- lies. CUPL provides support for all popular PLDs from many manu- facturers (PAL, IFL, EPLD, EEPLD, etc.) and produces standard JED- EC format output compatible with popular logic programmers. Also supports PROMs used as logic de- vices. (Note: output format in- cludes ASCII HEX for PROMs.)	PC-CUPL allows engineers to design PLDs using P-CAD's schematic capture program, PC-CAPS, as a front-end for logic design. PC- CUPL consists of CUPL, P-CAD's schematic capture program, as a front end for logic design. PC- CUPL consists of CUPL, P-CAD's PLD design software, NX-CUPL, a netlist interface from PC-CAPS to CUPL, and a library of symbols op- timized for PLD design. Previously, designers had to represent their PLD designs in numeric and textu- al statements and manually enter them into CUPL via an alphanu- meric keyboard. With schematic capture, logic elements are repre- sented graphically, and the design can be built using a mouse driven menu and symbols library. CUPL is a high-level programming lan- guage for PLDs. It supports all popular PLD devices, including PAL, EPLD, EEPLD, IFL and PROM architectures. CUPL also gener- ates a standard JEDEC download file used by most existing PLD de- vice programmers. PC-CUPL runs on IBM PC/XT, PC/AT and com- patible machines. (Note: input via schematic capture)	AMAZE design software was devel- oped by Signetics Corporation to support its entire line of program- mable logic devices. The software package consists of four double- sided, double density 5 1/4" flop- py diskettes that run on all MS- DOS 2.1 or later operating sys- tems.  AMAZE consists of five user- definable menu-driven modules that satisfy the fundamental PLD design, simulation, test vector generation, editing and program- ming requirements. 1. Designs can be entered into AMAZE by schematic capture, state equation, boolean equation, and program ta- ble. 2. AMAZE is capable of auto- matically selecting vectors for de- sign simulation or the user can in- teractively enter vectors and ob- serve the results. 3. Test vectors are automatically generated based on the defined fuse map. A 'log' file stores I/O values during simu- lation. 4. A menu-driven module is capable of down-loading design files in JEDEC format and down- loading simulator 'log' files togeth- er with design files. 5. PAL designs can be automatically converted to a Signetics OAL-type or PAL/PLS device.

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## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Programmable Logic Device Development Systems (Cont'd)			
Source	Trimeter Technologies	Valid Logic Systems Inc.	
Tool Name	Logic Consultant	ValidPLD	
FOR DETAILED DATA SEE:		page 4660	
Tool residence	APOLLO	DEC MICROVAX, IBM PC/XT/AT, SUN, Valid SCALDSsystem	
Allowed input formats			
Boolean equations	X		
Truth tables	X	X	
State diagrams		X	
Mixed input formats		X	
Logic reduction	X	X	
Automatic DeMorgan conversion		X	
Output formats			
JEDEC fuse map		X	
Signetics program table		X	
Other	X		
PLD verification			
Functional simulation		X	
Fault grading		X	
Automatic test pattern generation		X	
Read device fuse map		X	
Accepts net list from:		ABEL, CUPL, PALASM	
Links to PLD programmers		see ABEL, CUPL, PALASM	
PLD manufacturers supported		see ABEL, CUPL, PALASM	
Description	The ValidPLD product line includes libraries of unprogrammed models for PLDs such as PAL20s, PAL24s, the AMD22V10 and IFLs. The libraries are augmented by the ValidPLD Programmer, a software package which automatically generates user-programmed timing verification and simulator models from the output of the user's preferred PLD software -- either PALASM, ABEL, or CUPL. A user can program and reprogram models as required without having to make new library entries or modify schematics, thereby allowing for complete control and flexibility of models.		
	The Logic Consultant accepts input logic designs as netlists from Mentor Graphics systems with generic or foundry-specific symbols, as boolean equations or in PLD format.		
	The Logic Consultant first minimizes the design's logic and evaluates timing constraints. Then, using expert system technology, the Logic Consultant selects the optimal combination of cells and macrocells from the targeted ASIC library which provide the required logic functionality with the highest performance and/or the least possible area.		
	The Logic Consultant's Schematic Analyzer allows you to then quickly estimate propagation delays through selected signal paths, find the longest and shortest delay paths and calculate the associated timing delays of both the high-to-low and low-to-high signal changes.		



DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Silicon Compilers and Cell Generators			
Source	Daisy Systems	ES2/US2	Ferranti Interdesign
Tool Name	SILICONMASTER	SOLO 1000/SOLO 1200	Silicon Design Sys. ULASILCOM
FOR DETAILED DATA SEE:			
Tool residence	Daisy Siliconmaster	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, VAXstation 1200	DEC VAX, DEC MICROVAX
Compilable functional blocks			
Datapath	X		
Complex logic	X	X	X
Memory	X		X
Pads	X	X	X
Test	X	X	X
Random logic	X	X	X
Compile via behavioral description			
Circuit simulation		X	X
Functional simulation	X	X	X
Cells parameterized for			
Function		X	X
Speed		X	X
Load		X	X
Power dissipation		X	X
Process independent		X	
Path length minimization	X	X	X
Layout parameter extraction	X	X	X
Estimates power dissipation	X	X	X
Output formats	GDSII, CIF.	CIF	PG formatted tapes.
Technologies supported	Dual layer CMOS, single layer NMOS.	CMOS (single and double layer metal)	Ferranti Fab 1,2 & 3 collector diffusion isolation.
Foundries supported	Gould AMI, VLSI Technology, IMP, NCR, GTE Semiconductor.	European Silicon Structures, AMI, TI, Philips	Ferranti Interdesign.
Description	Uses software from Silicon Compilers, Inc.	The SOLO 1000/SOLO 1200 package is intrinsically a silicon compilation and cell generation package.	

DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Silicon Compilers and Cell Generators (Cont'd)			
Source	FutureNet (Data I/O)	Harris Semiconductor	NCR Microelectronics
Tool Name	DASH-GATES	Compilers	VIGEN Series
FOR DETAILED DATA SEE:	page 4651	page 4246	
Tool residence	IBM PC/XT/AT	APOLLO, DEC MICROVAX, MASSCOMP, SUN	Popular workstations
Compilable functional blocks			
Datapath			X
Complex logic			X
Memory		X	X
Pads			
Test			
Random logic		X	
Compile via behavioral description	X		
Circuit simulation			
Functional simulation	X	X	
Cells parameterized for			
Function		X	X
Speed		X	
Load			
Power dissipation			
Process independent	X		
Path length minimization	X		
Layout parameter extraction			X
Estimates power dissipation			
Output formats	Schematic w/JEDEC standard #12 macrocells + PLD JEDEC standard #3.		
Technologies supported	PLDs, gate Arrays, Standard cells.	2 micron CMOS, 2 micron Rad Hard CMOS	
Foundries supported	All who support JEDEC standard #3 or #12.	Harris Semiconductor	NCR Microelectronics.
Description	DASH GATES is claimed to be the first silicon compiler to accept high-level functional descriptions as inputs and then convert them into a schematic and a net list as required by gate-array foundries. For example, it accepts descriptions of circuit elements like multiplexers, decoders, and state machines in terms of equations, truth tables and state diagrams. The compiler, which runs on an IBM AT and compatibles, consists of a set of software tools that reduce the time and cost of designing, optimizing, and verifying a circuit. The designer enters a circuit using the compiler's ASIC design language. Then, once the user tests and debugs the design, the compiler automatically runs logic synthesis algorithms that minimize the number of gates, factors out redundancies to trade off speed and circuit size, and creates schematic and netlist output for the foundry.	Synchronous RAM Compiler- generates a synchronous, high performance RAM of up to 16K bits. User selectable parameters such as speed, bit configuration and optional tristatable outputs provide unique design specific compiled cells. Features 20ns access time to military temperatures. RAMS can be cascaded to allow addressing of more than 16K bits.  Asynchronous RAM Compiler- generates an asynchronous, high performance RAM of up to 16K bits. Configurable to customer's specification on Harris' Rad Hard process to full military specs.  ROM Compiler- generates a high performance ROM of up to 64K bits to the customer's specific configuration. The inputs and outputs of the compiled ROM can be selected as dedicated or multiplexed. The access times are 20ns at military temperatures. As with RAM compilers, ROMs are cascaded to address more than 64K bits.	For the design of NCR Microelectronics cell-based designs. VIGEN brings function generators/compilers from a "full" silicon compiler environment to a familiar semicustom design environment also supporting gate array and standard cell design on leading workstations. The user chooses his function, such as COUNTER, from the VIGEN family and configures it to his requirements by answering prompts (number of bits, up or down count, preload value, etc.). VIGEN automatically creates the schematic symbol, logic simulation model and VITA model. The user proceeds with his design as if the configured VIGEN function had always been in the library. The customer also sends the Configuration Files he has interactively produced to NCR for generation of the configured functions' transistor-level layouts. These generated "blocks" are then ready for place-and-route of the entire ASIC device. With the initial release of VIGEN added to the Verification Package, the user has these generated functions (as of January, 1987): RAM, ROM, PLA, ALU, Counter, Multiplexer, Shift Register, Dual-Port RAM. Optional high-level VIGEN functions (as of January, 1987): CRT Controller, EE-PROM Generator, 80C300 Microcontroller. Enhancements and additions to the basic set and optional VIGEN products will be released on a regular basis.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Silicon Compilers and Cell Generators (Cont'd)

SDA Systems Module Generation Development	SDA Systems Structure Compiler	Seattle Silicon Concorde ASIC Compiler	Silicon Compiler Systems Generator Development Tools
APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, Valid Logic, Mentor Graphics	APOLLO, DEC MICROVAX, SUN
X X X	X  X	X X X X X X	X X X X  X
		X	
		X	X
X		X	X
X		X X X X	X
	X	X	X
		X	X
	X	X	X
X		X	X
GDSII, netlists user defined	STREAM	GDSII, CIF, HP Plotter, Versatec.	GDSII, EDIF.
CMOS, NMOS, ECL, Bipolar, any IC technology	All	1,2,3 micron HCMOS p-well, n-well, twin-tub, with 1 or 2 layer metal and 1 or 2 layer poly.	GDT supports any user defined mask definable technology.
N/A	N/A	Motorola, NCR, AMI, ITT, Ricoh, National, UTMC, Rohm, GE, Samsung	
<p>Using the range of tools within the SDA Design Framework, IC manufacturers can design and build their own proprietary module generators. A powerful interactive language, SKILL, combined with a special cell assembly tool, the Structure Compiler, automatically builds cells from high-level user parameters. Generators build complete IC cells including schematic symbol, simulation model, documentation, layout, and place and route abstract.</p> <p>SDA's front-to-back IC design system provides a complete delivery system for generators and silicon compilation. Generators may be called during schematic entry, and the resulting design simulated when complete. Automatic place and route assembles the design, including the generated cells. Finally, post-layout parasitics can be extracted to ensure proper performance.</p>	<p>SDA's Structure Compiler is a flexible tool that optionally exists with SDA's layout editor to create complex circuit blocks such as RAMs, ROMs, ALUs, and datapaths from a library of tile cells.</p> <p>Circuit blocks generated by the Structure Compiler are easily modified by changing a simple personality file for quick full custom engineering revisions. Since the assembly of the circuit blocks are based on a "relational shape" template, the same design can be re-generated in moments by substituting a new tile cell library making technology revisions fast and easy.</p>	<p>The Concorde ASIC Compiler offers ASIC designers an economical and efficient path for high function digital, analog, and mixed digital and analog IC's in a CAE workstation environment. Concorde's exclusive dynamic compaction system creates circuit layout with custom density in multiple processes. Schematic capture and simulation occur through automatic database links with workstation tools from Valid Logic and Mentor Graphics. Integrated timing analysis and fully automatic placement and routing for random blocks and standard cells are provided in the compiler environment.</p> <p>Concorde is intended for the designer who is now using standard cells, gate arrays, or board-level solutions, and who wishes to create high performance custom parts that are smaller, more efficient, and less expensive to manufacture.</p>	<p>The Generator Development Tools (GDT) can be used by IC designers to create their own silicon compilers. The power of the GDT is based on a new language, L, developed by SDL. Generators, produced using L, can accept parameters from a user and develop completely custom layouts. GDT can also be used by logic designers and system designers to create larger functional blocks or complete chips using their own or Silicon Design Labs' basic. GDT features a Macintosh-like user interface, on-line design rule checking and an integrated hierarchical mixed mode functional/circuit/fault simulator. GDT also includes a complete standard cell library and automatic place and route tools as well as PLA generation tools.</p>

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Silicon Compilers and Cell Generators (Cont'd)			
Source	Silicon Compiler Systems	Silicon Compiler Systems	Unicorn Microelectronics
Tool Name	GENESIL	GENESIS	COMPILE
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, Daisy and Mentor workstations	APOLLO, DEC VAX, DEC MICROVAX	DEC VAX, DEC MICROVAX
Compilable functional blocks			
Datapath	X		X
Complex logic	X		X
Memory	X		X
Pads	X		X
Test	X		X
Random logic	X		X
Compile via behavioral description		X	
Circuit simulation	X		X
Functional simulation	X	X	X
Cells parameterized for			X
Function	X		
Speed	X		
Load	X		
Power dissipation	X		
Process independent	X		X
Path length minimization	X	X	X
Layout parameter extraction	X	X	X
Estimates power dissipation	X	X	X
Output formats	GDSII, CIF.	GDSII, CIF.	SILOS simulation models, CIF/GDSII, HSPICE circuit models.
Technologies supported	CMOS n-well, CMOS p-well, CMOS twin-tub, NMOS.	CMOS, n-well, p-well, VHSIC, 1.25 micron and 3 micron dual metal CMOS, 2 micron and 3 micron NMOS.	1.5 - 3.0 micron double metal single poly CMOS.
Foundries supported	Gould, VTI, Motorola, National, NCR, SGS, VTC, RCA, Honeywell, Matra-Harris, IMP, MOSIS, Ricoh, Seeq.	Gould AMI, GE, Honeywell, NCR, IMP, Seeq or user's process.	Gould Semi, NCR, IMP, Seiko, United Microelectronics Corp.
Description	<p>The GENESIL Silicon Development System includes all the necessary tools to complete the design of an integrated circuit: design definition and edit, simulation, timing analysis, placement and routing, and database management.</p> <p>The GENESIL System is available in single user through 10-user configurations and is currently available on VAX, MicroVAX, Apollo, and Daisy hardware platforms. NMOS and advanced two layer metal CMOS function sets are available on the GENESIL system. Circuits designed on the GENESIL System can be manufactured in either technology at a number of Silicon Compiler Systems Inc.franchised foundries.</p>	<p>The GENESIS Compiler Development System contains the tools which enable the IC designer to create parametric compilers which operate in the GENESIL design environment. The compiler development tools include: geometric model synthesis, timing model synthesis, functional model synthesis, power model synthesis, logical design rule model, and a human interface design language plus a comprehensive design verification environment.</p>	<p>Using the structural compilation methodology, design engineers may choose from a high level library which includes configurable core microprocessors, core supercell peripherals, datapath modules, parameterized RAM, ROM and FIFO. The COMPILE CMOS library contains the following user-configurable Datapath Modules which consist of the following Functional Units: Full Function ALU, Input/Output Steering Unit, Shift/Rotate Functional Unit, Barrel Shifter, Register File, Incrementer/Decrementer, Parity Generator/Checker, Bit Mask, Multiplexer, Bus Breaker and Transceiver. Designers may specify an ALU of any bit width, along with the required data manipulations and flag requirements. The COMPILE MODULE GENERATOR automatically generates logic simulation files, and the completed physical layout database. Datapath Modules support dual-bus oriented, register transfer operations. It supports 32-bit wide data operations at 15 MHz clock frequency, based on two non-overlapping clocks which cyclically set up and evaluate each unit stage and pipeline along the datapath.</p> <p>The COMPILE CMOS Library contains the following LSI-Level configurable core microprocessors: 29C01 microprocessor slice (any width), 29C03 upgraded 29C01 super slice, 29C10 microprogram controller, 80C51 microcontroller.</p>



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Silicon Compilers and Cell Generators (Cont'd)			
VLSI Technology VTIcellLib page 4665			
APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN			
X X X X  X  X  X			
X			
X			
X			
X			
X X X   X  X  X			
X			
X			
CIF.			
2 micron CMOS double metal.			
VLSI Technology.			
VTIcellLib is the interface to the VLSI cell libraries. With this tool the user can specify parameter values and display parameter properties for cell compilers and functional models. It can handle user-written functional models as well as those supplied in the VLSI libraries. VTI-cellLib compiles cells immediately or produces a command file to compile cells later.			

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
IC Layout Verification Tools			
Source	Calma	Calma	Clarity Systems
Tool Name	ECAD	Fast Mask Engine	GeoSet
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, Calma Fast Mask Engine	Calma Fast Mask Engine	APOLLO
Hierarchical methodology	X	X	X
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)			X
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)			X
Layout debugging	X		X
Layout vs. schematic checking	X	X	X
Layout parasitic extraction	X	X	X
Layout vs. layout checking	X	X	X
Output format	GDS II STREAM.	All major PG E-Beam formats including GDS II STREAM.	GDSII Stream and CIF.
Description	Software for ERCs.	The Fast Mask Engine is a hardware accelerator developed specifically for physical design verification. The FME also accelerates fracturing and formatting for mask machines and is also capable of supporting raster plotting. Speed: 10X software running on VAX 11/780. Joint project between Calma and Silicon Solutions Inc.	The IC layout verification tools are activated through GeoSet, the polygon editor. The tools include design rule checking, circuit extraction, computation of circuit parameters and comparison of the layout vs. the schematic. Error reporting features for the DRC utility include automatic panning to the next error and on-screen reports describing the violated design rule, the error, and the correct rule. In this manner, design rule violations can be fixed rapidly and interactively without resorting to hardcopy plots and batch programs. The circuit extraction utility performs connectivity and electrical parameter extraction. Geometric data is analyzed to create connectivity data consisting of transistors, ports, and nets that are defined in terms of the geometric features forming them. In addition, the utility computes transistor width and length and net capacitances. The comparison utility checks for matching transistor types and connections and flags violations graphically on the GeoSet view for fast location and correction of errors. The comparison also provides alphanumeric output. Errors are categorized into levels of severity ranging from perfectly matched devices to those which are incorreectly connected.



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****IC Layout Verification Tools (Cont'd)**

Daisy Systems MAX Interactive Rules Checker	ECAD DRACULA II	ECAD DRACULA III	ES2/US2 SOLO 1000/SOLO 1200
IBM PC/XT/AT, Daisy LOGICIAN 386/Personal LOGICIAN 386	APOLLO, DATA GENERAL, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, NEC PC, RIDGE, SUN, Alliant, MIPS	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, IBM MAINFRAME/MINI, SUN	VAXstation 2000
X		X	X
X X	X	X	X
X X	X	X	
X	X	X	
	X	X	
	X	X	X
X	X	X	
Versatec plotter, CIF, GDSII, Applicon.	PG/E Beam plotting, Error data: GDSII, Applicon (APPLE) & CIF. Mask making: Mann 3000, 3600, Perkin Elmer, Electromask.	PG/E Beam plotting, Error Data: GDSII, Applicon (APPLE) & CIF. Mask Making: Mann 3000, 3600, Perkin Elmer, Electromask.	
<p>Daisy's Interactive Rules Checker (IRC) enables CHIPMASTER users to perform fast "on-call" rules checking. By having IRC on line the user can create a cell of layout, check it, fix local errors and continue working. This feature eliminates the propagation of errors common to batch verification.</p> <p>A Locator function is part of the IRC program. The Locator quickly locates layout errors by panning, zooming, and pointing. It then shows the rule, allowing users to know the type of error.</p>	<p>DRACULA II is a complete set of integrated software programs for integrated circuit layout verification and post processing. DRACULA II incorporates the latest developments in verification algorithms. This approach results in unmatched speed and accuracy while making the most efficient use of available mass storage. DRACULA II is technology independent and can be used in MOS, bipolar as well as GaAs technologies. DRACULA II accepts data in several different formats including GD-SII, Applicon, and CIF. DRACULA II is available on a variety of mainframe computers or workstations, either directly from ECAD or through several of ECAD's OEMs.</p> <p>DRACULA II's Design Rule Checker (DRC) module performs the most complex spacing checks through its conjunctive rule capability. DRC also offers generalized resizing capability to accommodate modified design rules for changing process technologies. The Electrical Rules Checker (ERC) can be used to perform process independent checks such as opens and shorts and process dependent checks such as improper implants, substrate bias, etc. The Layout vs. Schematic (LVS) and Layout vs. Layout (LVL) modules are provided for checking layout consistency. The Layout Parameter Extraction (LPE) modules allow the user to accurately extract parasitic information such as capacitance delays, etc. based on the actual layout.</p>	<p>DRACULA III is a state-of-the-art IC layout verification system. Its algorithms take advantage of the layout hierarchy to significantly increase performance over conventional methods. DRACULA III's hierarchical verification capability is ideally suited for large chips and for newer methodologies such as gate arrays, standard cells and structured custom designs. DRACULA III is up to 10X faster than competing products. This results in much shorter verification cycles and significant savings in expensive computer time. DRACULA III offers concise error reporting. Errors for cells are reported only once, thus eliminating redundant errors. DRACULA III makes very efficient use of available mass storage, minimizing disk overflow problems on large chips. DRACULA III's interactive preprocessor's simple yet powerful command structure keeps learning time down to a minimum. It is totally compatible with DRACULA II thus there is minimal relearning for existing DRACULA users. DRACULA III is a complete IC layout verification package. It performs geometrical, electrical and connectivity checks. It allows layout verification in three different modes: hierarchical mode, conventional flat mode, and cell mode for verifying individual cells.</p>	<p>The SOLO circuit layout system produces a full, all-layer layout of an optimized array. The functional elements are constructed with exactly the number of transistor pairs needed to implement the circuit. Each wiring channel is made just wide enough to accommodate the number of wires used in that particular channel. This produces layouts that are always correct by design.</p>

# IC MASTER

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
IC Layout Verification Tools (Cont'd)			
Source	EXAR	Ferranti Interdesign	Gould Semiconductor Division
Tool Name	DRACULA I (see ECAD, Inc.)	Silicon Design Sys. ULA CHECK	SCEPTRE II
FOR DETAILED DATA SEE:	page 4222		page 4244
Tool residence	DEC VAX	DEC VAX, DEC MICROVAX	IBM PC/XT/AT, NEC PC, VICTOR
Hierarchical methodology	X	X	
Design rule checking			
Batch mode	X	X	X
On-line (Interactive)		X	
Electrical rule checking			
Batch mode	X	X	X
On-line (Interactive)		X	
Layout debugging	X	X	X
Layout vs. schematic checking	X	X	X
Layout parasitic extraction	X	X	X
Layout vs. layout checking	X		
Output format	STREAM	Error listings and circuit verification.	
Description	DRACULA I is a general purpose layout verification suite of programs for design rules checking, electrical rules checking, layout vs. schematic checking, layout parameter extraction, and layout vs. layout. It is an integral part of the EXAR design automation system.		Supports complete cell-based ASIC design, from schematic capture through physical layout and verification.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

IC Layout Verification Tools (Cont'd)

Harris Semiconductor Harris/SDA Workstation page 4246	Matra Design Systems CHECK/EVAL	Mentor Graphics REMEDI	National Semiconductor Design Automation System page 4294
APOLLO, DEC MICROVAX, MASSCOMP, SUN	DEC VAX, IBM PC/XT/AT	APOLLO	IBM MAINFRAME/MINI
X			
X X	X		X
X X	X		X
X	X		
X	X		X
X	X		X
X			X
Physical and electrical design rule violations are output graphically in SDA's database format.	Standard ASCII disk files.		GDSII file and text file.
Harris supports layout verification through the use of the SDA tools PDcheck, PDextract and PDcompare. All tools are completely integrated with the SDA Framework to allow rapid design flow between tools. PDcheck, coupled with Harris' design rule packages give flat or hierarchical physical design rule checks either on-line or in batch mode. An incremental checking procedure and integrated graphical display of errors allow quick feedback to the designer after layout. PDextract is provided for extraction of complete device (real and parasitic) and connectivity information for use in ERCs and layout to schematic comparison. PDcompare allows layout to schematic, schematic to schematic, or layout to layout comparison of both network topology and electrical parameters extracted from the layout. PDcompare is fully integrated with the SDA graphics editor allowing graphical output of mismatches and cross probing between compared representations.	Eval will generate SPICE descriptions of nets running SPICE simulations.	REMEDI (Responsive Mentor Debugging Interface) is an automatic and interactive schematic-to-layout debugging module which operates in conjunction with the Mentor Graphics CHIPGRAPH custom VLSI layout editor and DRACULA II layout verification package. This combination represents a unique weaving of VLSI design tools and will substantially reduce the time required to debug IC layouts.  REMEDI integrates schematic connectivity information with the physical layout of a custom VLSI circuit and graphically displays the results in windows containing schematic and layout representations. REMEDI allows the user to graphically interpret errors associated with the layout-to-schematic comparison, a significant design productivity advance compared to present methods which compel the designer to manually correlate schematic and layout images.	For the design of National Semiconductor gate arrays and standard cells. National uses DRACULA from ECAD for chip-level layout verification.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
IC Layout Verification Tools (Cont'd)			
Source	NCR Microelectronics	SDA Systems	SDA Systems
Tool Name	VILAY Series	ERC	PDCHECK
FOR DETAILED DATA SEE:			
Tool residence	Popular workstations	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC MICROVAX, MASSCOMP, SUN
Hierarchical methodology		X	X
Design rule checking			
Batch mode			X
On-line (Interactive)			X
Electrical rule checking			
Batch mode		X	
On-line (Interactive)		X	
Layout debugging		X	X
Layout vs. schematic checking	X		
Layout parasitic extraction	X		
Layout vs. layout checking			
Output format			Fully integrated with LAYOUT graphics editor for easy error correction.
Description	For design of NCR Microelectronics' cell-based designs. Layout support and analysis CAD software. NCR developed its own layout checking and interconnect extraction tools for use with industry-leading standard cell layout programs. VILAY includes block-level netlist extraction (vs. transistor-level) and RC-tree interconnect delay extraction. These proprietary software tools and all necessary utilities, models and technology files are available for supported cell-based layout systems so that the user has control over the layout and post-layout analysis process. INTERCONNECT ANALYSIS extracts a block (cell)-level netlist, interconnect capacitance and distributed RC-tree files from the completed layout and reports certain types of errors. These include unconnected inputs, outputs shorted together, undriven nodes, unused interconnect and open power nets. X-Y coordinates, occurrence numbers and pin numbers are listed for errors. The interconnect capacitance and RC-tree files are fed to NODE DELAY for post-layout timing analysis. NETCOMPARE compares the pre-layout and extracted netlist and reposts mismatches.	SDA's Electrical Rule Checker (ERC) is a flexible tool that allows IC designers to run electrical connectivity checks on a network. These connectivity checks are applicable to both physical and logic representations. ERC is a technology independent program, allowing complete flexibility when checking today's complex circuits. By using ERC, IC designers are able to elicit highly accurate information from the circuit network and insure that correct electrical rules have been maintained.  ERC also provides for the reduction of a transistor level circuit to gate level circuit, including series and parallel processing. Some uses of this feature include: input to a logic simulator, calculation of beta ratios, driven node extraction for loading and timing.	SDA's Physical Design Rule Checker (PDCHECK) is a powerful VLSI full custom and cell-based layout verification tool. Its unique capabilities and features make it one of the most technologically advanced integrated circuit design rule checking programs. PDCHECK is ideal for checking the popular layout methodologies currently in use, as well as those being considered for the future. Whether using full custom, structured custom, standard cell, macro cell or compiler techniques, PDCHECK is a tool that ensures the early detection of all angle layout errors from even the most complex technologies. This greatly increases the probability that designs will work the first time.(P>) Additionally, productivity is increased by PDCHECK's fully hierarchical operation, on-line availability, incremental checking procedure, and unique pattern recognition capability that minimizes run times. Tightly coupled with SDA's design, simulation, and other physical design verification products, PDCHECK is part of a complete IC design system. PDCHECK provides a powerful, yet easy-to-use tool for IC layout design rule checking.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

IC Layout Verification Tools (Cont'd)

SDA Systems PDCOMPARE	SDA Systems PDEXTRACT	Silicon Compiler Systems Generator Development Tools	Silicon Solutions/Zycad Fast Mask Engine
APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC MICROVAX, MASSCOMP, SUN	APOLLO, DEC MICROVAX, SUN	APOLLO, DEC VAX, DEC MICROVAX, SUN, Silicon Solutions Fast Mask Engine
	X	X	X
		X X	X
		X X	X
X	X		
X		X	X
	X	X	X
X		X	X
Fully integrated with LAYOUT graphics editor for cross reference probing.	Extracted file provides suitable input for timing analysis, transistor-level simulation, or SDA's PDCOMPARE program.	GDSII, EDIF.	All major PG formats including GDSII STREAM.
<p>SDA's Physical Design Circuit Comparator (PDCOMPARE) is a flexible tool that provides a fast and accurate means for checking a physical layout against a schematic for discrepancies. In addition to checking circuit networks, PDCOMPARE can compare electrical parameters extracted from the layout with those specified by the designer in the schematic. PDCOMPARE may also be used for other practical purposes such as layout-to-layout and schematic-to-schematic comparisons.</p> <p>Using advanced features such as full device permutability, no correspondence points, fully integrated graphics feedback, on-line availability, and fast checking algorithms, SDA's PDCOMPARE provides the designer with a state-of-the-art method for verifying the integrity of a chip layout.</p>	<p>SDA's Physical Design Extractor (PDEXTRACT) is a highly versatile fully integrated tool that allows IC designers to extract complete device and connectivity information from any integrated circuit layout. Independent of technology and methodology, all "real device" parameters and most parasitic devices encountered in the layout are also extracted. The output of PDEXTRACT is a new representation called "extracted", which is a flattened network of the entire circuit. This new database description is at the transistor level with the elements of the circuit being schematic devices, parasitic devices, and all derived parameters.</p> <p>By using PDEXTRACT, IC chip developers are able to elicit highly accurate information from the layout and run a subsequent simulation to determine the layout's exact performance. This produces extremely accurate and optimally designed integrated circuits further resulting in reduced design times and minimized design costs.</p>	<p>The Generator Development Tools (GDT) can be used by IC designers to create their own silicon compilers. The power of the GDT is based on a new language, L, developed by SDL. Generators, produced using L, can accept parameters from a user and develop completely custom layouts. GDT can also be used by logic designers and system designers to create larger functional blocks or complete chips using their own or Silicon Design labs' basic functions. GDT features a Macintosh-like user interface, on-line design rule checking and an integrated hierarchical mixed-mode functional/circuit/fault simulator. GDT also includes a complete standard cell library and automatic place and route tools as well as PLA generation tools.</p>	<p>Also accelerates fracturing and formatting for mask machines. Speed: 10X software running on VAX 11/780. Hardware accelerator for performing DRCs.</p>

# IC MASTER

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
IC Layout Verification Tools (Cont'd)			
Source	Silvar-Lisco	Silvar-Lisco	Standard Microsystems Corp.
Tool Name	DVS	Parallel DVS	STANCOMP
FOR DETAILED DATA SEE:			page 4310
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, SUN	ELXSI	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, Mentor, Daisy, Valid
Hierarchical methodology	X	X	X
Design rule checking Batch mode On-line (Interactive)	X	X	X X
Electrical rule checking Batch mode On-line (Interactive)	X	X	X X
Layout debugging	X	X	X
Layout vs. schematic checking	X	X	X
Layout parasitic extraction	X	X	X
Layout vs. layout checking	X	X	
Output format	See Description.	GDS I & II, Applicon 860/870, Calplot/Calplot C, CIF, Computervision CADD5 2, Electromask 2000, Mann 3000/3600, ALF, etc.	
Description	Includes: mask data preparation, circuit extraction, SPICE network generator, and schematic vs. schematic checking. Interfaces supported: GDS I & II, Applicon 860/870, Calplot/Calplot C, CIF, Computervision CADD5 2, Electromask 2000, Mann 3000/3600, ALF/Cambridge/ETEC (all), Varian, EE-BES.	Silvar Lisco's Design Verification System (DVS) is available in a parallel version on ELXSI's System 6400. Parallel DVS uses up to 12 CPUs concurrently to speed up a single IC design verification. The number of CPUs to be used is specified at run time. Parallel DVS performance depends on both the size and nature of the circuit being processed. For example, an ELXSI DYAD (2-CPU) configuration has shown throughput improvements, measured by total elapsed time, from 1.4x to 1.7x compared to a 1-CPU configuration.	Layout verification software for use with SMC cell-based designs. Provides the chip layout and design rule checking functions. Further, it provides the capability of checking the netlist extracted from the layout with the logical netlist to assure the correctness of the layout data.



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****IC Layout Verification Tools (Cont'd)**

Tektronix CAE Systems DRACULA II (see ECAD Inc.) page 4658	Valid Logic Systems Inc. ValidCOMPARE/ERC page 4660	Valid Logic Systems Inc. ValidDRC/EXTRACT page 4660	VLSI Technology VTIverify page 4665
DEC VAX, DEC MICROVAX	DEC MICROVAX, SUN, Valid SCALDsystem	DEC MICROVAX, SUN, Valid SCALDsystem	APOLLO, DEC VAX, DEC MICROVAX, ELXSI, HEWLETT-PACKARD, RIDGE, SUN
	X	X	X
X		X X	X X
X	X X		X X
X	X	X	X
X	X		X
X		X	X
X		X	X
Outputs to most common available optical and E-beam pattern generators.	GDS II, CIF, EDIF	GDS II, CIF, EDIF	Graphic display, ASCII file in CIF format.
<p>DRACULA is a full set of integrated software to help the designer verify his IC mask layout.</p> <p>DRACULA offers a Design Rule Checker, an Electrical rule Checker, an LVS tool that guarantees total design logic before the first silicon implementation, Layout Parameter extraction, LVL tool that compares two different layout databases and outputs the geometric, logical and parametric differences. DRACULA also has a mask fracturing feature that permits fracturing of most modern mask geometries with accuracy, efficiency and ease.</p>	<p>Compares the logical electrical circuit with the layout circuit. This ensures that all electrical functions on the schematic are present on the layout. It also provides for back annotation of the schematic.</p> <p>Performs electrical rule checks on the extracted IC layout netlist. Electrical rules are used to ensure the electrical circuit functions correctly. These include paths to power and ground, and minimum transistor size.</p>	<p>ValidDRC/EXTRACT performs design rule checks on and between IC mask layers. Design rules include a safety margin for mask misalignment and other process variations in manufacturing. These include minimum line width; minimum line spaces, etc.</p> <p>Extracts from transistor, capacitor, and resistance information from the IC layout (including transistor W or L ratio). This file can then be formatted into an arbitrary netlist description, such as a SPICE deck.</p>	<p>VTIverify provides the user with a netlist extractor, a netlist comparator, a design rule checker, and an electrical rule checker. These tools verify that the netlist and physical layout produced by the tools are correct and consistent.</p>

## IC MASTER

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Hardware Tools—Physical Modelers			
Source	Appicon	Cadnetix	Calma
Tool Name	Dynamic Hardware Modeler	CDX-7950 Physical Modeling Pkg	Physical Modeler System
FOR DETAILED DATA SEE:			
Tool residence	Stand alone, works on a TCP/IP network	CDX-70000 Configurable Analysis Engine	APOLLO
Physical model packaging			
SIP & DIP	X	X	X
Leadless chip carrier	X	X	X
Pin grid array	X	X	X
Surface mount device			X
PC board			X
Device pin assignment			
Hard-wired fixtures	X	X	X
Software pin assignment	X	X	
Network modeler accessibility			
Directly to workstations	X	X	X
Via host only			
Logic simulation states			
High-z sensing	X	X	X
User-selectable drive strength	X	X	
Unknown state handling	X	X	X
Fault simulation	X		
Memory depth			
Fixed memory allocated per pin	X		X
Variable assignment		X	X
Test vectors per pin (max.)	512K expandable to 2M	512K	512K
Clock rate (max. MHZ)	8 MHz data rate	16 MHz	10 MHz
Capacity			
ICs per carrier	1	6	1
IC carriers per mainframe (max.)	30	5 (30 total ICs per box)	30
VLSI Parts supported	2901, 29501, 6801, 6809, 68000, 68020, 68452, 68681, 68901, 8035, 8039, 8040, 8086, 8088, 8237, 8253, 8254, 8251A, 8259A, 8288, 8748, 8749, 80287, and others.	Motorola 6800/68000 family & peripherals; Intel 80XX/80X86 family & peripherals; AMD bit-slice Family; Zilog Z80/Z8000 family & peripherals; and others.	AMD bit-slice, Motorola 6800/68000 families & peripherals, Intel 8088/80287 families & peripherals, Zilog Z80, TI 32010 DSP, many others.
Description	The Dynamic Hardware Modeler may be used in conjunction with the Logic Analysis package to model complex components in an overall circuit simulation. The Dynamic Hardware Modeler is a shared network resource, and allows numerous cartridges to be plugged in which contain the actual component being modeled.	The CDX-7950 Physical Modeling Package provides physical modeling capability for complex VLSI components with up to 364 inputs and 384 outputs. Maximum storage is 512 K vectors at 96 bits wide each. Maximum clock rate is 16 MHz.  The Physical Modeling Package is an option to the Cadnetix Configurable Analysis Engine and includes the Cadnetix Digital Design Environment simulation software.	The Calma logic simulation system provides a suite of capabilities to answer the needs of the system designer. This ranges from the switch/gate level simulation based on software models built up from intrinsic primitives to behaviorally-described modules using the expressive power of the TEXSIM/B language. The Calma Hardware Modeler extends the TEXSIM/B behavioral capability by adding an interface to hardware models.  The Calma Hardware Modeler System consists of a hardware engine interfaced to a Calma Logic Explorer workstation via Ethernet. This engine acts as a server that can support multiple users running TEXSIM/B simulations over the DOMAIN network ring. The particular hardware devices to be used in simulations are configured onto VME printed wiring boards called cartridges and inserted in the hardware engine. The Calma Hardware Modeler will allow the design engineer to simulate complex VLSI devices quickly and accurately using the actual device.

Bold face indicates data is provided in the page noted



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Hardware Tools—Physical Modelers (Cont'd)

Case Technology DHM (see HHB Systems)	Daisy Systems Physical Modeling Extension	FutureNet (Data I/O) DASH-CATS page 4651	Genrad HICHIP
	IBM PC/XT/AT, LOGICIAN/Personal LOGICIAN/MegaLOGICIAN		APOLLO, DEC VAX, DEC MICROVAX, HEW. LETT-PACKARD, IBM MAINFRAME/MINI, RIDGE, SUN, Intergraph
X	X X X X		X X X X
X	X X		X
X	X		X
X X X X	X X X X		X
512K	128k		X 256k
8	25 MHz with PMX FastBoard		16
30	154 channels (static) 96 ch. dynamic 5		1 16
Motorola, Intel, Zilog	Daisy's Physical Modeling Extension supports all microprocessors from the following: Intel, Motorola, Zilog, National, AMD, TI, Weitek.	FutureNet has signed an agreement with HHB Systems that will allow FutureNet to offer the HHB Cats Hardware family of CAE tools. CATS provides full CADAT simulation capabilities plus combined hardware and software modeling. CATS allows hardware models to be included in the same circuit along with switch, gate, behavioral, and CATS Accelerator software models. As part of the package, the CATS Accelerator addresses the simulation time problem and turns large simulations into part of an interactive design process.	The HICHIP Universal Hardware Modelling System enables efficient use of logic simulation when using complex VLSI components. Previously, models of these devices were difficult or impossible to create using some simulation techniques. HICHIP adds the concept of hardware modelling to the powerful HILO functional modelling language to provide a modelling choice for the user.
Can simulate LSI and VLSI chips and incorporate the results into overall simulation of a design. Features include: plug-in cartridges for hardware modeling, interactive user control through a software shell, supports full CADAT capabilities plus combined hardware and software modeling. Functions as a shared system resource. Holds up to 30 cartridges.	Tightly coupled to simulation engine. Direct support of static components. Interchangeable device carriers. Open architecture. Sharing of signal channels.	The CATS Fault Accelerator, offering very fast fault simulation performance, is an option that can be configured for fault simulation by simply adding a fault acceleration module. Designers can incorporate physical LSI and VLSI chips into a design by using convenient plug-in cartridges. Hardware models are fast and inexpensive to create and can save considerable software programming time. The devices are simulated as an integral part of the system design along with software SSI/MSI models assembled by the designer from the CATS/CADAT model library.	System characteristics: 16 MHz data application rate; adjustable strobe resolution; dynamically adjustable memory of up to 256K words of 128 bits; up to 128 input/output pins per device; TTL compatible +5, +12 and -12 volt supplies; RS-232 or multi user Ethernet communication; and State Sensitive software shell.

## DESIGN AUTOMATION—Design Tools

## Generic Function

## Design Tool Capability

## Hardware Tools—Physical Modelers (Cont'd)

Source	Harris Semiconductor	Hewlett-Packard	HHB Systems
Tool Name	CATS (see HHB Systems)	HICHIP (see Genrad)	CATS Modeler
FOR DETAILED DATA SEE:	page 4246		
Tool residence	CATS SHM- Based on Sun 3	HEWLETT-PACKARD	APOLLO, DEC VAX, DEC MICROVAX, MAS-SCOMP, SUN
Physical model packaging			
SIP & DIP	X	X	X
Leadless chip carrier	X	X	X
Pin grid array	X	X	X
Surface mount device	X		X
PC board	X		X
Device pin assignment			
Hard-wired fixtures	X	X	X
Software pin assignment	X	X	X
Network modeler accessibility			
Directly to workstations	X	X	X
Via host only	X		
Logic simulation states			
High-z sensing	X		X
User-selectable drive strength	X		X
Unknown state handling	X	X	X
Fault simulation	X		X
Memory depth			
Fixed memory allocated per pin			
Variable assignment	X	X	X
Test vectors per pin (max.)	512Kk	256k vectors per pin	512K
Clock rate (max. MHZ)	12	16 MHz	10
Capacity			
ICs per carrier	1	1	1
IC carriers per mainframe (max.)	30	16	30
VLSI Parts supported	All digital VLSI parts.	Expanding list	Over 100 parts available, and kits for custom VLSI parts.
Description	Using the CATS Dynamic Hardware Modeler, designers are able to incorporate physical LSI and VLSI chips into a design by means of plug-in DHM cartridges. The actual devices are then simulated as an integral part of the system design along with the software SSI/MSI models assembled by the designer from the CADAT model library. The entire "virtual breadboard" design is then simulated using HHB Systems' CADAT under the control of the CATS shell software.	Hewlett-Packard's HICHIP Hardware Modeling System provides an efficient method for modeling complex LSI/VLSI devices within the H-P Electronic Design System. HICHIP simplifies board-level simulation by integrating hardware models, using the actual device, into logic simulation.	The CATS (Computer Aided Test System) Modeler interfaces HHB Systems' CADAT 6.0 logic, timing and fault simulator with physical LSI and VLSI devices to provide an efficient and cost effective method of exercising and debugging board level designs. The CATS Modeler is marketed as an end user and OEM product.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Hardware Tools—Physical Modelers (Cont'd)

Mentor Graphics Hardware Modeling Library	Racal-Redac VISULA CATS	Simulog SuperSim	Tektronix CAE Systems HICHIP (see Genrad)  page 4658
APOLLO	APOLLO, DEC MICROVAX, IBM PC/XT/AT, SUN, (Resides on SUN; accessible by others)	DEC MICROVAX	APOLLO, DEC VAX, DEC MICROVAX
X X X  X	X X X X	    X	X X X
X	X X	X X	X
X	X	X X	X
X X X X	X  X	X X	X X
X	X	X	
X 64K	X  512K/pin (512,000 states/pin)	X  Up to 256K bit	X  256K
16 MHz	10 MHz (vector rate)	20 MHz	16 MHz
4 64-pin DIP packages 8	30 devices at one time		Up to 128 IC pins per card max Up to 8 128 pin cards per system
PARTIAL LIST: Microprocessors: Motorola 68000, 68010, 68020, Intel 8031, 8051, 80186, 80C86, Zilog Z80, AMD bit slice 2901, 2910, Support VLSI: Motorola 68230, 68451, 68452, Intel 8254, 8253, 8288, 8289, 82284, AMD 2940.		Any device through 256 pin connections.	
<p>The Mentor Graphics Hardware Modeling Library (HML) System eliminates the process of writing software models for complex components by allowing designers to use actual components as models in simulations. The hardware models are accurate and full functional models; they allow for complete design verification using software simulation. Furthermore, micro-code can be run in the simulations allowing for firmware and system debugging before any hardware is assembled. HML is designed to be a transparent, network sharable resource capable of supporting multiple users concurrently. HML can simultaneously provide any number of instances of a hardware element to all network users.</p> <p>Timing information for HML simulations can come from two sources: software timing files, or the optional timing analyzer. The timing analyzer gives HML precise timing measurement capability by measuring time parameters directly from the components I/O pins, sampling up to 256 pins at 100 MHz.</p>	<p>CATS is said to be the only fully integrated hardware &amp; software system in the CAE/CAD/CAT world. CATS leaps the void between design and test by joining in a single standalone system: design simulation, fault simulation, hardware modeling and prototype verification capabilities. There are three major elements: 1) CADAT, HHB Systems' logic and concurrent fault simulator; which is made faster with the addition of a hardware accelerator. 2) A hardware evaluator which simplifies the modeling process of complex IC's and PCB's by using the actual device as a simulation model and providing the intelligent handling of initialization and race conditions. The hardware evaluator works with CADAT's fault simulation capability for efficient grading of PCB test programs. 3) A dynamic chipchecker and board-checker which makes prototype testing of ICs and PCBs simpler and quicker. Both functions test physical prototypes at rates up to 8 MHz against data automatically extracted from CADAT simulations.</p> <p>Design engineers can verify prototype devices and no longer need access to production Automatic Test Equipment.</p>	<p>Simulog, Inc. has a family of six standard machines with simulation speeds of 10 Giga to 200 Giga gate evaluations per second and gate capacity of 32K to 1M, respectively. Models of up to 8M gates are available. SuperSim is a fully interactive machine: Breakpoints specifying complex conditions may be used to interrupt a simulation, then any network node may be checked and its logic level changed if desired.</p> <p>A designer may interactively build additional circuitry and wire it into the already existing simulated design. He may rewire (connect and disconnect) portions of the network and continue simulating the altered network without having to recompile. SuperSim may be operated as a stand-alone system or a network server, and it has a multi-user option (up to 8 concurrent users).</p>	<p>HICHIP Hardware Modelers enables efficient use of logic simulation when using complex VLSI components. HICHIP modeler allows simulation of devices for which there are no software models yet written. The need to write lengthy software models for describing complex chips is reduced, thus saving engineering time and effort. The modeler also eliminates the chance of errors in software modeling by using the functions of the actual part, guaranteeing accuracy of simulation early in the design.</p>



## DESIGN AUTOMATION—Design Tools

## Generic Function

## Design Tool Capability

## Hardware Tools—Physical Modelers (Cont'd)

Source	Teradyne	Valid Logic Systems Inc.	Valid Logic Systems Inc.
Tool Name	DATASource	Networked Realchip	Realchip
FOR DETAILED DATA SEE:		page 4660	page 4660
Tool residence	DEC VAX, DEC MICROVAX, Teradyne DATAServer simulation engine	DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN, Valid Proprietary	Valid Proprietary
Physical model packaging			
SIP & DIP	X	X	X
Leadless chip carrier	X	X	X
Pin grid array	X	X	X
Surface mount device	X	X	X
PC board	X	X	X
Device pin assignment			
Hard-wired fixtures			
Software pin assignment	X	X	X
Network modeler accessibility			
Directly to workstations		X	X
Via host only	X		
Logic simulation states			
High-z sensing	X	X	X
User-selectable drive strength		X	X
Unknown state handling	X	X	X
Fault simulation	X	X	X
Memory depth			
Fixed memory allocated per pin			
Variable assignment	X	X	X
Test vectors per pin (max.)	256,000	16k	16K
Clock rate (max. MHZ)	16.7 MHZ	5 MHZ	4 MHZ
Capacity			
ICs per carrier	Pins assigned in groups of 4	8	2
IC carriers per mainframe (max.)	60	32	18
VLSI Parts supported	Static and dynamic TTL, ECL, and CMOS parts (including gate arrays), and mixed-logic devices.	AMD, AT&T, Digital Equipment, Fairchild, Ferranti, Harris, Intel, Motorola, National, NEC, Signetics, Texas Instruments, Western Digital, Wietek, Zilog	AMD, AT&T, Digital Equipment, Fairchild, Ferranti, Harris, Intel, Motorola, National, NEC, Signetics, Texas Instruments, Western Digital, Wietek, Zilog
Description	<p>DATASource is a VLSI hardware modeling system which permits the use of physical models in board and system level simulations using the LASAR Version 6 simulation system. DATASource is capable of serving multiple users, and is claimed to be the first modeling system to support high-speed, concurrent fault simulation as well as logic simulation operations.</p> <p>The DATASource hardware modeling system provides a maximum of 2,400 pins, which can be configured flexibly to accommodate multiple devices, and devices of any size up to 2,400 pins. The system handles static and dynamic TTL, ECL and CMOS parts (including gate arrays), and mixed-logic devices, and can drive up to 160 device inputs simultaneously at the maximum pattern rate of 16.7 MHZ.</p>	<p>Networked Realchip is a member of Valid's Realproducts family of application-specific hardware. Based on Valid's Realchip hardware modeling technology, Networked Realchip provides designers with concurrent, multi-user access to models of VLSI devices. The models are available to all users who are connected to the Ethernet network (TCP/IP protocol). The basic Networked Realchip can accommodate two state-of-the-art VLSI devices such as the Motorola 68020, Intel 80386, or Digital's VAXBI device. It can be expanded to handle up to 64 VLSI devices.</p>	<p>Realchip is a hardware modeling system that uses real chips to model themselves when simulating designs containing complex VLSI devices such as microprocessors, complex peripheral chips, custom chips, gate arrays, and similar devices. Realchip makes its hardware model library of complex devices available to the ValidSIM logic simulator for the simulation of complex designs. Valid was granted a patent on the fundamental hardware modeling technology used in Realchip in May, 1986.</p> <p>Realchip can be used as a model development station or when a user requires a unit dedicated to his workstation. An example is checking finished ASIC devices for correct functional operation. As a design team resource, another version called Networked Realchip is available. It is designed to communicate with all platforms on the network by using industry standard Ethernet and TCP/IP communication protocols with an integral network server. Concurrent multi-user operation is available, facilitating maximum productivity for all members of the design team with minimal investment.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Hardware Tools—Physical Modelers (Cont'd)

Valid Logic Systems Inc. Realmodel page 4660			
Valid Proprietary			
X X X X X			
X			
X			
X X X			
X			
X 256K			
16 MHz			
4 18 (30 optional)			
AMD, AT&T, Digital Equipment, Fairchild, Ferranti, Harris, Intel, Motorola, National, NEC, Signetics, Texas Instruments, Western Digital, Wietek, Zilog			
<p>Realmodel is a simulation subsystem specifically designed for quick and efficient simulation of system designs that include VLSI and VHSIC devices. Realmodel combines tightly coupled simulation acceleration and hardware modeling engines into a single, high-performance system.</p> <p>Because Realmodel is integrated into the Valid Simulation Environment, accelerated simulation of designs containing models at switch, gate, functional, behavioral, and hardware levels may be performed with a single simulator having a single human interface.</p> <p>Realmodel's long simulation capability makes software-hardware integration of microprocessor-based designs possible for the first time, before the hardware is available. The design cycle can be shortened considerably by catching many hardware problems in simulation that would normally not be caught until the software was loaded and executed on actual hardware. Hardware integration can be simulated with application or operating system modules.</p>			

**DESIGN AUTOMATION—Design Tools**

Generic Function		Design Tool Capability	
Hardware Tools—Circuit Simulation Accelerators			
Source	Harris Semiconductor	Mentor Graphics	Mentor Graphics
Tool Name	PACSIM (see Simucad)	Compute Engine running MSIMON	Compute Engine running MSPICE
FOR DETAILED DATA SEE:	page 4246		
Tool residence	APOLLO, DEC VAX, MASSCOMP, SUN	APOLLO, Mentor proprietary	APOLLO, Mentor proprietary
Guaranteed convergence		X	
Network sharable	X	X	X
User interface			
Batch mode	X	X	X
On-line (Interactive)		X	X
Capacity field upgradable	X	X	X
Algorithm accelerated		MSIMON	MSPice
Capacity (transistors max.)	3,000-4,000	5,000 transistors w/20 MB Compute Engine	5,000 transistors w/20 MB Compute Engine
Speed (MFLOPS)	20 MFLOPS	8	8
Precision (bits)	64 bits	64	64
Acceleration compared to reference software run on non-accelerated hardware	The accelerator is approximately 2X as fast as the non-accelerated version in the transient loop and 3X faster in system CPU time.	10X over MSIMON on an Apollo DN660. Note that MSIMON on the DN660 is approx. 20X MSPICE on the DN660.	5-10X MSPICE on an Apollo DN660.
Other functions accelerated		The Compute Engine Global Accelerator addresses the entire range of compute intensive CAE applications, including simulation, layout, and design rule checking.	The Compute Engine Global Accelerator addresses the entire range of compute intensive CAE applications, including simulation, layout and design rule checking.
Description	PACSIM is a fast and accurate simulation program that performs nonlinear DC, nonlinear transient and linear AC analyses. PACSIM is compatible with the input formats, output formats, and models of Berkeley's SPICE2G.	The Compute Engine global accelerator accelerates all compute intensive applications including user-written applications. MSIMON is a circuit simulator that is optimized for digital MOS analysis.	The Compute Engine global accelerator accelerates all compute intensive applications, including user-written applications. MSPICE is Berkely 2G.6 SPICE with a powerful front and back end developed by Mentor Graphics Corp.



DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Hardware Tools—Logic Simulation Accelerators			
Source	Aida	Aida	Cadnetix
Tool Name	Aida CoSimulator Processor	Aida PerSimulator Processor	CDX-770 Accel. Digital Design
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, SUN	APOLLO	CDX-70000 Configureable Analysis Engine
Hierarchical simulation			
Switch level			X
Gate level	X	X	X
Functional level			X
Behavioral level			
Physical model level			X
Network sharable	X	X	X
Field upgradable	X		X
User interface			
Batch mode	X	X	X
On-line (Interactive)	X	X	
Algorithm accelerated	Levelized compiled code	Levelized Compiled Code	
Speed (events per second)	5 million	5 million	200,000
Simulation size			
Type of primitive modeled	Gate	Gate	Functional
Number of primitives modeled	1 million gates	128,000 gates	1,000,000 equivalent gates
Number of states	4		21
Acceleration compared to reference software run on non-accelerated hardware	Accelerated Levelized Compiled Code is 100 times faster than LCC algorithm executing in software.	Accelerated Levelized Compiled Code is 100 times faster than LCC algorithm executing software.	200 times performance of MC68020-based Configureable Analysis Engine.
Other functions accelerated	Aida Fault Simulation, Fault Inferencer and Aida Automatic Test Pattern Generation.	Aida Fault Simulation, Fault Inferencer, and Aida Automatic Test Pattern Generation.	Physical modeling simulation.
Description	The Aida CoSimulator Processor is a proprietary hardware accelerator. Installed in an Apollo or Sun workstation, it speeds up the execution of the Aida Logic Simulators, Fault Simulators, Fault Inferencer and ATPG. With the CoSimulator Processor, it is possible to verify designs of up to 1 million gates at speeds of 5 million gate evaluations per second.	The Aida PerSimulator Processor is a proprietary hardware accelerator. Installed in an Apollo DN3000 or DN4000 workstation, it speeds up the execution of the Aida Logic Simulators, Fault Simulators, Fault Inferencer, and ATPG. With the PerSimulator Processor, it is possible to verify designs of up to 128,000 gates at speeds of 5 million gate evaluations per second.	The CDX-770 Accelerated Digital Design Environment is a network simulation resource for accelerated analysis. Based on the MC68020 processor, the CDX-770 runs at a rate of 200,000 events per second and has a maximum capacity of 1,000,000 equivalent gates. The CDX-770 includes the Cadnetix Digital Design Environment software and is an option to the CDX-70000 Configureable Analysis Engine.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Hardware Tools—Logic Simulation Accelerators (Cont'd)			
Source Tool Name FOR DETAILED DATA SEE:	Case Technology CATS Accelerator	Daisy Systems MegaLOGICIAN	Gateway Design Automation VERILOG-XL
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN	Daisy proprietary hardware	APOLLO, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN, Silicon Graphics, Gould
Hierarchical simulation Switch level Gate level Functional level Behavioral level Physical model level	X X X X X	X X X X X	X X X X
Network sharable	X	X	X
Field upgradable	X	X	X
User interface Batch mode On-line (Interactive)	X	X	X
Algorithm accelerated	CADAT	Proprietary	Proprietary
Speed (events per second)	16 million	100 evaluations per second	Up to 200,000
Simulation size Type of primitive modeled Number of primitives modeled	4 input 1 output device 2.1 million	Switch through RAM, ROM and PLA 64K	Gate/switch level primitives 1,400,000 with 50 MB virtual memory
Number of states	21	12	106
Acceleration compared to reference software run on non-accelerated hardware	10000 gate design that required 10 hours on a VAX 780 was completed in 10 minutes on the accelerator.	100X Daisy Logic Simulator on Daisy LOGICIAN.	On the same general purpose computer VERILOG-XL runs approx. 20X faster than VERILOG at the gate/switch level.
Other functions accelerated	Fault simulation.	Gate array layout, fault simulation	
Description	1000 times faster than VAX 11/780. Supports all levels of simulation, expandable capacity for up to 2.1 million primitives. Stand alone or networked operation. Can be networked to any of the listed platforms. Parallel and pipeline processing. Uses 500 bit wide memory.	Daisy's MegaLOGICIAN combines the basic LOGICIAN tools with a high-speed hardware simulation engine for a quantum leap in simulation performance. Three custom-microcoded, but-slice processors, each operating in parallel, perform over 100,000 functional evaluations per second with no loss of simulation accuracy.  It is designed to accelerate logic simulation, fault simulation (MegaFAULT) and gate array layout (MegaGATEMASTER). The MegaLOGICIAN can be operated as a standalone workstation or as a network resource, interactively accessed and controlled by Daisy workstations.	VERILOG-XL is a high performance, mixed-level digital design language and interactive simulation system that integrates the capabilities of behavioral level languages, register-transfer level languages, and numerous gate-level and switch-level languages, along with the capability of dynamically interacting with user-written software programs. VERILOG-XL uses "significant event simulation" at high design levels. At lower levels, an advanced form of clock suppression, called "adaptive behavior recognition" is employed. As a result, VERILOG-XL simulation at all levels is extremely fast and efficient. At the gate/switch level it rivals the performance of hardware accelerators built just for gate/switch simulation.  VERILOG-XL provides advanced interactive symbolic debugging facilities and employs a single homogeneous language for circuit description, waveform description, and symbolic debugging. VERILOG-XL combines high-speed compilation of the design description with high-speed simulation thereby providing a truly interactive capability on computers the size of today's workstations. At the behavioral/register level, VERILOG-XL's features include sequential and/or concurrent process execution, dynamic delay expressions, named events, arithmetic/logical and bit-wise reduction operators, procedural constructs, and dynamic linkup with user programs.

Bold face indicates data is provided in the page noted



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Hardware Tools—Logic Simulation Accelerators (Cont'd)**

Harris Semiconductor CATS 9000 (see HHB Systems) page 4246	Hewlett-Packard Precision Architecture	HHB Systems CATS Accelerator	IKOS Systems IKOS 800
The CATS 9000 Sun-3 based machine	HEWLETT-PACKARD	DEC VAX, DEC MICROVAX, MASSCOMP, SUN	IBM PC/XT/AT
X X X X X	X X X X	X X X X X	X
X	X	X	X
X	X	X	X
X X	X X	X X	X
CADAT	HILO	CADAT Logic Simulation	
16 million events per second		500k per module	500,000 to 20,000,000
4-input NAND 256K	HILO primitives 18	4 input, combinational and sequential 256 user definable	4-input/1-output table driven 64,000
21	15	21	16
Speeds up to 162X faster than software on a Sun-3 have been achieved.	Same as HILO software accelerated.	500X a VAX 11/780	
Fault simulation	Logic and Fault simulations.	Fault simulation	Stimulus input and stimulus response acceleration.
The CATS 9000 accelerator is a special purpose computer designed to perform logic simulations at speeds up to 1000X faster than on a VAX 11/780. The core algorithms of the CADAT simulator are implemented on full custom VLSI chips.		The CATS Accelerator is a special purpose computer designed to perform logic and fault simulations at speeds up to 500 times faster than on a VAX 11/780. Yet, it is available at a workstation price. The CATS Accelerator's speed and low cost are derived from its unique architecture.  The core algorithms of the CADAT 6.0 logic, timing, and fault simulator are implemented in full custom VLSI chips. Additionally, the CATS Accelerator takes full advantage of pipeline and parallel processing and a 500 bit wide-memory. Up to 8 accelerator modules can be attached in parallel to allow simulations of up to 512 thousand primitives at speeds up to 4 million events per second.	

## DESIGN AUTOMATION—Design Tools

## Generic Function

## Design Tool Capability

## Hardware Tools—Logic Simulation Accelerators (Cont'd)

Source	Mentor Graphics	Silicon Solutions/Zycad	Simulog
Tool Name	Compute Engine w/QuickSim	Mach 1000	SuperSim
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, Mentor proprietary	APOLLO, DEC VAX, DEC MICROVAX, HEW-LETT-PACKARD, IBM MAINFRAME/MINI, SUN, TEKTRONIX, Silicon Solutions proprietary hardware	DEC MICROVAX
Hierarchical simulation			
Switch level	X	X	X
Gate level	X	X	X
Functional level	X	X	X
Behavioral level	X	X	X
Physical model level	X		X
Network sharable	X	X	X
Field upgradable	X	X	X
User interface			
Batch mode	X	X	X
On-line (Interactive)	X	X	X
Algorithm accelerated	QuickSim		Exhaustive simulation
Speed (events per second)	30,000 events/sec	500k to 16 Meg.	200 GIGA evaluations/sec
Simulation size			
Type of primitive modeled	Switch, gate, behavioral, QuickParts		2-input (+ 1 expand) logic gate, or D-FF
Number of primitives modeled	80K gates; 80K primitives in 20MB Engine	512,000	1 Meg standard, up to 8 Meg
Number of states	12	21	3 levels, definable strengths (4 stdrd)
Acceleration compared to reference software run on non-accelerated hardware	10X QuickSim on Apollo DN660.	1000X Cadat on VAX 11/780.	On 250K gate test circuit runs more than 750 times faster than competing accelerators and more than 100,000 times faster than software simulators.
Other functions accelerated	The Compute Engine Global Accelerator addresses the entire range of compute intensive CAE applications including simulation, layout and design rule checking.		1. Compile time for network and stimuli. 2. Load time of the above into the accelerator.
Description	The Compute Engine global accelerator accelerates all compute intensive Mentor Graphics applications, including user-written applications. QuickSim is Mentor Graphics' full-featured logic simulation accelerator. All types of software modeling techniques are accelerated including switch, circuit, gate, QuickParts and Behavioral Level Models. Hardware modeled parts are also supported.	A very flexible logic simulation accelerator. Field upgradable to Mach 1000 Logic + Fault Simulator. True timeshare system for networked users. Circuit element described at the behavioral level are simulated but not accelerated.	Simulog Inc. has a family of six standard machines with simulation speeds of 10 Giga to 200 Giga gate evaluations per second and gate capacity of 32K to 1M, respectively. Models of up to 8M gates are available. SuperSim is a fully interactive machine: Breakpoints specifying complex conditions may be used to interrupt a simulation, then any network node may be checked and its logic level changed if desired.  A designer may interactively build additional circuitry and wire it into the already existing simulated design. He may rewire (connect and disconnect) portions of the network and continue simulating the altered network without having to recompile. SuperSim may be operated as a stand-alone system or a network server, and it has a multi-user option (up to 8 concurrent users).



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Hardware Tools—Logic Simulation Accelerators (Cont'd)

Teradyne DATAServer	Valid Logic Systems Inc. Realfast page 4660	Valid Logic Systems Inc. Realmodel page 4660	XCAT HSE Hierarchical Accelerator
Customized Sequent Balance 21000	Valid Proprietary	Valid Proprietary	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/ XT/AT
X X X X X	X X X X X	X X X X X	X X X
X		X	X
X	X	X	X
X	X X	X X	X
LASAR Version 6			Event driven
Varies depending on operation	To 500K	To 500K	Up to 5 MEPS
Switch/gate/functional/behavioral	32K (1 million optional)	32K (1 million optional)	4-input 1-output Up to 8 MEPS
15 plus drive current-strength analysis	20	20	4 (1, 0, X, Z)
10-15 times faster than VAX 11/780.	Up to 500,000 events per second (equivalent to 1.25 million evaluations/second) which is 100-500 times that of workstation simulation speeds for large designs.	Up to 500,000 events per second (equivalent to 1.25 million evaluations/second) which is 100-500 times that of workstation simulation speeds for large designs.	Up to 2500 times faster than software simulators running on a VAX 11/780.
Fault simulation, model compilation, vector compilation.		Hardware Model Simulation	Timing simulation and fault switch level simulation.
<p>The DATAServer simulation server is a multi-processor system that uses parallel processing techniques to speed up LASAR Version 6 simulations. Providing 10 to 15 times the performance of a VAX 11/780 computer, DATAServer accelerates every simulation package available in LASAR: good-circuit logic simulation; worst-case timing analysis; and concurrent fault simulation. The system also supports any mix of structural, behavioral, and hardware models in simulation.</p> <p>Unlike hardware accelerators, which encode simulation algorithms on custom ICs, DATAServer runs LASAR Version 6 in software. As a result, the LASAR algorithms can be modified and upgraded easily as new simulation capabilities are developed. Moreover, while hardware accelerators are limited exclusively to simulation activities, DATAServer includes general-purpose, UNIX-based processors to run non-simulation tasks. Based on Sequent Computer Systems Inc.'s Balance 21000 parallel computer system, DATAServer augments the Balance system's general-purpose processors with hardware optimized by Teradyne for simulation operations. It also includes custom software that enables any LASAR simulation job to be executed in parallel.</p>	<p>Simulating at a maximum rate of 500,000 events per second, the Realfast Simulation Accelerator provides interactive simulation of designs containing up to a million primitives, while supporting the advanced simulation capabilities and user interface of the ValidSIM logic simulator.</p> <p>Realfast reduces the design cycle by allowing the engineer to verify a design in a fraction of the time of software simulation only. Realfast can work in conjunction with real-chip to provide hardware modeling as well as simulation acceleration.</p>	<p>Realmodel is a simulation subsystem specifically designed for quick and efficient simulation of system designs that include VLSI or VHSIC devices. Realmodel combines tightly coupled simulation acceleration and hardware modeling engines into a single, high performance system.</p> <p>Because Realmodel is integrated into the Valid Simulation Environment, accelerated simulation of designs containing models at switch, gate, functional, behavioral, and hardware levels may be performed with a single simulator having a single human interface.</p> <p>Realmodel's long simulation capability makes software-hardware integration of microprocessor-based designs possible for the first time, before the hardware is available. The design cycle can be shortened considerably by catching many hardware problems in simulation that would normally not be caught until the software was loaded and executed on actual hardware. Hardware integration can be simulated with application or operating system modules.</p>	<p>XCAT's HSE series includes the HSE-400 and the HSE-1000. The HSE (Hierarchical Simulation Engine) is the industry's first hardware accelerator specifically for engineers performing hierarchical designs. It provides very-high capacity and performance for multi-chip or system-level logic simulation through a hierarchical and parallel macro processor. With this unique integrated hardware/software approach XCAT is able to provide a capacity/performance increase of up to 10 times at a price increase of only about 1.5. As with all XCAT hardware accelerator systems, the designer has full interactive access to all design names, including those nested deep in the logic hierarchy. The HSE also includes asymmetrical rise/fall timing with a resolution of 0-4095 steps and an optional Pin-to-Pin timing simulator. There is also on-board memory which allows RAM/ROM models to be accelerated at the same speed as the logic models. Although the HSE series are primarily high performance logic simulators they do accelerate a reduced fault or switch level simulation.</p>

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Hardware Tools—Logic Simulation Accelerators (Cont'd)			
Source	XCAT	XCAT	Zycad
Tool Name	MX Logic/Fault Accelerator	MXT Logic/Fault/Timing Accel.	Expediter
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT	APOLLO, AT&T, CONTROL DATA, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PRIME, RIDGE, SUN, TEKTRONIX, Zycad proprietary
Hierarchical simulation			
Switch level		X	X
Gate level	X	X	X
Functional level	X	X	X
Behavioral level			X
Physical model level			
Network sharable	X	X	X
Field upgradable	X	X	X
User interface			
Batch mode			X
On-line (Interactive)	X	X	X
Algorithm accelerated	Event driven	Event driven	
Speed (events per second)	Up to 2 MEPS	Up to 2 MEPS	1 Meg.
Simulation size			
Type of primitive modeled	4-input 1-output	4-input 1-output	
Number of primitives modeled	Up to 64K	Up to 256K	
Number of states	4 (0, 1, X, Z)	16 Total- Logic 0,1,X,Z- Switch F,D,R,Z	12
Acceleration compared to reference software run on non-accelerated hardware	1000 times faster than software simulators running on a VAX 11/780.	1000X faster than software simulators running on a VAX 11/780.	1,000X Tegas on VAX 11/780.
Other functions accelerated	Fault simulation of up to 64K primitives at up to 6 MEPS.	Fault, timing, and switch level simulation.	
Description	System includes fault simulation. The Expediter is a turn key simulation system, and includes: Zilos; software drivers; optional TTL library; plus the Expediter simulation engine. Speed is one-million events per second.		
	XCAT's MX series of high performance hardware accelerator systems include the MX-50 and MX-100 logic and fault simulators. XCAT's simulator systems are interactive and multi-user. Up to seven designers using a personal computer can share one MX accelerator system. An even larger number of designers can take advantage of XCAT's multi-user software on Apollo or VAX systems. Interactive operations are designed into MX hardware accelerators and supported by XCAT's MX-SIM software and incremental compiler. The menu-driven software with help screens provides a turnkey simulation system. MX-SIM software is hierarchical and includes an incremental compiler as well as high level modeling capabilities. XCAT's hardware accelerator systems incorporate a number of features that emulate the way most designers develop and debug their designs. These features include rework, stop/restart and breakpoint. Optional netlist translators are available for popular workstations using TEGAS Design Language, Mentor, FutureNet and EDIF.	XCAT's MXT series of high performance hardware accelerator systems include the MXT-50, MXT-100 and the MXT-400 logic and fault simulators. The MXT series also include an asymmetrical rise/fall timing simulator and optional Pin-to-Pin timing and uni/bi-directional switch level simulators. An integrated hardware/software approach forms the basis of a turnkey system. MXSIM, the menu-driven software with an incremental compiler and numerous user/designer oriented utilities, make XCAT's systems easy to integrate into an existing design system and completes the turnkey approach. XCAT's hardware accelerator systems allow mixed mode simulation. MXSIM also includes a high-level modeling capability that allows designers to enter design models as Boolean equations, truth tables, parameterized macros or in the form of some behavioral description. The XCAT system allows the designer to switch interactively between logic and fault simulation without recompiling or reloading the network.	

DESIGN AUTOMATION



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Hardware Tools—Logic Simulation Accelerators (Cont'd)

Zycad Logic Evaluator	Zycad Magnum	Zycad System Development Engine	
APOLLO, AT&T, CONTROL DATA, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PRIME, RIDGE, SUN, TEKTRONIX, Zycad proprietary	APOLLO, AT&T, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, SUN, TEKTRONIX	APOLLO, AT&T, CONTROL DATA, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PRIME, RIDGE, SUN, TEKTRONIX, Zycad proprietary hardware	
X X X X X	X X X X	X X X	
X	X	X	
X	X	X	
X X	X X	X	
1 Meg to 16 Meg	500,000	1 Billion	
	128,000	1.1 million	
12	12	12	
Smallest model (LE1002) is 1000X + Tegas on VAX 11/780. Largest model (LE1032) is 16,000X + Tegas on VAX 11/780.	250X SILOS on VAX 11/780	100,000X Tegas on VAX 11/780.	
System includes accelerated fault simulation. There are 8 versions of the Logic Evaluator available. The Logic Evaluator can be installed using ZILOS software for a "turn key" type system. Zycad also pro- vides many translators including Tegas, Daisy, Mentor, Tektronix and HILO.	The Magnum is a low-cost logic and fault (optional) simulation accel- erator that can be used to simulate smaller designs (+ 128,000 gates) and portions of larger de- signs. The Magnum is fully com- patible with Zycad's larger logic and fault simulation accelerators.	The System Development Engine (SDE) is Zycad's most powerful ac- celerator, running at 1 billion events per second. The speed of the SDE permits "virtual prototyping", where microcode, operating systems, diagnostic soft- ware, etc., can be run on the simu- lated prototype.	

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Hardware Tools—Fault Simulation Accelerators			
Source	Aida	Aida	Case Technology
Tool Name	Aida CoSimulator Processor	Aida Persimulator Processor	CATS (see HHB Systems)
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, SUN	APOLLO	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT, SUN
Hierarchical simulation			
Switch level			X
Gate level	X	X	X
Functional level			X
Behavioral level			X
Physical model level			X
User interface			
Batch mode	X	X	X
On-line (Interactive)	X	X	
Network sharable	X	X	X
Field upgradable	X		X
Algorithm accelerated	Levelized Compiled Code	Levelized Compiled Code	CADAT fault simulation
Speed (fault evaluations per second)			16 million
Simulation parameters			
Type of primitive modeled	Gate	Gate	4 input one output
Number of primitives modeled	1 million gates	128,000 gates	2.1 million
Acceleration compared to reference software run on non-accelerated hardware	Accelerated Levelized Compiled Code is 100 times faster than LCC algorithm executing software.	Accelerated Levelized Compiled Code is 100 times faster than LCC algorithm executing in software.	10000 gate design that required 2 days on VAX 11/780 was completed in less than 1 hour.
Other functions accelerated	Aida Logic Simulation and Aida Automatic Test Pattern Generation.	Aida Logic Simulation and Aida Automatic test Patter Generation	Logic simulation.
Description	The Aida CoSimulator Processor is a proprietary hardware accelerator. Installed in an Apollo or Sun workstation, it speeds up the execution of the Logic Simulator, Fault Simulator, Fault Inferencer, and ATPG. With the CoSimulator Processor, it is possible to verify designs of up to 1 million gates at speeds of 5 million gate evaluations per second.	The Aida PerSimulator Processor is a proprietary hardware accelerator. Installed in an Apollo DN3000 or DN4000 workstation, it speeds up the execution of the Aida Logic and Fault Simulators. With the CoSimulator Processor, it is possible to verify designs of up to 128,000 gates at speeds of 5 million gate evaluations per second.	1000 times faster than VAX 11/780. Supports all levels of simulation. Expandable capacity for up to 2.1 million primitives. Stand alone or networked operation. Can be networked to any of the listed platforms. Parallel and pipeline processing. Uses 500 bit wide memory.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Hardware Tools—Fault Simulation Accelerators (Cont'd)

Daisy Systems MegaFAULT	Gateway Design Automation TESTGRADE-A	Harris Semiconductor CATS 9000F (see HHB Systems) page 4246	Hewlett-Packard Precision Architecture
Daisy MegaLOGICIAN	APOLLO, ELXSI	The CATS 9000 Sun-3 based machine	HEWLETT-PACKARD
X X X X	X X X	X X X X X	X X X X
X X	X X	X X	X X
	X	X	X
X	X	X	
	Proprietary	CADAT	HILO-3
	Depends on number of CPUs employed	16 million events per second	
64k	Gate/switch Up to 1,000,000 gates on Elxsi	4-input NAND 256K	HILO primitives 18
	On 10 CPU configuration, TESTGRADE-A runs 4000X TEGAS on VAX 11/780.	Speeds up to 578 times faster than software fault simulations have been achieved.	Same as HILO software accelerated
Daisy Logic Simulator, gate array layout.		Logic simulation	
<p>Daisy's MegaFAULT grades the effectiveness of test patterns in detecting potential manufacturing defects. It provides full function, technology independent fault simulation that is hardware accelerated on the Daisy MegaLOGICIAN.</p> <p>MegaFAULT provides fast convergent simulation that includes statistical coverage analysis, incremental and exhaustive modes. Users can analyze MegaFAULT results with a series of reports including both histograms and tabular reports.</p> <p>MegaFAULT and MDLS (accelerated logic simulation) share a common database. No model or netlist conversion is required- saving users time.</p>	<p>TESTGRADE-A is a distributed processing version of TESTGRADE which takes full advantage of ELXSI multi-processor computers. Up to 12 processors can be used with ELXSI with attendant performance that exceeds that of special purpose hardware accelerators. TESTGRADE-A also runs on networks of Apollo workstations with up to 10 nodes. TESTGRADE-A employs the latest simulation techniques, including many proprietary algorithms, to provide a highly efficient and powerful fault simulation capability for single stuck faults as well as for CMOS stuck-open faults. It simulates random sequential logic networks composed of TTL and/or MOS primitives, including the bi-directional pass devices and resistive MOS devices. TESTGRADE-A also provides very efficient simulation for random sequential logic networks containing such high-level primitives as multiport RAMs and ROMs. The 15-value simulator provides the resolution needed for effective simulation of dynamic MOS.</p> <p>Fault simulation can be performed in an incremental manner with no loss of data between incremental steps. Fault sampling is provided to facilitate quick experimentation. A powerful functional language is provided for the designer to concisely specify highly complex test programs for fault simulation. TESTGRADE-A includes an automatic test pattern generation capability that generates effective tests under user guidance.</p>	<p>The CATS 9000F Accelerator is a special purpose computer designed to perform logic and fault simulations at speeds up to 1000X faster than on a VAX 11/780. The core algorithms of the CADAT logic, timing, and fault simulator are implemented in full custom VLSI chips. During fault simulation, CADAT's concurrent algorithm inserts "stuck-at-one" and "stuck-at-zero" faults on inputs and outputs, and transistors which are stuck open or closed. Like logic simulation, the speed of fault simulation can be increased by adding extra CATS fault acceleration modules.</p>	

DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Hardware Tools—Fault Simulation Accelerators (Cont'd)			
Source	HHB Systems	IKOS Systems	Silicon Solutions/Zycad
Tool Name	CATS Accelerator	IKOS 800	Mach 1000F
FOR DETAILED DATA SEE:			
Tool residence	DEC VAX, DEC MICROVAX, MASSCOMP, SUN	IBM PC/XT/AT	APOLLO, DEC VAX, DEC MICROVAX, HEW-LETT-PACKARD, IBM MAINFRAME/MINI, SUN, TEKTRONIX, Silicon Solutions proprietary hardware
Hierarchical simulation			
Switch level	X		X
Gate level	X	X	X
Functional level	X		X
Behavioral level	X		X
Physical model level	X		X
User interface			
Batch mode	X		X
On-line (Interactive)	X	X	X
Network sharable	X	X	
Field upgradable	X	X	X
Algorithm accelerated	CADAT concurrent fault simulation		Concurrent fault
Speed (fault evaluations per second)	500k per module		
Simulation parameters			
Type of primitive modeled	4 input, combinational and sequential	4-input/1-output table driven	
Number of primitives modeled	256 user definable	64,000	512,000
Acceleration compared to reference software run on non-accelerated hardware	500X CADAT on a VAX 11/780		1000X Cadat on VAX 11/780.
Other functions accelerated	Logic simulation		
Description	<p>The CATS Accelerator is a special purpose computer designed to perform logic and fault simulation at speeds up to 500 times faster than on a VAX 11/780. Yet, it is available at a workstation price.</p> <p>The core algorithms of the CADAT 6.0 logic, timing and fault simulator are implemented in full custom VLSI chips. Additionally, the CATS Accelerator takes full advantage of pipeline and parallel processing and a 500 bit wide memory. Up to 8 accelerator modules can be attached in parallel to allow simulations of up to 512 thousand primitives at speeds up to 4 million events per second.</p>		<p>The Mach 1000F performs high-speed fault simulation two to three hundred times faster than a VAX 11/780, depending on system configuration and circuit size. The machine has a capacity for a logic description of over 64,000 modeling elements, expandable to over one million. The Mach 1000F is used by design and test engineers to develop comprehensive, reliable test vectors. It enables engineers to simulate manufacturing defects by introducing deliberate faults into the netlist logic description of computer systems, printed circuit boards, and integrated circuits including CMOS, MOS, and bipolar technologies. Suites of test vectors are then applied to the "faulted" netlist of a logic description to verify that the test vectors can identify the faults. The Mach 1000F is based on the same technology as the Mach 1000 Logic Accelerator and includes all Mach 1000 logic simulation capabilities plus concurrent fault simulation capabilities implemented completely in hardware.</p>



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Hardware Tools—Fault Simulation Accelerators (Cont'd)**

Simulog SuperSim	XCAT MX/MXT Fault/Logic Accelerator	Zycad Fault Evaluator	
DEC MICROVAX	APOLLO, DEC VAX, DEC MICROVAX, IBM PC/XT/AT	APOLLO, AT&T, CONTROL DATA, CRAY, DATA GENERAL, DEC VAX, DEC MICROVAX, IBM MAINFRAME/MINI, PRIME, RIDGE, SUN, TEKTRONIX, Zycad proprietary hardware	
X X  X	X X X	X X X	
X X X	X	X X	
X	X	X	
X	X	X	
Serial or parallel insertion (100%)	Parallel	Concurrent fault	
Runs the same speed as logic simulator	Up to 6 MEPS		
2-input (+ 1 expand) logic gate, or D-FF 1M standard, up to 8M	4-input 1-output Up to 256K	512,000	
100,000X.	50-100 times faster than software simulators running on a VAX 11/780.	Smallest version is 300x SILOS on VAX 11/780.	
Pre-simulation activities: a) network compilation, b) network load, c) pattern (stimuli) and memory loads.	Logic, timing, switch level simulation.		
<p>Simulog, Inc. has a family of six standard machines with simulation speeds of 10 Giga to 200 Giga gate evaluations per second and gate capacity of 32K to 1M, respectively. Models of up to 8M gates are available. SuperSim is a fully interactive machine: Breakpoints specifying complex conditions may be used to interrupt a simulation, then any network node may be checked and its logic level changed if desired.</p> <p>A designer may interactively build additional circuitry and wire it into the already existing simulated design. He may rewire (connect and disconnect) portions of the network and continue simulating the altered network without having to recompile. SuperSim may be operated as a stand-alone system or a network server, and it has a multi-user option (up to 8 concurrent users).</p>	<p>XCAT's MX/MXT series of logic and fault hardware accelerator systems include the MX-50, MX-100, MXT-50, MXT-100 and the MXT-400. XCAT's MX/MXT systems are both logic and fault simulators. The MXSIM software allows the designer to switch interactively loading the network. XCAT's fault simulator features three types of stuck-at-faults (0,1,Z) that can be applied to input as well as output pins. MXSIM also includes utilities to automatically generate a fault list. The designer has the option of choosing between prime faults, macro pin faults or total fault mode. The designer can also include or exclude blocks of faults from the system-generated fault list. XCAT software also includes utilities for building fault coverage statistics and analysis.</p>	<p>In conjunction with existing Fault Evaluator lines, Zycad is offering FE models at substantially lower cost than previously required Logic Evaluator/Fault Evaluator combinations. Both FE product groups deliver fault simulation speeds up to 500 times faster than software-based concurrent fault simulators running on mainframe computers, and can handle designs containing up to 512,000 gates. The FE-1000 Series Fault Evaluator is targeted for engineers performing fault simulation on VLSI chips, subsystems, or large system designs at the functional or gate level. The FE-2000 Series was created for markets requiring switch-level fault simulation such as the semiconductor industry, and most notably ASIC or ASIC-predominant systems. The FE-2000 provides MOS or bipolar transistor modeling with bi-directional switches. The Fault Evaluator-2000 Series analyzes bi-directional-switch flow and fans out the appropriate levels and strengths. Other transistor-level models include uni-directional transfer switches and wired functions.</p>	

Bold face indicates data is provided in the page noted

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Hardware Tools—IC Prototype Test Systems			
Source	CADIC, Inc.	CADIC, Inc.	CADIC, Inc.
Tool Name	STM4100 Digital VLSI Test Sys.	STM5100 Digital VLSI Test Sys.	STM5200 Digital Test System
FOR DETAILED DATA SEE:			
Tool residence	IBM PC/XT/AT	IBM PC/XT/AT	IBM PC/XT/AT
Universal test fixture	X	X	X
Integrated with following workstations	Sentry; General purpose CAE interface	Sentry; general purpose CAE interface	Sentry; general purpose CAE interface
Channels per mainframe	64 to 256 channels (all bidirectional)	32 to 256 channels (all bidirectional)	32 to 352 channels (all bidirectional)
Pattern gen. channels (min/max)	64 to 256	32 to 256	32 to 352
Logic state channels (min/max)	64 to 256	32 to 256	32 to 352
Timing analysis channels (min/max)	64 to 256	32 to 256	32 to 352
Memory depth per channel (min/max)	Unlimited (>64k)	64K	64k
Logic anal. clock speed (MHz)	PC I/O	20 MHz	50 MHz
Data acquisition speed (MHz max)	PC I/O	10 MHz	50 MHz
Timing analysis clock speed (MHz)		20 MHz	50 MHz
Description	The STM4100 is a low cost, flexible tool for quick and efficient verification and failure analysis of devices at the engineer's bench. Features include: SoftWire Fixturing; Per-Pin Architecture; Up to 256 Bidirectional Pins; Unlimited Test Vector Depth; Learn Mode; Menu-Driven Software; Automatic Pattern Generation; Automatic Self Test.	The STM5100 is a flexible, low cost, portable system based on high pin-count and a per-pin architecture. Features include: SoftWire Fixturing; Per-Pin Architecture; Up to 256 Bidirectional Pins; 64k Vector Depth; Built-In Autocalibration; Expanded Timing Formats; Learn Mode; Real-Time Hardware Compare; Menu-Driven Software.	The STM5200 is similar to the STM5100 but features much higher performance. Features include: SoftWire Fixturing; Per-Pin Architecture; Configurable up to 352 Bidirectional Pins; All Pins Individually Maskable; Test Rate: 25 MHz in Normal Mode, 50 MHz in Double Return Mode, 50 MHz in Memory Multiplex Mode; 4 programmable Driver and Sense Voltage Pins; Slew Rate > 1.5 Volts/ns; Drive Capabilities of 50mA @ 50ohms; System Accuracy + /- 1.5 ns; and, Independant Timing Edges.



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Hardware Tools—IC Prototype Test Systems (Cont'd)**

Calma CATSCOPE	Daisy Systems Engineering Test System	Ferranti Interdesign Ferranti Test System	Hewlett-Packard 81810S
APOLLO, + I.M.S. Logic Master	Daisy Personal Logician	DEC VAX, DEC MICROVAX	HEWLETT-PACKARD
X	X		
Calma	Daisy	DEC MicroVAX	HP9000 Series 300
16/384	128 (max 384)	140	
16/384	32/192	140	
16/384	32/192	140	
16/384	4/24	140	8 minimum, 256 maximum channels
8k to 192k	192	32K	16K per channel
20		1	
20	40	1	50 MHz
20		10	
Timing channel resolution: 1ns. Emulation of GHz logic analyzer.	Daisy ETS can input stimulus and acquire at 40 MHz with 1ns resolution.		ASIC verification system. This system links through the Hewlett-Packard Design Center to EE EDS tools.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Hardware Tools—IC Prototype Test Systems (Cont'd)			
Source	Hilevel Technology	Hilevel Technology	Hilevel Technology
Tool Name	CAE/LINK	HALE SPG	TOPAZ 25
FOR DETAILED DATA SEE:	page 4652	page 4652	page 4652
Tool residence			IBM PC/XT/AT, TOPAZ 25
Universal test fixture			
Integrated with following workstations			
Channels per mainframe	288 signal pins	288 signal pins	288 signal pins
Pattern gen. channels (min/max)	0/288 with six stimulus data formats	0/288 with six stimulus data formats	0/288 with six stimulus data formats
Logic state channels (min/max)			0/256 channels 4K deep
Timing analysis channels (min/max)			N/A
Memory depth per channel (min/max)	4K, 16K, or 64K	4K, 16K, or 64K	4K, 16K, or 64K
Logic anal. clock speed (MHz)	50	25MHz (fast assembly time)	25
Data acquisition speed (MHz max)	50		25
Timing analysis clock speed (MHz)			N/A
Description	<p>This optional software package provides a communications path from computer simulation workstations to the Topaz series design verification test systems. It also provides vector translation so software test vectors developed in simulation may be re-assigned and converted into hardware test vectors for the Topaz series testers.</p> <p>CAE/LINK is general purpose and works with any workstation capable of storing simulation vecotrs in an ASCII file. Time stamps can be created by CAE/LINK. If the source vector file contains time stamps they may be maintained or scaled by the translation algorithm.</p> <p>Limited to: Daisy Systems, Valid Logic, Mentor Graphics, FutureNet or any vectors that can be stored in an ASCII file.</p>	<p>HALE SPG is Hilevel's assembly language environment Symbolic Pattern Generator (SPG). HALE SPG allows a user to generate his own complex test vector programs written with user-defined symbols and mnemonics. These programs are then assembled into test vectors for use by the Topaz system. This software program is a relocatable macro meta assembler program which can execute on an IBM-PC with a minimum memory of 256 kbytes or on a VAX 11/750 system using the Berkeley UNIX or VMS operating system. The program is supplied in the form of diskette resident executable files for the IBM-PC or magnetic tape resident executable files for the VAX 11/750.</p>	<p>The TOPAZ 25 is a 25 MHz design verification system capable of testing VLSI devices with 288 signal pins. State-of-the-art features include real time operation and verification up to 25 MHz, programmable drivers and receivers on each pin, 500 psec timing resolution, automatic deskewing, fully integrated logic state analyzer, and a software link to most CAE simulator programs. With mechanical fixturing that supports devices with up to 512 pins, the electronics may be expanded in 18-pin increments up to the maximum of 288 signal pins. The memory plug-in options, known as SRC modules, offer a choise of 4K, 16K or 64K deep vector memories. Each SRC option supports 16 I/O pins and provides two independently controlled strobepins. Timing and formats of I/O pins may be programmed in 8 pin segments. Timing and format of I/O pins may be programmed in 8 pin segments. All strobe pins may be individually controlled.</p>



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Hardware Tools—IC Prototype Test Systems (Cont'd)**

Hilevel Technology TOPAZ 50 page 4652	Hilevel Technology TOPAZ FX page 4652	Hilevel Technology TOPAZ II page 4652	Integrated Measurement Systems Logic Master
IBM PC/XT/AT, TOPAZ 50	IBM PC/XT/AT	IBM PC/XT/AT	I.M.S. proprietary
			X
			Gateway Design Automation
288 signal pins	252 signal pins	288 signal pins	384 in two mainframes
0/288 with six stimulus data formats	0/252 with six stimulus data formats	0/288 with six stimulus data formats	16/384
0/256 channels 2K deep	0/256 channels 2K deep	0/256 channels 2K deep	16/384
N/A			2/48
4K or 16K	4K or 16K	4K, 16K, or 64K	16
50	50		20
50	50		20
N/A			1ns timing resolution
The TOPAZ 50 is a 50 MHz design verification system capable of testing VLSI devices with 288 signal pins. State-of-the-art features include real time operation and verification up to 50 MHz, programmable drivers and receivers on each pin, 500 psec timing resolution, automatic deskewing, fully integrated logic state analyzer, and a software link to most CAE simulator programs. With mechanical fixturing that supports devices with up to 512 pins, the electronics may be expanded in 18 pin increments up to the maximum of 288 signal pins. The memory plug-in options, known as SRC modules, offer a choice of 4K or 16K deep vector memories. Each SRC option supports 16 I/O pins and provides two independently controlled strobe pins. Timing and formats of I/O pins may be programmed in 8 pin segments. All strobe pins may be individually controlled.	The TOPAZ FX is Highlevel's affordable verification system capable of testing CMOS and TTL VLSI devices with 252 pins up to 30 MHz. State-of-the-art features include real time comparison, fully programmable receivers, and drivers programmable from +4.5V to +5.5V on each pin, 500 psec timing resolution, automatic deskewing, fully integrated fault analyzer, and a software link to most CAE simulator programs.  With mechanical fixturing that supports devices with up to 512 pins, the electronics may be expanded in 18 pin increments up to the maximum of 252 signal pins. The memory plug-in options, known as SRCA modules, offer a choice of 4K or 16K deep vector memories. Each SRCA option supports 16 I/O pins and provides two independently controlled strobe pins. Timing and formats of I/O pins may be programmed in 8 pin segments. All strobe pins may be individually controlled. Universal DUT fixture and wafer probe interface are available.	The Topaz II is a High Performance 50 MHz Design Verification System capable of testing VLSI devices with 100 ps timing resolution. State-of-the-art features include 288 signal pins, real time comparison, 16 globally assignable timing delays, variable clock frequency from 25 KHz to 50 MHz in .025 MHz steps.  Programmable drivers and receivers on each pin, automatic deskewing, fully integrated logic state analyzer, and a software link to most CAE simulator programs. With mechanical fixturing that supports devices with up to 512 pins, the electronics may be expanded in 18 pin increments up to 512 pins, the electronics may be expanded in 18 pin increments up to the maximum of 288 signal pins. The memory plug-in options, known as SRC modules, offer a choice of 4K, 16K, or 64K deep vector memories. Each SRC option supports 16 I/O pins and provides two independently controlled strobe pins. Timing and formats of I/O pins may be programmed in 8 pin segments. All strobe pins may be individually controlled. Universal DUT fixtures and wafer probe interfaces available. Shmoo plotting, DC parameters, LSSD, and programmable pattern generator options.	Features real-time comparison. Programmable driver and receiver levels. Resident simulator download conversion software.

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Hardware Tools—IC Prototype Test Systems (Cont'd)			
Source	Mentor Graphics	Tektronix	
Tool Name	Hardware Verification System	DAS9100	
FOR DETAILED DATA SEE:			
Tool residence	APOLLO, + Mentor proprietary hardware	Tektronix proprietary	
Universal test fixture	X	X	
Integrated with following workstations	Mentor Graphics	Tektronix	
Channels per mainframe	160 + 18 clock and controller	216	
Pattern gen. channels (min/max)	32/160	16/216	
Logic state channels (min/max)	32/160	32/96	
Timing analysis channels (min/max)	16/16	32/96	
Memory depth per channel (min/max)	4K Logic State; 8K Pattern Generation	512	
Logic anal. clock speed (MHz)	50	25	
Data acquisition speed (MHz max)	20	25	
Timing analysis clock speed (MHz)	100	2 GHz	
Description	<p>Mentor Graphics' Hardware Verification System (HVS) is a fully integrated Logic Analyzer and Pattern Generator that provides test and verification for prototype designs. HVS software allows an engineer access to the entire design database. This enhances productivity by allowing direct upload of software simulation vectors into Pattern Generation memory. Similarly, software simulation results can be compared to actual data gathered by the Logic Analyzer facilitating analysis. Also, the HVS software can call upon stored mnemonic disassembly tables to convert acquired data into a more user-readable form. This includes both standard microprocessor and special user-defined instruction sets.</p> <p>HVS communicates to any Mentor Graphics workstation through an RS-232 interface port, so it can be easily moved from project to project. Multiple HVS mainframes can be daisy-chained to expand the number of available channels of pattern generation or data acquisition.</p>	<p>Controlled by Tektronix CAE2000 DAS Link interface software.</p>	



**DESIGN AUTOMATION—Design Tools****Generic Function****Design Tool Capability****Miscellaneous Design Tools**

Source	Technology Modeling Associates	Cadnetix	MicroSim
Tool Name	SUPREM-3	CDX-760 RISC Engine	PSpice Digital Files
<b>FOR DETAILED DATA SEE:</b>			
Function	1-D Process Modeling Program	Accelerator for Compilation & Analog Sim	Analog/Digital Simulation Link
<b>Description</b>	<p>A versatile IC process simulation program with electrical calculation capabilities, SUPREM-3 simulates complete fabrication processes for both MOS and bipolar devices. It models the changes in the impurity distributions and material layer thicknesses of a device structure during processing and then calculates the electrical characteristics of the resulting device. The simulation is one-dimensional along the direction perpendicular to the wafer surface.</p> <p>SUPREM-3 can model a wide variety of device structures composed of as many as 10 separate layers. These layers may consist of any of 10 different materials, including the default materials silicon, polysilicon, silicon dioxide, silicon nitride, and aluminum. As many as six impurities, including boron, phosphorus, arsenic, and antimony, may be implanted, diffused, or included in deposited layers to develop simulated structure.</p> <p>TMA's proprietary version of SUPREM-3 has major enhancements resulting from years of industrial feedback and continuing development by TMA's process engineers. These enhancements include: improved accuracy of process models and electrical calculations, additional informative output, and new features that add to its flexibility and ease of use.</p>	<p>Cadnetix' RISC Engine is an accelerator based on the MIPS Computer Systems, Inc. R2065 Series Component Kit. The 8 MB single-card accelerator, designated the CDX-760, utilizes RISC technology and operates at an effective rate of 10 mips. The RISC Engine also features a floating point processor, cache memory and facilities for parallel processing.</p> <p>The RISC Engine is fully compatible with existing Cadnetix engines, and can be added as an option to the CDX-70000. Accelerated applications on the RISC Engine are to be the SABER analog simulator from Analogy, Inc. and schematic compilation.</p>	<p>The Digital Files option allows PSpice to interface with digital simulators. It reads and writes files in the correct format for several popular logic simulators, including ViewSim and CADAT. With this option you can run a digital simulator and then use its output as input to PSpice. Conversely, you can run PSpice and have it create a file to be used as input to a digital simulator. In both cases, PSpice does the necessary D to A and A to D conversion.</p>

DESIGN AUTOMATION—Design Tools			
Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source	Intergraph	Genrad	HHB Systems
Tool Name	TANTEST	HITEST	THESEUS
FOR DETAILED DATA SEE:			
Function	ATPG and Scan Path Generation	Automatic Test Pattern Generation	Automatic Test Pattern Generation
Description	<p>TANTEST automatically synthesizes scan-path test circuitry into a cell-based IC design and then automatically generates test patterns for complete fault coverage. The integration of TANTEST into the TANCELL cell-based IC design system greatly simplifies design for testability. The package minimizes overall die size and reduces the impact of circuit timing performance associated with adding scan-path testability to a design.</p>	<p>The HITEST Test Generation System is a suite of software tools used to create test data for digital logic circuits. The HITEST software can be used by designers and test engineers to develop test programs for Application Specific Integrated Circuits, full custom integrated circuits, printed circuit boards and systems.</p> <p>The HITEST test generator provides automatic test generation for circuits that adhere to a scan-based design-for-test methodology. The number of vectors generated is optimized for efficient test throughput on the target ATE.</p> <p>Automatic test generation to 100% fault coverage can be accomplished with the combinational test generation module in HITEST. Non-scan circuits that exhibit good testability structure can also be handled by the HITEST test generator.</p> <p>General purpose test generation modules coupled with a very interactive user environment enables the engineer to create a "dialog" with the test generator, guiding the test generation process for maximum fault coverage.</p>	<p>Theseus generates test programs for contemporary ASIC chips. The circuit may consist of combinational gates, flip flops, counters, shift registers and scan-path devices. Theseus takes advantage of testability analysis for producing efficient vectors. Interactive Testability Analysis (ITA) provides a tool for experimenting with techniques to improve testability. Knowledge Base Compiler (KBC) provides a means of accepting user supplied information which controls the test generation process. Theseus is available on popular computers such as VAX (UNIX and VMS) and Sun workstations.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Miscellaneous Design Tools (Cont'd)

Aida Aida ATPG	Gateway Design Automation TESTSCAN	Praxis Systems ELLA	CAD Group, Inc. (CGI) SHDL(SALT Hdware Descr. Lang.
Automatic Test Pattern Generator	Automatic Test Pattern Generator	Behavioral Language for VLSI Design	Behavioral Model Simulator
<p>The Aida Automatic Test Pattern Generator guarantees automatic generation of test patterns yielding 100% coverage of detectable faults. ATPG produces test patterns automatically, using a combination of both path sensitizing and random vector generation algorithms. Includes a scan path logic conversion/synthesis tool.</p> <p>ATPG provides 100% coverage of detectable single stuck-at faults and obtains improved performance through fault simulation. It is optimized for large complex digital system designs. ATPG can be used as a shared engineering resource within the Aida Design System network. It accepts designs created using the Aida Design Creation System or translated from other systems.</p>	<p>TESTSCAN is an automatic test generation system for digital circuits that use structured design for testability techniques. TESTSCAN is claimed as the only commercially available system that guarantees totally automatic test generation for VLSI-complexity products that employ scan design disciplines. Automatic test vector generation for VLSI logic networks (50,000 gates and higher) is made practical with the TESTSCAN system. TESTSCAN is a push-button system. Besides any one of the four published scan disciplines, a very flexible form of functional scan design may be used with TESTSCAN. The published forms of scan design include Random Access Scan developed by Am-dahl/Fujitsu, Scan Set developed by Sperry-Univac, Level-Sensitive Scan Design developed by IBM, and Scan Path developed by Nippon Electric.</p> <p>TESTSCAN consists of three processes: the design audit which checks a logic network for compliance with the critical design rules embodied in the various scan disciplines, the generation process which provides automatic test pattern generation and test compaction, and a grading process which provides fault grading along with a fault dictionary. Precise diagnostics are provided to the user for violations of the scan design rules. TESTSCAN generally provides 100 percent detection of all detectable faults in the network. The system is capable of determining whether or not a stuck fault is untestable and informs the user about such faults.</p>	<p>The ELLA Design System is a VLSI design system based on a behavioral hardware description language, a simulator and comprehensive design support environment. ELLA is unique among behavioral languages in that it has a common notation for behavior and structure. This means that the decomposition of behavior to structure is very efficient, significantly speeding up the design process. Additionally, ELLA is a succinct, yet very powerful language and is easy to learn and use. A procedural interface is provided to the ELLA database which allows translations of designs to lower-level tools.</p> <p>The ELLA system is now in use in many of the UK's major electronics companies significantly reducing design time and cost and increasing design quality. ELLA is marketed in the US by ECAD Inc.</p>	<p>SHDL describes behavior at an abstract level in actual hardware terms. SHDL is a register transfer language, simulator and debugger, which uses the "C" programming language to create behavioral model definitions. After describing a model in hardware terms, SHDL translates the hardware description into the "C" programming language. It may then be simulated and debugged with the SHDL simulator. This procedural language simulator can be used to quickly code and simulate hardware modules, which may then be linked together to form large hardware functions.</p> <p>After using SHDL to describe models at any level of complexity, from the most complex systems architecture level, down to the simplest gate level, the correct behavior of a new model may be analyzed with the SHDL simulator and debugger. The SHDL simulator and debugger can then be used to analyze the behavior of a single model or to analyze complete systems consisting of many models. SHDL may be used to quickly analyze many different approaches to a design, after determining the most desired design, the new models may then be added to the SALT simulator where they can be used in a true hierarchical, mixed level simulation environment that allows concurrent simulation of all levels of hierarchy including behavioral, functional, macro, gate, and switch levels.</p> <p>Models Developed in "C". The second method to create user models, is to define them directly in the "C" programming language. Although some knowledge of programming is required, this method has been developed in a way that allows a user with limited programming skills to accurately construct a new model. After a new model has been created with this method, it may be simulated with the SHDL simulator and debugger before placing it into the SALT simulator. In addition, models that have been designed with SHDL, may be modified at the "C" language level.</p>

DESIGN AUTOMATION—Design Tools			
Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source	EXAR	Octal	EEsof
Tool Name	XRSIM	Direct CAD Database Converters	E-SYN
FOR DETAILED DATA SEE:	page 4222		
Function	Bipolar Circuit Analysis	CAD Database Conversion	Circuit Synthesis
Description	<p>XRSIM is a fast circuit analysis system for bipolar circuit designs. XRSIM utilizes a simple device model and hence gains much of its speed. It utilizes an algorithm for adaptive time step selection which gives rise to more speed gains. Between 10 and 40 times speed gains over the standard SPICE 2G5 have been observed. A very flexible data viewing system is linked with it to present and manipulate simulation data. Currently XRSIM runs on the IBM/AT, PS2 (all models) and Apollo.</p>	<p>Direct conversions offer many advantages over conversion via so-called "neutral" formats, which do not represent the required union of all CAD databases in one format. COMPLETENESS: Direct converters are not subject to different interpretations or different levels of support of a neutral family by different CAD vendors. Direct converters convert 100% of the database, including dimensions, text, and non-graphic information, subject only to the limitations of the output CAD system. Direct conversion is not affected by limitations of an intermediate format or by vendor fears of providing efficient paths out of their system. ACCURACY: Unlike with vendor-written pre- and post-processors, the author of the direct converter is expert in both databases. "Touch-up" is never required after conversion. EASE OF USE: Direct converters usually read and write existing archival data formats directly. You need not own both kinds of CAD systems. Converters execute on various hardware platforms, including: VAX/VMS, VAX/UNIX, IBM VM/CMS, IBM MVS, Prime, Apollo, and IBM PC/AT. PERFORMANCE: Direct converters are efficient since they process the database only once with a single program running on a single computer.</p>	<p>For synthesis of lumped element, noise-matching, interstage matching, impedance-matching, multiplexers, and filter networks based on supplied electrical specifications. Provides amplitude shaping in filter and amplifier design work. Reduces design time by eliminating look-up tables and extensive hand calculations; maximizes circuit efficiency by providing several different circuit topologies to choose from. After synthesis is complete, E-SYN translates the network into a Touchstone circuit file for verification of the electrical response.</p>



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Miscellaneous Design Tools (Cont'd)			
Berne Electronics ELAN-MOD	EEsof TOUCHSTONE Sr.	Meta-Software SUXES-10	MicroSim PSpice Parts
Component Modeling/Parameter Extraction	Component Modeling/Parameter Extraction	Component Modeling/Parameter Extraction	Component Modeling/Parameter Extraction
Interactive transistor and diode modeling program for deriving non-linear model parameters from data usually available from manufacturer's specifications and/or laboratory measurements. Allows user to enter data from measurements or from spec sheets. Uses default values when the user doesn't have appropriate data. User can check, modify and recalculate parameters, until suitable model data is obtained.	For modeling custom or proprietary elements and incorporating them into TOUCHSTONE's extensive element library. Provides full access to TOUCHSTONE- interactive tuning, linear analysis, and optimization. Includes all of the TOUCHSTONE elements plus ten user-defined ones. An ideal tool for designers who know how to mathematically model microwave elements in terms of their S-parameters, and are familiar with Pascal. With TOUCHSTONE Sr. and these skills, the designer's special knowledge is readily available to others.	The SUXES-10 program is a tool for the extraction and optimization of device model parameters. SUXES-10 generates the set of model parameters that create the best fit between the model equation results and a specified set of points- generally, current/voltage curves measured in a laboratory. The optimization technique is independent of the model equation, so new models may be incorporated simply by inserting the equations into the SUXES-10 program shell. SUXES already incorporates the model equations from HSPICE, SPICE2G.6, ASPEC, and SUPREM.	Microsim's PARTS program allows a user to generate PSPICEparameters by means of curve fitting standard data book parameters. Coupled with Microsim's device model library (included with PSPICE) the user is provided with over 200 devices including OpAmps, power MOSFETs, voltage comparators, diodes, and bipolar transistors) and the capability to generate additional component parameters with relative ease. PARTS is purchased as an optional program to augment Microsim's SPICE.

DESIGN AUTOMATION—Design Tools			
Generic Function	Design Tool Capability		
Miscellaneous Design Tools (Cont'd)			
Source	MOSAID	Silvaco Data Systems	Technology Modeling Associates
Tool Name	MOSFIT	UTMOST	TOPEX
FOR DETAILED DATA SEE:			
Function	Component Modeling/Parameter Extraction	Component Modeling/Parameter Extraction	Component Modeling/Parameter Extraction
Description	<p>MOSFIT is a tool for extracting semiconductor model parameters from test device measurements. Consisting of three components for data acquisition, parameter optimization and plotting, MOSFIT will generate global parameter sets that are independent of bias conditions and device geometry. The package is available on a variety of hardware including IBM PC/XT/AT machines, DEC VAX and PDP-11 and Keithley parametric testers.</p> <p>MOSFIT is used as an accessory to any circuit simulator (e.g. SPICE). It provides the means for calibrating the simulator to the IC fabrication process by generating accurate model parameters from real measurements on fabricated test devices. The program can accommodate any user-defined model and, in addition, has powerful MOSFIT analysis methodology built in which includes the industry standard SPICE MOS models. The plotting facility displays measured and simulated I-V curves and serves as an interactive learning aid for understanding the modes and effects of parameter variation.</p>	<p>UTMOST (Universal Modeling Software Technique) provides complete solutions for device characterization and modeling in an interactive environment. Design engineers use UTMOST to perform device parameter extraction on a semiconductor which is similar (uses the same fabrication process) to the semiconductor they're designing. UTMOST fully characterizes bipolar devices to 10 GHz and beyond. The accuracy of the newly extracted parameters is verified by UTMOST using one of the many MOS or bipolar device models such as SPICE, which is coded into UTMOST.</p>	<p>In most cases, users must not only know how a single device behaves but how to describe it accurately to a circuit simulator by means of a model with the appropriate parameters. To fulfill this need TMA developed TOPEX, a parameter extraction and model development program. A general-purpose program that fits mathematical models to measured or simulated data, TOPEX is especially useful for extracting parameters for circuit simulation. It comes complete with SPICE MOS and bipolar models, but it also allows users to develop and implement models of their own. TOPEX can easily be adapted to complement virtually any circuit simulation program.</p> <p>Allowing flexible input, simulated data from TMA's device simulation programs or experimental data is read. Parameters that minimize the relative error at selected data points are extracted by a sophisticated optimization algorithm that always converges. The sensitivity of the fit to each parameter and the dependencies among the parameters are computed automatically. The extracted parameter values may be saved in a file for future use. They can be input into a circuit simulator or may be used as initial values for subsequent TOPEX simulations.</p>



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Miscellaneous Design Tools (Cont'd)**

Clarity Systems PlaSet	Clarity Systems GluSet	Cadtec SHERPA	FutureNet (Data I/O) DASH-CADAT Plus page 4651
Custom PLA Block Layout	Custom Random Logic Generator	Database/Program Management	Database/Program Management
<p>PlaSet provides quick and automatic generation of PLA block layout. It makes use of a finite variety of "Tiles" which are defined as part of a geometric view. Tiles are created for such structures as input and output buffers, "AND" plane and "OR" plane core cells as well as for programmed versions of the core cells. The tiles are constructed using the powerful editing commands of the geometric layout editor GEDI. The logical input to PlaSet is a truth table description of the PLA block in terms of its input and output. This truth table can be constructed and edited using SimuSet's Behavioral Description Language Editor (BDL-ED) for error-free, methodology compliant behavioral view creation. The same truth table description also provides the behavior of the PLA block for digital simulation via SimuSet's MIXIM simulator. With PlaSet, the designer can minimize the PLA truth table for the smallest number of terms, resulting in the most compacted physical layout. PlaSet checks for redundant input, output and minterms. It then provides a cross reference between original and resulting truth tables for quick correlation and identification of the areas where minimizations have occurred. The result of PlaSet is a completed physical layout of a PLA as a geometric view. This block can then be used either alongside other layout blocks in the geometric editor GEDI, or it can be instantiated in the topological editor.</p>	<p>GluSet provides quick and automatic generation of dense random logic layout directly from the schematic view. Once a schematic view has been defined using StrucSet, and all of the relevant device sizes have been determined, GluSet can be invoked to produce the layout. GluSet is based on a sophisticated proprietary algorithm that minimizes the horizontal size of the block (or cell) by optimally ordering transistors such that the number of separations between regions of diffusion are minimized. By assigning the transistor length and width attributes to gates in the schematic view of the design, the designer has full control over the layout device sizes. Due to SuperSet's integrated design database, these parameters are then passed directly to the layout.</p> <p>GluSet's output is produced as a topological, or symbolic layout view. Due to the tight integration of SuperSet's modules, the designer can run the layout compaction program (COMPACTOR) directly on the symbolic layout, to yields extremely high device densities. Process independence is achieved due to the fact that compaction uses a technology file that contains process design rules.</p>	<p>Sherpa is a software system that manages product development and the release process for engineering organizations using computer design tools. Sherpa manages the development process online and controls its results throughout the project life cycle. This new system allows an engineering installation to automatically develop and enforce a design methodology unique to each of its design projects.</p> <p>Sherpa automatically requests and collects data on a project's status thereby ensuring that its database of status information is up-to-date at all times. It then uses this information as the basis for enforcing standards of product development.</p>	<p>DASH-CADAT PLUS is a high level executive program that links, unifies, and controls standalone CAE tools with a common menu. The executive also provides a scrollable waveform generator that shows tasks. DASH-CADAT Plus is for DASH personal workstations with DASH monochrome and DASH-3C color enhanced displays. It integrates the logic design tasks of schematic capture, net list extraction, logic and fault simulations, as well as test vector development and simulation of low-end ASICs.</p>

## DESIGN AUTOMATION—Design Tools

Generic Function

Design Tool Capability

## Miscellaneous Design Tools (Cont'd)

Source	Systems Calculations	Valid Logic Systems Inc.	Technology Modeling Associates
Tool Name	CircuitBase	DIAL	CANDE
FOR DETAILED DATA SEE:		page 4660	
Function	Database/Program Management	Design Interface and Access Language	Device Modeling
Description	<p>CircuitBase is a database structure designed to store engineering data about printed circuit boards. CircuitBase comes with software which: 1. creates database entries from the output of schematic entry programs; 2. extracts from the database to form input for CAE/CAD tools; 3. injects results of CAE/CAD analyses back to the database; and, 4. provides reports to management. The CircuitBase structure and software can be customized to the relational database system. This open architecture approach gives maximum flexibility and access to design data. CircuitBase is available on VAX mainframes and on IBM-PC compatibles.</p> <p>Interfaces already in place: Case CT1000/2000, Predictor, PC-Predictor, CYBERNET*EXPRESS and Datatrieve. In progress: HS-PICE, ICAP, PC-ICAP and DBASE-II.</p>	<p>DIAL has been developed to provide Valid system users access to the components of the design database. DIAL consists of a set of library routines, subprograms, and support utilities that can be assembled into a powerful, user-defined interface program written in Pascal.</p> <p>By using DIAL, user-defined custom interfaces to external analysis tools and physical design systems can be written with minimal effort and in a significantly shorter period of time. Numerous high-level operations are predefined; routines to read and process each of the database files minimize the amount of effort required to implement the interface.</p> <p>Through DIAL, access to both the logical and physical descriptions of the design as well as the component libraries is permitted. The user defines both the data to be accessed and the format of the data to be presented.</p>	<p>Two-dimensional MOS device simulation program. CANDE models the two-dimensional distributions of potential and carrier concentrations in a device to predict its electrical characteristics for any bias condition. It solves Poisson's equation and either the electron or hole current-continuity equation to analyze devices such as MOS-FETs, JFETs, MESFETs, CCDs and high power MOS devices in which current flow is dominated by a single carrier. CANDE can model a wide variety of device structures composed of a semiconductor substrate covered by an insulating layer. The semiconductor and insulator can both have nonplanar surface topographies either specified explicitly or input from the TMA process simulation program SUPRA. An optional insulating substrate can be included below the semiconductor to model SOI structures. Multiple electrodes and contacts can cover the device surface, and virtually any impurity distribution can be created through a combination of analytic functions and inputs from TMA's process modeling programs SUPRA and SUPREM-3.</p> <p>CANDE calculates most experimentally measured device characteristics much more quickly and inexpensively than fabrication and device measurement. The user is given total control over all aspects of the device structure without having to worry about process fluctuations. CANDE lets the user observe internal device operation and better understand the mechanisms responsible for device behavior.</p>



**DESIGN AUTOMATION—Design Tools****Design Tool Capability****Miscellaneous Design Tools (Cont'd)**

Technology Modeling Associates GEMINI	Technology Modeling Associates PISCES-2B	Technology Modeling Associates SEDAN-2	Context Context Series
Device Modeling	Device Modeling	Device Modeling	Documentation
<p>Two-dimensional device simulation program. A versatile IC device simulation program, GEMINI models the two-dimensional distributions of potential and carrier concentrations in a device to predict the electrical characteristics. It solves Poisson's equation and is useful for analyzing a wide variety of MOS devices. GEMINI can model a wide variety of device structures composed of a semiconductor substrate covered by an insulator layer. The semiconductor and insulator may both have nonplanar surface topographies and an optional insulating substrate may be included below the semiconductor to model SOI structures. Multiple electrodes and contacts may cover the device surface and virtually any impurity distribution can be created through a combination of analytic functions and inputs from the TMA process simulation programs.</p> <p>GEMINI calculates many device characteristics that can be measured experimentally, but requires much less time and expense than fabricating and measuring the actual device. GEMINI provides the user with total control over all the aspects of the device structure, without the concern that process fluctuations during fabrication will obscure important device effects. But perhaps most importantly, GEMINI allows the user to observe internal device potential, electric field, carrier concentration, and impurity concentration at each node in the simulation structure.</p>	<p>Two-dimensional MOS and bipolar device simulation program. A powerful device simulation program that can be used to develop both MOS and bipolar integrated circuits, PISCES-2B models the two-dimensional distributions of potential and carrier concentrations in a device to predict its electrical characteristics for any bias condition. It solves Poisson's equation for both the electron and hole current-continuity equations to analyze devices such as diodes, bipolar transistors, and effects in which the current flow involves both carriers such as CMOS latch-up. PISCES-2B can also analyze devices in which current flow is dominated by a single carrier such as MOSFETs, JFETs, and MESFETs. In addition, PISCES-2B can be used to study devices under transient operating conditions.</p> <p>PISCES-2B can calculate most experimentally measured device characteristics much more quickly and inexpensively than fabrication and device measurement. In addition, the user is given total control over all aspects of the device structure without having to worry about the process fluctuations during fabrication that can, and often do, obscure important effects. Most important, PISCES-2B lets the user observe internal device operation and, in doing so, more completely understand the mechanisms responsible for device behavior.</p>	<p>One-dimensional device modeling program. SEDAN-2 performs one-dimensional device simulations along user-defined paths through bipolar and MOS device structures. It analyzes the transient and steady-state operation of bipolar devices by solving Poisson's equation and the two current-continuity equations, and analyzes the operation of MOS devices by solving Poisson's equation. Both steady-state bias stepping and transient analysis are available. SEDAN-2 is TMA's proprietary version of the popular SEDAN program. The program has been completely rewritten, and features more flexible input, complete error reporting, and an extensive plotting capability.</p>	<p>Context Corp. will offer its complete line of documentation workstations on the new Apollo DN3000C. The line includes the Context Writer, featuring the documentation editor (DOC), electronic mail and text interface utilities, the Context Editor, which has the capabilities of the Writer plus the Picture Editor (PicED) and graphics utilities, and the Context Documentor, which includes all the features of the Editor plus programming extensions to allow design automation OEMs to directly integrate their databases.</p>

**DESIGN AUTOMATION—Design Tools**

Generic Function

Design Tool Capability

**Miscellaneous Design Tools (Cont'd)**

Source	Cadnetix	Tektronix CAE Systems	Valid Logic Systems Inc.
Tool Name	2D Drafting Editor	TekWriter	ValidFLAT
FOR DETAILED DATA SEE:		page 4658	page 4660
Function	Drafting Editor	Engineering Documentation Package	Flattens Hierarchical Designs
Description	<p>The 2D drafting editor provides general-purpose drafting capability and is included with all Cadnetix color PCB layout workstations. The engineer or designer can now more easily define PC board hardware. Documentation such as assembly and fabrication drawings can be accomplished on the Cadnetix workstations as part of the design process, minimizing turn-around time and reducing opportunity for error. The user definable snap grid and electronic ruler, combined with automatic dimensioning and "leadering" (arrows that point from text to the drawing at 45 degree angles) are features that facilitate documentation.</p> <p>Commonly used shapes are easily created and stored in libraries for future use. Complicated descriptions are possible through advanced features such as block and group operations, "rotate, copy and mirror" functions, automatic filling of polygon areas, and five levels of hierarchy. Before layout, the graphical information can be imported into the workstation's PCB editor to define the area for trace routing. After layout, graphics are again imported for creation of fabrication and assembly drawings.</p>	<p>TekWriter is an engineering documentation package that provides high quality, illustrated documents. TekWriter is based on Workstation Publishing Software (WPS.C) from Interleaf, Inc. an acknowledged technology leader in the design and development of computer aided publishing software.</p> <p>TekWriter merges text and graphics from Tektronix' DDSC system for fast creation and revision of illustrated documents. It is easy to use, and provides "what-you-see-is-what-you-get" capability with team editing flexibility. TekWriter's on-line spelling checker includes a user dictionary update facility. The system has a powerful graphics subsystem and provides camera-ready hardcopy.</p>	<p>ValidFLAT is a flexible software tool developed specifically to transform hierarchical schematics into flat schematics. With ValidFLAT, you can take advantage of the speed and efficiency inherent in hierarchical design techniques, yet document designs in the manner required for production. In the past, documentation requirements for flat, fully annotated drawings prevented many designers from taking advantage of hierarchical design techniques.</p> <p>* Facilitates use of structured design techniques * Converts hierarchical designs into flat designs * Generates schematics matching the physical design * Provides a cross-reference of all signals and parts * Translates designs created on other CAE or CAD systems into a Valid database * Creates schematics intelligently</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Miscellaneous Design Tools (Cont'd)

VIA Systems PG-Tool	Texas Instruments Functional Evaluation Models page 4314	Valid Logic Systems Inc. ValidCONVERT page 4660	MicroSim PSpice Probe
Full Custom PG Fracturing	Functional Evaluation Models	GDSII/Valid IC DesignDatabase Translator	Graphics Post-Processor for PSpice
<p>PG-Tool, a high speed fracturing and design data converter, accelerates the data preparation required for the fabrication of integrated circuits. To accommodate fracturing of design data, PG-Tool accepts any industry-standard design format, fractures the input, and converts the file for all major optical or E-beam pattern generators. Pattern files may also be converted into VIA format, as well as any other industry standard format. PG-Tool is available for the UNIX-based Sun Microsystems products, as well as the Ultrix-based VAXstation II/GPX.</p> <p>Features: industry standard database converters; Boolean logical operators; optical pattern generation; E-beam pattern generation; full database integration; user-friendly operator environment.</p>	<p>These functional evaluation models are written in the C language and are designed to simulate device activity in a computer simulation environment. The models can be used in a standalone mode or as callable functions. Both I/O activity and a number of internal register results can be output to the standard I/O or a file. The device models available are the SN74ACT8837, 64-bit Floating Point Processor and the SN74ACT8836, 32-bit Integer Multiplier.</p>	<p>ValidCONVERT performs two distinct conversion operations. To protect a user's investment in existing GDS-II based designs, ValidCONVERT produces a physical design description compatible with the ValidLED Layout Editor from a GDS-II design. Similarly, for compatibility with external layout plotting devices and systems, ValidCONVERT generates a GDS-II compatible layout description from a design created or modified by ValidLED.</p> <p>To convert from the GDS-II format, ValidCONVERT reads the GDS-II formatted tapes and writes a file compatible with ValidLED to the design database; to convert a design generated by ValidLED, ValidCONVERT writes a GDS-II compatible file to the design database that can be copied to tape and transported to the physical layout system.</p> <p>ValidCONVERT maintains cell definition hierarchy, automatically generates technology and color map files, and allows selective conversion of individual cells within a design.</p>	<p>MicroSim's optional Probe graphics post-processor is an interactive, comprehensive program that gives outstanding visual enhancement to PSpice work. After PSpice is run, Probe allows results of the simulation to be put on the screen in seconds. Besides displaying voltages and currents, you can also display arithmetic expressions involving voltages and currents. Integrals, derivatives, or the instantaneous power at a given node can all be shown on the screen.</p>

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DESIGN AUTOMATION—Design Tools			
Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source Tool Name FOR DETAILED DATA SEE:	DA Systems CIM Software	DA Systems Network Software	Mentor Graphics Test Systems Strategies/Mentor
Function	Interface and Communications	Interface and Communications	Interface and Communications
Description	DA Systems CIM Software, a collection of software packages which use the DA Systems Network, automates the flow and coordination of design data throughout the life cycle of an electronic product from engineering through each revision. The software gives its users the ability to automatically convert design data, transfer it, and coordinate the job flow. It provides a common user interface between the various islands of automation and host computers connected via the DA Systems Network. CIM software provides a framework and the tools with which to implement computer-integrated manufacturing (CIM). Customization will accommodate the currently installed base (turnkey and custom systems, different databases, etc.), the different types of products being designed and manufactured, outside services (e.g. assembly and test), and the company's management style.	The DA Systems Network Software runs on IBM PCs connected to each other via a Local or Wide Area Network. The software enables PCs to interconnect computer-aided equipment, computers and their networks. The software is designed for the development of networked applications and networked process-to-process communications.	Test Systems Strategies Inc. (TSSI) is providing its Test Development Series (TDS) software for the Mentor Graphics IDEA Series of Engineering Workstations. The TDS software takes information directly from the Mentor Graphics Idea Station simulation data file and optimizes it for use in production testing through the automatic synthesis of an executable test program.  Combining the Test Development Series software with the Mentor Graphics Idea Station provides users with a range of capabilities which effectively integrates design activities with test requirements. The TDS software allows Mentor Graphics users to generate functional, executable test programs for new devices and systems. The TDS software system includes modules to support all major testers in a variety of automated test equipment configurations.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Miscellaneous Design Tools (Cont'd)

Silvar-Lisco IZYCAD	Silvar-Lisco Test Systems Strategies/S-L	Kontron Laser Film Plotter	Analog Design Tools Basic Device Library
Interface and Communications	Interface and Communications	Laser Film Plotting	Library Addition
<p>The IZYCAD interface enables users of Silvar-Lisco's SDS Schematic Design System, HELIX Behavioral Simulator and LOGIX Logic Simulator to use Zycad Accelerators. The availability of the IZYCAD interface dramatically reduces simulation time for complex electronic designs. IZYCAD automatically transfers schematic designs captured by SDS and simulated by its HELIX or LOGIX-SL. The schematic information is used as netlist and control command input for Zycad's accelerators. After acceleration on the Zycad system, simulation results are displayed by Silvar-Lisco's waveform analyzer, LOGAN.</p> <p>The Zycad products include logic and fault simulation engines that enable simulation at speeds over 1000 times faster than software-based simulators operating on mainframe computers.</p>	<p>An interface from Silvar-Lisco links the Test Development Series from Test Systems Strategies to Silvar-Lisco design tools. Silvar-Lisco's ITSSI interface enables design engineers to generate functional, executable test programs for new devices and systems. The package supports popular testers. The ITS-SI interface allows users of Silvar-Lisco's behavioral and logic simulation products, HELIX and LOGIX-SL to drive hardware testers. Simulation results from Silvar-Lisco's HELIX behavioral simulation software is converted into an ASCII data file that is subsequently formatted into appropriate tester language, including the ability to perform data compression and correct clock cycle assignments.</p>	<p>A direct laser film plot device output is provided to generate raster bit-maps from the KAD layout database to the Linotronic-300 or Linotronic-500 laser film plotter. This direct interface provides high speed plot capabilities (typically 3 minutes for a VME board file) for the Kontron KAD System. Daylight operation and cassettes for 100 feet of film permit batch operation of arbitrary length (30 or 50 cm film width) with 4, 8 or 16 mil selectable resolution. The system can process large databases and can therefore handle very complex designs.</p>	<p>The Analog Workbench, the CAE system made specifically for the design of analog circuits, now has unbundled its General Device Library to meet the needs of designers. A new Basic Device Library, consisting of 50 discrete and IC devices in 14 different categories, is now available for users of either the Analog Workbench or the PC Workbench. The devices in this module were carefully selected to include a cross section of the most commonly used semiconductors in the industry. In addition the user can add or modify symbols with the new Symbol Editor or he can add or modify device parameters with the Parameter Entry and Subcircuit function, both of which are now basic on both versions of Analog's CAE system. The Analog Workbench runs on workstations from Apollo, Hewlett-Packard and Sun Microsystems. The PC Workbench offers the same features at a lower cost.</p>

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## DESIGN AUTOMATION—Design Tools

Generic Function

Design Tool Capability

## Miscellaneous Design Tools (Cont'd)

Source	Valid Logic Systems Inc.	Micro Linear	Aldec
Tool Name	ValidEZLIB	FB300 Linear Array Layout	FAST
FOR DETAILED DATA SEE:	page 4660		
Function	Library Development Tool	Linear Array Layout	Logic Analyzer to Logic Simulator Link
Description	<p>ValidEZLIB is a sophisticated library development tool that eliminates the need to manually calculate delay information and provides a fast and easy method to enter timing information for both timing verification and simulation.</p> <p>ValidEZLIB utilizes the familiar datasheet format. With ValidEZLIB, you can change timing specifications from one family to another family without having to redo the model.</p> <p>* Provides user friendly interface for creation or modification of library components * Automatically calculates timing delays and distributes to model * Automatically creates a timing specification template file from existing models * Simplifies creation of new models * Completely integrates with existing Valid library development tools</p>	<p>Micro Linear provides a tape of layout templates for its FB300 Linear Bipolar Array series. This tape contains the manual layout information for the chips. Metal tabs are shown for each discrete device, with special color-keyed identifiers to indicate the device type. Layout does not require knowledge of chip design. Menus are provided that simplify the layout procedure by predefining the interconnect layers and line widths. Placement of the Macro Cells is easily performed by selecting a Macro from the menu, and placing it in the desired position. A DRC error-free layout can be achieved by following layout guidelines and menu selections. This tool is available on the Daisy Chipmaster, Calma GD-SII, Mentor, and Applicon workstations and will route on up to two layers.</p>	<p>Fully Automated Simulation and Troubleshooting (FAST) provides for automatic fault location using any logic analyzer and standard IBM PC or compatible. FAST software feeds into the schematic the same signals that were fed into corresponding points on the P.C. board under test. If the schematic's response to these input signals is different from the hardware (logic analyzer) outputs, then there is a hardware fault. FAST simulates the suspected board fault by forcing certain schematic test points to either logic 'high' or 'low' (grounding them). If the pre-conditioned schematic generates identical outputs as the logic analyzer, it means that the board under test is failing in the schematic simulation. Required: standard IBM PC w/color/graphics adapter, 512 kBytes of RAM, logic analyzer w/RS-232C or IEEE-488 interface.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Miscellaneous Design Tools (Cont'd)

Aida	Harris Semiconductor	Valid Logic Systems Inc.	Valid Logic Systems Inc.
Aida Logic Design Rules Check	Logic Compiler	ValidCOMPILER	ValidPACKAGER
	page 4246	page 4660	page 4660
Logic Design Rules Checker	Logic Minimization/ Circuit Optimization	Logical Compiler	Logical-to-Physical Database Translator
<p>The Aida Logic Design Rules Checker (LDRC) is a rules-driven, knowledge-based, artificial-intelligence system. Using the LDRC, engineering teams can produce a customized rules set to automatically check whether a design conforms to the chosen design methodology, electrical rules, technology constraints, and even parts preferences. Specific design rules or idiosyncrasies of different design methodologies can be automatically checked without having a designer manually track and verify each occurrence.</p>	<p>Logic Compiler from Optimal Solutions Incorporated allows a designer to describe a circuit functionality with netlists, PLAs, or Boolean functions. Logic minimization is performed through algorithmic Boolean algebraic reductions. Circuit optimization is performed using technology libraries to reduce circuit size and delay.</p> <p>Using Logic Compiler will yield: faster designs, functional correctness, better circuits, greater control of design requirements, and technology transfer.</p>	<p>This logic compiler builds the logical database used by other Valid-TOOLS. It features incremental (only what has been changed) compilation for quick revision turnaround. ValidCOMPILER expands hierarchical designs, checks design interfaces, and incorporates library descriptions of parts into the design database. Input is accepted from ValidGED.</p>	<p>The ValidPACKAGER is an easy-to-use physical design and analysis tool that lets you convert a logical design created using the ValidGED graphics editor, into a packaged design suitable for physical layout. ValidPACKAGER bridges the gap between logical schematics and printed circuit board (PCB) layouts and additionally helps ensure that your drawing is design rule correct. * Assigns reference designators and pin numbers * Performs design rule checking * Prepares data for backannotation of schematic * Simplifies Engineering Change Orders * Produces cross-reference lists and netlists * Supports parameterization of parts</p>

DESIGN AUTOMATION—Design Tools			
Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source	Cadnetix	EEsof	Texas Instruments
Tool Name	CDX 60000S	MICmask	Memory Management Design Kit
FOR DETAILED DATA SEE:			page 4314
Function	Manufacturing Workstation	Mask Generation Software- RF/Microwave	Memory Management Circuit Design
Description	<p>The Manufacturing Workstation (MWS) addresses the complete requirements of printed circuit board manufacturers. It includes the Cadnetix Panel Editor, powerful postprocessing capabilities and a Database Query Language (DQL) facility. The MWS database accepts PCB design input from a variety of sources.</p> <p>The Panel editor allows the systems user to construct a multiple image tooling area, or panel, for the manufacture and assembly of one or more instances of a PCB design (or designs). With the editor, the user can actually change the board artwork to improve manufacturability.</p> <p>DQL permits the user to directly select and tailor data in a panelized format for manufacturing and test equipment: photoplotters, NC drillers, profile routers, autoinsertion tools, pick and place tools, punch and reinsert tools, board handlers, axial sequencers, and board testers.</p>	<p>Post-processing software for production of camera-ready artwork on: Aristomat 100, Gerber photoplotter, Hewlett-Packard 7270/7475/7550 desktop plotters, Aviotab TA2, Calma GDS II. Used with EEsof's MiCAD on a PC, the MICmask post-processor programs offer complete control over the layout process and artwork production. MICmask also provides MICKnife, a diamond stylus, which replaces a pen in the HP desktop and drafting plotters and enables rubylith cutting at the designer's desktop. MICmask for HP plotters is included with MiCAD.</p>	<p>Texas Instruments Memory Management Design Kit is offered to provide the user with a complete package of information and tools for design of any memory management system. The kit contains data, applications information, device samples, graphics symbols compatible with the Mentor and FutureNet CAE systems, and information about behavioral circuit simulation models from Logic Automation. The range of memory management applications products offered in this package includes cache Address Comparators, DRAM Controllers, Error Detection and Correction (EDAC) devices, Programmable Logic for timing and control functions, Memory products, and Memory Drivers.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Miscellaneous Design Tools (Cont'd)

Trimeter Technologies Microcode Assistant	EEsof Filter Design Programs	MicroSim PSpice Monte Carlo Analysis	HHB Systems LANA CADAT
Microcode Creation and Verification	Microwave Filter Design	Monte Carlo Analysis of PSpice	Parallel Processing for Fault Simulation
<p>Trimeter's Microcode Assistant allows you to graphically create and verify microcode. By using interactive graphics for microcoding, you can eliminate many of the problems and frustrations that make microcoding one of the most difficult, burn-out prone and highly turned-over tasks in the industry.</p> <p>The Microcode Assistant has four integrated environments: 1) the Microword Format Editor which allows you to graphically define microword formats; 2) the Microprogram Editor which allows you to graphically or textually produce code for any architecture; 3) the Verification Environment which allows you to graphically verify the microprogram with a register transfer level behavioral hardware simulation model; and 4) the Logical/Physical Format Editor which allows you to work in formats that you are comfortable with, not with the format required by the hardware.</p> <p>With the Microcode Assistant, you can graphically create microcode in a comfortable, productive environment. And you can SEE your microcode working even before the hardware exists.</p>	<p>From Wenzel/Erlinger Associates, a series of microwave filter design programs which enable practical designs for a wide variety of filters, both wideband and narrow band. Verified for designs at frequencies through Ku-band. The first four programs are available in 1986: Filter I (ECS), for designing edge-coupled stripline bandpass filters with exact equal ripple response; Filter II (ECM), for edge-coupled microstrip bandpass filters with exact equal ripple response; Filter III, for combine filters; Filter IV, for interdigital filters. Future programs include microstrip lowpass, coaxial lowpass, microstrip bandpass, waveguide bandpass, and others.</p>	<p>The Statistical (Monte Carlo) Analysis option allows the assignment of tolerances to component values which are then used to make multiple runs of an analysis with variations of those values. For each run, the actual component values used can be printed and the analysis output (e.g. a transient waveform) can be printed or plotted. All of the PSpice analysis, including: DC, AC and transient analysis, can be used with the Statistical Analysis option.</p>	<p>HHB Systems is complementing its hardware simulation acceleration engine (point accelerators) platforms with LANA CADAT which provides increased simulation throughput by distributing fault simulation across parallel processors in a networked computer/workstation environment. HHB Systems' LANA CADAT runs on Apollo and Sun networks.</p>

## DESIGN AUTOMATION—Design Tools

Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source	Electrical Engr'ng Software	GT Systems	GT Systems
Tool Name	DEVICELIB	AutoNET	AutoTRACE
FOR DETAILED DATA SEE:			
Function	Parts Model Library	PCB Enhancement to AutoCAD	PCB Enhancement to AutoCAD
Description	DEVICELIB is a collection of transistors, diodes, and opamps that can be used in PRECISE to model the electrical characteristics of standard parts.	<p>AutoNET is an enhancement to AutoCAD for printed circuit board design. Autonet reduces the time consuming task of capturing a schematic digram and ultimately translating it into an accurate printed circuit layout. AutoNET provides a set of symbols and specific line conventions which enable the graphic drawing of schematics with embedded attributes, thus allowing the extraction of parts lists and interconnection data. This data is output in a number of formats as selected by the designer. Generally, output is either printed in a page format for "human" use or as an ASCII file for transfer into an automatic separate printed circuit layout routine. Errors in the form of cross connections between nets are reported and the X,Y coordinates of each symbol and line in the schematic are reported.</p> <p>The Net List is available in three forms: The first is listed by the component reference DESIGNATOR and shows each pin of the component and the netname and/or number connected to those pins. The second form of output is listed by NETNAME. Under each name is a listing of its connections by component reference designator and pin number. The third is an SDF format ASCII disk file sorted by NETNAME. This file is used to drive other programs such as a rat's nest generator, auto-router or wire-wrap system.</p>	AutoTRACE is an interactive printed circuit board layout and design system engineered to be used with AutoCAD. The system takes advantage of the extremely fast and flexible line editing routines incorporated in AutoCAD by allowing the user to design a board using simple outlines for pads and lines for traces. Just prior to plotting, AutoTRACE processes the drawing data file to convert all of the lines to traces of a specified width and all of the pads to graphically correct designs suitable for final artwork. System speed is greatly enhanced by eliminating the repeated regeneration of solid pads and traces. Trace width of finished layout may be changed with a single specification.



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Miscellaneous Design Tools (Cont'd)

GT Systems TRANSPAD	Valid Logic Systems Inc. TIMEMILL page 4660	LPKF Pacific LPKF-Color CAM	ProtoCAD CAD/Magic 3500
PCB Enhancement to AutoCAD	Post IC Layout Switch Level Timing Anal	Printed Circuit Board Prototyping System	Printed Circuit Board Prototyping System
TRANSPAD links smARTWORK by Wintek with AutoCAD to create a complete interactive printed circuit board design package. The smARTWORK program is a very efficient tool for development of single-sided, double-sided, and multilayer circuit board artwork. Within the limitations of 50 mil grid and 10" x 16" maximum finished board size, smARTWORK is a very efficient means of preparing an artwork master using the IBM PC. Once the artwork has been prepared, TRANSPAD extracts the traces and pad locations from the smARTWORK plot file and creates an AutoCAD .DXF file. If the smARTWORK Padmaster plot is used, TRANSPAD runs about 3X faster. AutoCAD, with the TRANSPAD screen menu and symbols, is then used to create the component, assembly, board outline and screening drawings based on the extracted .DXF file. Thus the combination of AutoCAD, TRANSPAD, and smARTWORK form a complete, effective and economical PC design and documentation system for the IBM PC engineering work station.	TIMEMILL is a mixed-level timing simulator and critical path analyzer that can handle designs at the behavioral, gate, and transistor switch levels. TIMEMILL's delay calculation, based on post-layout extracted data, is highly accurate, and its analysis speed is more than ten thousand times faster than SPICE. The mixed-level capability supports a hierarchical design methodology, like Valid's pioneering SCALD methodology, in which components with different levels of abstraction can be mixed to achieve high simulation and verification efficiencies. TIMEMILL also includes a sophisticated critical path analyzer which performs pattern-independent static path analysis.  TIMEMILL will run on all Valid-supported IC design platforms: Sun, Digital, and Valid's own SCALDsystem. By using it with Valid's other proven design tools, users will be able to get the highest possible performance from their designs.	The LPKF-COLOR CAM is a complete interactive CAD/CAM system for the design and instant manufacture of milled printed circuit boards. It is intended to be used both as a development tool and as a stand-alone fabrication system. As a development tool it offers a fast and economical means of laying out, creating, testing and editing prototype circuit boards. COLOR-CAM can be interfaced to all other Gerber-formatted systems. It can be used to design in all techniques including conventional, consequent groundplane and surface mount. Minimum line width is 2 mils. Either single or double sided boards can be manufactured, in any size up to 16.5 X 15 inches.	The CAD/MAGIC 3500 produces double sided printed circuit boards with plated through holes directly from a PCB CAD database. This system offers a rapid, inexpensive, and highly convenient alternative to conventional prototyping methods.  The CAD/Magic 3500 system consists of three modules, each with a 40 x 28 inch footprint, providing the functions of drilling, plotting, etching and plating. These units are self contained, environmentally safe, require no special facility fit-up, are transportable and suitable for use within a design lab.  The system features menu driven software, microprocessor controls, automatic tool change, single bath copper plating, peroxide/sulfuric etching, and interfaces with PCB CAD databases using Gerber photoplotter format. Minimum board size is .5 x .5 inches. Maximum board size is 10 x 16.5 inches. Minimum trace width is .008 inches. Drill sizes range from .020 to .062 inches.

**DESIGN AUTOMATION—Design Tools**

Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source	Technology Modeling Associates	Technology Modeling Associates	SDA Systems
Tool Name	SUPRA	DEPICT-1	SKILL
FOR DETAILED DATA SEE:			
Function	Process Modeling	Process Simulation Program	Program Development Environment
Description	<p>Two-dimensional process modeling. A powerful IC process simulation program that simulates complete fabrication processes for nonplanar MOS and bipolar devices, SUPRA models the two dimensional changes in impurity distributions occurring in a device during processing to predict the final device structure. The combination of analytic and numerical solution techniques makes it an uncommonly efficient engineering tool. SUPRA can model a wide variety of device structures composed of as many as eight implantation masking layers in addition to the silicon substrate and thermally grown oxide. The implant masking layers may each consist of any of the five materials: polysilicon, silicon dioxide, silicon nitride, aluminum, or photoresist. Four impurities: boron, phosphorous, arsenic and antimony- may be implanted, diffused, or included in deposited layers to develop the simulated structure.</p> <p>TMA's proprietary version of SUPRA has major enhancements resulting from years of industrial feedback and continuing development by TMA's process engineers. These enhancements include: more accurate process models and two-dimensional modeling algorithms, additional informative output, and new features that add to its flexibility and ease of use.</p>	<p>A powerful new program that simulates the topographical evolution of a device during processing, DEPICT-1 simulates the critical photolithography and deposition steps required to fabricate ICs. The program was developed by TMA's staff of engineers and physicists to satisfy the IC industry's need for a flexible, easy to use topography simulator. DEPICT-1 can simulate the fabrication of a wide variety of device structures composed of up to 10 separate arbitrarily shaped layers. Each layer may consist of any of 40 different materials, including single crystal silicon, silicon dioxide, polycrystalline silicon, silicon nitride, aluminum, gallium arsenide, sapphire, and many commonly used photoresists.</p> <p>A device structure may be formed by depositing new layers of materials, etching existing layers, and by photolithographically exposing and developing photoresist layers. Alternatively, a structure formed with TMA's SUPRA program may be input as a starting point for the DEPICT-1 simulation through TMA's proprietary interprogram file interface.</p> <p>Physical (PVD) and Chemical Vapor Deposition (CVD) processes are simulated through models which account for the vapor transport and adsorption of material at the structure surface. Deposition rates are specified directly, avoiding the need for complex physical-chemical reaction models. Photolithographic imaging and exposure is simulated for projection steppers with multiple illumination wavelengths, defocus and any degree of coherence. During exposure simulation, DEPICT-1 models the destruction of the photoactive component (PAC) in one or more photoresist layers present in the structure. Development is treated as a surface controlled etching reaction with the etch rate dependent upon the remaining PAC concentration.</p>	<p>The SKILL language provides access to SDA's Human Interface, database, and tools. Using SKILL it is possible to tailor the system, add new tools, or create new functionality. SKILL is based on the LISP language but uses a more conventional syntax. The SKILL development environment is integrated into the Design Framework so applications can quickly be developed from within the system.</p>



DESIGN AUTOMATION—Design Tools

Design Tool Capability

Miscellaneous Design Tools (Cont'd)

Texas Instruments Microcode C-Compiler  page 4314	Teradyne Circuit Breaker	Analog Design Tools Smoke Alarm Module	SDA Systems STL
Program Development Tools, Retargetable	Programmable Logic Device ATPG	Safe Operating Conditions Analysis	Simulation and Test Language
<p>These program development tools are designed for retargetable Single Instruction Multiple Data (SIMD) Non-Von Neuman architectures and allow the user to reconfigure his program development tools with a minimum of time and effort. The tools included in this package are an Architecture Description Language Compiler, Machine Architecture Description Compiler, Retargetable C-language Compiler, Fortran Compiler, Macro Assembler, Linker, and Load Module Converter. TI's 8-bit Slice family and 32-bit Building Block products are supported and Module Definition Files for these devices are provided with the programs.</p>	<p>Circuit Breaker is a new option available with Teradyne's LASAR Version 6 simulation system. The LASAR/Circuit Breaker combination is claimed as the first automatic test generation solution for programmable logic devices (PLDs) which is capable of creating dynamic as well as static tests, and of handling highly sequential PLDs as well as simpler combinatorial parts. Aimed at high-volume incoming inspection operations and in-circuit board test applications, Circuit Breaker provides static tests with 95% or better fault coverage, and grades dynamic tests' coverage of various slow path faults in the PLD.</p>	<p>The Smoke Alarm module automatically evaluates the operating conditions of all circuit elements, including passive components, semiconductor devices and power supplies. It warns the designer if any components are outside their safe operating areas. After constructing a circuit on either the Analog Workbench or PC Workbench, the designer simulates and modifies it for the desired functionality. He then runs the Smoke Alarm module to check each component against its maximum (or derated) operating conditions. If these conditions are exceeded, a "smoke" icon is displayed beside the guilty component on the circuit schematic. The user also is allowed to derate operating condition values below their maximum data-book levels.</p>	<p>STL-- SDA's high-level programming language for developing simulation-input and production-test programs-- provides a common meeting ground for the chip designer and test engineer. STL (for Simulation and Test Language) offers designers the tools to specify stimulation stimuli and expected responses; test engineers can write additional functional test vectors. A single STL source program can then be compiled by various code-generation modules into output for many simulators and testers. Code generators supported now include SILOS and HILO-3 logic simulators, the SPICE circuit simulator, and the SENTRY and GenRad VLSI testers.</p>

Bold face indicates data is provided in the page noted

DESIGN AUTOMATION—Design Tools			
Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source Tool Name FOR DETAILED DATA SEE:	Logic Automation SmartModels	Quadtree Designers' Choice	MicroSim PSpice Device Equations
Function	Software Models	Software Models	Source Code (Partial) to PSpice
Description	<p>SmartModels are behavioral level models of commercially available ICs which run on popular logic simulators and CAE workstations. They provide the symbols, logic and timing information needed to perform complete logic simulation analysis of PCB and systems level designs. Models for hundreds of parts are available, ranging from 32-bit building blocks and microprocessors, to memories, PALs, and complex TTL.</p> <p>SmartModels increase designer productivity through knowledge based system analysis. The models incorporate capabilities that pinpoint design errors. During simulation, the models analyze all transitions and states, identifying such problems as incorrect protocols, timing errors, illegal chip useage, and initialization errors. Error messages give the exact location, time, and nature of the problem. Checks for all error conditions, as identified by the IC manufacturer's data books, are included.</p> <p>SmartModels make board level simulation a reality, allowing substantial cost and design time reductions.</p>	<p>Quadtree is a developer of full-function microprocessor and peripheral device simulation models for use along with a number of currently popular logic simulators including the ubiquitous CADAT simulator. Simulation models are a new area in the CAE environment and represent a significant advance in the state-of-the-art in electronic design automation. Current Behavioral models include libraries from: Motorola, Intel, AMD, T.I., IDT, Weitek, and MMI. The microprocessor models have an optional built-in graphic microprocessor development environment similiar to an in-circuit emulator for combined hardware and software development. IEEE/ANSI STD-91 symbol library is used. Unknown state, X, handling is supported and timing and functionality problems are reported including those caused by transients. Logic simulators supported include: FutureNet, HHB Systems, Mentor Graphics, Silvar-Lisco, Valid and LSI Logic.</p> <p>In addition to full-function models, Quadtree offers Express Models, available for fast delivery and providing the ability to verify designs before system software is available, and a set of Express Model Generator Tools, to enable end-users to build their own models.</p>	<p>The Device Equations option is the partial source code to the PSpice program. It allows modification of the equations that interpret the device parameters. This option is not required to simply alter device parameters. Modifying those may be done easily and simply just by changing the input circuit file with a text editor. The Device Equations option requires a good understanding of the C programming language and the internals of SPICE.</p>



DESIGN AUTOMATION—Design Tools			
Design Tool Capability			
Miscellaneous Design Tools (Cont'd)			
Endot N.2	SDA Systems SCOAP	Valid Logic Systems Inc. Thermal & Reliability Analysis page 4660	Cadam Thermal Analysis (Thermax)
Systems Level Design	Testability Analyzer	Thermal & Reliability Analysis	Thermal Analysis
N.2 is a system level CAD environment that assists the designer during the crativity-intensive levels of design and analysis. N.2 supports hierarchical specification, design, and functional simulation of complex digital systems including VLSI chips, PC boards and systems. The N.2 system contains a powerful, interactive simulator with extensive debugging facilities and an integrated microcode and macrocode development facility. N.2 supports modeling of systems that contain a high degree of inherent concurrency between processors, within processors, and within processes.	SCOAP, a well-known testability analysis program developed by the Sandia National Laboratories, is now also accessible through SDA's easy-to-learn-and-use graphical interface. This means that designers who have used SDA's other design-automation products will be working in a familiar environment. SCOAP handles both sequential and combinational circuits, and considers only circuit topology in its analysis. SCOAP's graphical interface highlights difficult-to-test nodes on the schematic diagram, thus letting the designer identify early in the design process the nodes with the poorest testability numbers. This visual feedback greatly increases productivity and speeds up the design-analysis cycle.	Valid's Thermal and Reliability Analysis software is an operation under the Allegro PCB Design System. This software performs a finite difference analysis to calculate the thermal behavior of PC boards under alternate operating environments specified by the user. Four different heat transfer mechanisms are modeled: natural and forced convction, conduction, and radiation.  Reliability analysis based on the MIL HDBK417D standards are also calculated ona component-by-component basis, with absolute and relative failure rates displayed graphically.  Additionally, noise margin analyses are conducted to pinpoint areas where thermal shifts between pin pairs may violate noise thresholds.	Thermal Analysis provides for computerized evaluation of thermal properties associated with the design of printed circuit boards. The package expands upon the foundation of Interactive PRANCE Cadam (IPC), used for printed circuit board design. Once IPC has completed placement, Thermal Analysis quantifies related heat dissipation characteristics. Four basic cooling techniques are considered automatically: radiation, air flow on components, air flow in hollow card, and heat exchanges. Any combination of these techniques may be used. The results of the analysis are then displayed graphically in the form of temperature gradients for each individual component, as well as for the entire board within its operating environment.

DESIGN AUTOMATION—Design Tools			
Generic Function		Design Tool Capability	
Miscellaneous Design Tools (Cont'd)			
Source	Scientific Calculations	Control Data	Aida
Tool Name	SCITHERM	MIDAS	Aida Timing Verifier
FOR DETAILED DATA SEE:			
Function	Thermal Analyzer	Timing Analyzer	Timing Analyzer for well clocked designs
Description	The SCITHERM program is a heat transfer CAD system that enables designers of electronic equipment to analyze problems of space versus heat buildup at every stage of the design and production process. SCITHERM runs on the IBM PC XT/AT and DEC VAX.	Modular Integrated Design Automation System provides path trace and logic timing analysis for long and short paths. MIDAS provides worst-case timing and hierarchy timing analysis and automatically generates test operands. Maximum gates: 200,000. Performance: 40 + (.01 x gates) = CP seconds.	The Aida Timing Verifier analyzes timing for multi-ASIC and multi-board designs. It evaluates all paths in a design to determine critical paths and displays the user-selected number of worst-case paths.  The Aida Timing Verifier provides fast, accurate digital timing analysis to designers of large ASICs and multi-board, multi-chip systems. Operating independently of input stimulus, it analyzes all possible paths in a design for timing violations. It calculates delays using Aida's sophisticated timing equations, which incorporate input rise time, output loading, and cell delays. And it computes clock skews to accurately report set-up and hold time violations without creating numerous false reports.

DESIGN AUTOMATION



DESIGN AUTOMATION—Design Tools

Design Tool Capability			
Miscellaneous Design Tools (Cont'd)			
EEsof LINECALC	Quantic Laboratories GREENFIELD 2	Datacon DataPlace	Standard Microsystems Corp. STANWIRE page 4310
Transmission Line Analysis	Transmission Line PC Board Simulation	Wire Wrap Panel Device Placement	Wirewrap Board Emulator
<p>A transmission line analysis and synthesis program for automatic calculation of transmission line electrical parameters (from physical parameters) and physical parameters (from electrical parameters). Includes all TOUCHSTONE transmission line models based on physical parameters. Appropriate for designers of UHF, VHF, microwave, and millimeter wave circuits requiring numerous transmission line calculations. Applications include single and coupled transmission lines in microstrip and stripline, plus single lines in coplanar waveguide, and grounded CPW.</p>	<p>At high speeds, impedance mismatch at connectors and components causes reflections, ringing and signal distortion. GREENFIELD is a graphics-oriented and menu-driven family of CAE/CAD software tools for simulation of complex systems of cables and coupled multi-conductor lines on printed circuit boards. Senior family members are GREENFIELD2: a field solver and PHYLLIS, a physical load and line simulator. GREENFIELD2 is a high-order boundary element method code for the determination of self and mutual inductances and capacitances of cables and systems of PC traces with accuracy, convenience and speed. Per unit length line impedances, time delays, inductance, and capacitance matrices are produced.</p> <p>PHYLLIS is a time-domain transmission-line network simulator for arbitrarily interconnected and loaded cables and circuit board transmission lines stored in files produced by GREENFIELD2. The user may prescribe excitation signals of arbitrary shape and apply them to the network. Ringing and cross-talk waveforms are displayed in the time domain as they would be seen on a scope during a laboratory test.</p> <p>With the GREENFIELD system the effects of dielectric changes, reconfiguring line spacings and lengths, and varying load conditions may be seen, sensitivity and cross-talk studies are easily performed.</p>	<p>This software package allows a circuit designer to place devices on a screen image of a wire wrap board. A device list, with pin information, is then generated. This list is provided to dataCon with the netlist, for a quick turnaround prototype. Runs on IBM-PC/XT/AT, and requires only graphics capability (no CAE required).</p>	<p>Produces a wirewrap breadboard of CMOS discrete parts from the logic netlist of any circuit designed using the 74LS family of customization cells.</p>

DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→) (←)		Function	Name	Source	Comments
Design Tool Interfaces							
(Industry standard)							
ASCII	ASCII Output	X	X	Intermediate format	PDIF	P-CAD	
CIF	Caltech Int Format	X	X	Full custom layout	GDS I	Calma	Via Octal Inc. interface
		X	X	Full custom layout	GDS II	Calma	Via Octal Inc. interface
		X	X	Graphic database	SDL	Silvar-Lisco	
		X	X	PCB layout	APLE860	Applicon	Via Octal Inc. interface
		X	X	Silicon compiler	C4 Compiler	Seattle Silicon	
		X	X	Silicon compiler	C5 Compiler	Seattle Silicon	
		X	X	Silicon compiler	Genesis & Genesil	Silicon Compilers	
		X	X	Silicon compiler	Compile	Unicorn	
		X	X	Graphic database	SDL	Silvar-Lisco	
		X	X	Logic sim. accel.	MX/MXT/HSE	XCAT	
EDIF	Intermediate format	X	X	Schematic capture	SCHEMA	Omaton	
		X	X	Silicon compiler	Genesil	Silicon Compilers	
JEDEC	PLA fuse map	X		Logic simulator	LIBSIM	ACASI	
				Logic simulator	LIBSIM	ACASI	
SPICE	Circuit simulator		X	Database	SCALD	Valid Logic	
			X	Database	SCALD	Valid Logic Systems	
			X	Design database	CIEDS	IBM	
			X	Design database	IDEA System	Mentor Graphics	To Version 2G.6
			X	Graphic database	SDL	Silvar-Lisco	
			X	Parameter extraction	TOPEX	Tech Modeling Assoc	
			X	Schematic capture	Hierarch Schem Edit	Cadnetix	
			X	Schematic capture	CT-1000	Case Technology	Via Torric Inc. FREND
			X	Schematic capture	ED-Schematics	Control Data	
			X	Schematic capture	DASH	FutureNet	Via Torric Inc. FREND
			X	Schematic capture	NETED	Mentor Graphics	Via SPICENET
			X	Schematic capture	Grate/Lognet	NCA	
			X	Schematic capture	SCHEMA	Omaton	
			X	Schematic capture	NX-SPICE	P-CAD	
			X	Schematic capture	PC-CAPS	P-CAD	Via Torric Inc. FREND
			X	Schematic capture	Visula CAE	Racal-Redac	
			X	Schematic capture	Visula CAE	Racal-Redac	
			X	Schematic capture	DDSC	Tektronix/CAE	
			X	Schematic capture	Schematic Entry	Versatec	
			X	Schematic capture	Expert Schematics	XEROX	
			X	Silicon compiler	C4 Compiler	Seattle Silicon	
			X	Silicon compiler	C5 Compiler	Seattle Silicon	
	X	Silicon compiler	Genesis	Silicon Compilers			
Academi							
PCB Layout	PCB layout	X	X	Database	SCALD	Valid Logic Systems	
		X	X	Schematic capture	Vanguard Stellar	Case Technology	Netlist, back annotation
ACASI							
LIBSIM	Logic simulator	X	X	Logic sim. accel.	Logic Evaluator	Zycad	
		X	X	Logic simulator	LIBSIM	ACASI	
		X	X	Logic simulator	HILO	Genrad	Data migrate (PC to Mainframe)
		X	X	Logic simulator	CADAT	HHB Systems	
		X	X	Logic simulator	SILOS	Simucad	
		X	X	PLD development sys.	A + Plus	Altera	
		X	X	PLD development sys.	ABEL	Data I/O	Simulates PLDs/fuse map
		X	X	PLD development sys.	ABEL	Data I/O	
		X	X	PLD development sys.	PALASM	MMI	
		X	X	PLD development sys.	CUPL	P-CAD	
		X	X	PLD fuse map	JEDEC	(Industry standard)	
		X	X	PLD fuse map	Signetics prog table	Signetics	
		X	X	Schematic capture	CT-1000	Case Technology	
		X	X	Schematic capture	Ed-Schematics	Control Data	
		X	X	Schematic capture	DASH	FutureNet	
		X	X	Schematic capture	DASH	FutureNet	
		X	X	Schematic capture	NETED	Mentor Graphics	Direct interface/no translate
		X	X	Schematic capture	SCHEMA	Omaton	
		X	X	Schematic capture	Redlog	Racal-Redac	
LIBTEST	Test prgm edit/gener	X		ATE	Sentry	Fairchild	
		X		ATE	(various)	Genrad	
		X		ATE	(various)	Teradyne	
		X	X	Logic simulator	LIBSIM	ACASI	
Aida							
Aida ATPG	Auto test pattern	X	X	Design database	TDL	Calma	
	Auto test Pattern	X	X	Logic simulator	Proprietary sys	ICS	Scan designs
	Auto test pattern	X	X	Logic simulator	LDS	LSI Logic	Scan designs
		X	X	Logic simulator	Proprietary System	Toshiba	Scan designs
		X	X	Netlist	Netlist	Any	Scan design
		X	X	Schematic capture	NETED	Mentor Graphics	
Aida Fault Simulator	Fault simulator	X	X	Netlist	Netlist	Any	
		X	X	PCB layout	Crystal Router	Shared Resources	
Aida FaultInferencer	Test grading		X	Netlist	Netlist	Any	Scan design
Aida Logic DRC	LDRC		X	Netlist	Netlist	Any	
Aida Logic Simulator	Logic simulator		X	Netlist	Netlist	Any	
Aida Timing Verifier	Timing verifier		X	Netlist	Netlist	Any	
AIDA							
Fault Simulator	Fault simulator	X	X	Design database	TDL	Calma	
		X	X	Schematic capture	NETED	Mentor Graphics	
LDRC	Logic design rule ck	X	X	Design database	TDL	Calma	
		X	X	Schematic capture	NETED	Mentor Graphics	
Logic Simulator	Logic simulator	X	X	Design database	TDL	Calma	
		X	X	Schematic capture	Vanguard Stellar	Case Technology	Netlist
		X	X	Schematic capture	NETED	Mentor Graphics	
Tim Ver	Timing analysis	X	X	Design database	TDL	Calma	
		X	X	Schematic capture	NETED	Mentor Graphics	
Algorex							
PCB Layout	PCB layout	X		PCB layout	Koloa PCB	Shared Resources	



DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→)   (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Algorex (Cont'd) PCB Layout	PCB layout	X		PCB layout	Crystal Router	Shared Resources	
Altera A + PLUS	PLD development sys	X		Logic simulator	LIBSIM	ACASI	
PLDSMOD1	PLD development sys		X	Logic simulator	PC-LOGS	P.CAD	12-state simulator
PLE2	PLD development sys		X	Schematic capture	DASH	FutureNet	
			X	Schematic capture	PC-CAPS	P-CAD	
Analog Design Tools Analog Workbench	Circuit simulator		X	Schematic capture	Expert Schematics	XEROX	
			X	Simulation models	Lin Cad II	Micro Linear	
Applicon A6S870	PCB layout	X		PCB layout	GDS II	Calma	Via Octal Inc. interface
APLE860	Full custom layout	X	X	Graphic database	SDL	Silvar-Lisco	
	Gate array layout		X	Gate array layout	Gatemaster	Daisy	Via Octal Inc. interface
	PCB layout	X	X	Caltech Int. Format	CIF	(Industry standard)	Via Octal Inc. interface
		X	X	Full custom layout	CADD5 2	Computervision	Via Octal Inc. interface
Applicon	PCB layout		X	Schematic capture	ED-Schematics	Control Data	
LEAP	Schematic capture	X	X	PCB layout	V04	Calay Systems	
PCB Layout	PCB layout		X	Database	SCALD	Valid Logic Systems	
			X	Graphic database	SDL	Silvar-Lisco	Via Octal Inc. interface
ASI PRANCE	PCB layout	X		PCB layout	Koloa PCB	Shared Resources	
Augat WRAPID/QUIKDRAW	Wire wrap		X	Schematic capture	Redlog	Racal-Redac	
WRAPID/QWIKDRAW	Wire wrap		X	Schematic capture	SCHEMA	Omaton	
Automated Images IDEEL	Schematic capture	X		Circuit simulator	PSpice	MicroSim	
B&C Microsystems SCH/DE	Schematic capture		X	Schematic capture	DASH	FutureNet	
CAD Group, Inc.(CGI) SALT	Logic simulator	X X X X		ATE	Sentry	Fairchild	
				Fault grader	PFG	Mentor Graphics	
				Fault simulator	PFG	Caedent	
				Intermediate format	ZIF	Zycad	
			X	Logic simulator	TEGAS-5	Calma	
			X	Logic simulator	RTLRC	Hughes Aircraft	
		X		PCB layout	SCICARDS	Sci. Calculations	Links RTLRC to SALT
			X	Schematic capture	CaePac II	CAECO	Links SALT to SCISIM
			X	Schematic capture	CT-1000	Case Technology	
		X		Schematic capture	Vanguard Steller	Case Technology	Multi-window
			X	Schematic capture	ED-Schematics	Control Data	
			X	Schematic capture	SCHEMA	Omaton	
			X	Schematic capture	Schematic Capture	OrCad	
			X	Schematic capture	SCIDESIGN	Sci. Calculations	
Cadam PRANCE	PCB layout		X	Database	SCALD	Valid Logic Systems	
Cadlinc CimCAD	Mechanical CAD	X	X	PCB layout	Route Editor	Cadnetix	
CimPLOT Plotting	Output format		X	PCB layout	Route Editor	Cadnetix	
Cadnetix CADAT	Logic simulator		X	Schematic capture	Design System	NCR Microelectronics	
		X		Test prgm edit/gen	VITEST	NCR Microelectronics	Workstation resident
			X	Timing analysis	VITA	NCR Microelectronics	Workstation resident
Hier. Schem Editor	Schematic capture	X	X	Design database	TDL	Calma	
		X	X	PCB layout	SCICARDS	Sci. Calculations	
Route Editor	PCB layout	X	X	Mechanical CAD	CimCAD	Cadlinc	
		X	X	Output format	CimPLOT Plotting	Cadlinc	
		X	X	Output format	NC drill	Excellon	
			X	Schematic capture	Vanguard Stellar	Case Technology	Netlist, back annotation
			X	Schematic capture	ED-Schematics	Control Data	
			X	Schematic capture	SCHEMA	Omaton	
			X	Schematic capture	Expert Schematics	XEROX	
CAECO CAEPAC II	Schematic capture	X		Logic simulator	SALT	CAD Group, Inc.(CGI)	
Schematic Capture	Schematic capture	X		Logic simulator	VERILOG	Gateway Des. Auto.	
Caedent PFG	Fault simulator		X	Logic simulator	SALT	CAD Group, Inc.(CGI)	
			X	Schematic capture	Vanguard Stellar	Case Technology	Netlist
Calay Systems V04	PCB layout	X X	X X	Database Logic simulator Schematic capture	SCALD PC-LOGS LEAP CALOS 6000 CT-1000 ED-Schematics DRAWING EDITOR II Automatic Schematic DASH Design Capture Sys. NETED SCHEMA NX-CALAY PC-CAPS Redlog DDSC	Valid Logic Systems P.CAD Applicon CALOS Case Technology Control Data Daisy Drafting Dynamics FutureNet Hewlett-Packard Mentor Graphics Omaton P-CAD P-CAD Racal-Redac Tektronix/CAE	US & European versions   <

DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→) (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Calma							
GDS I	Full custom layout	X	X	Full custom layout	GDS II	Calma	Via Octal Inc. interface
GDS II	Full custom layout	X	X	Caltech Int. Format	CIF	(Industry standard)	Via Octal Inc. interface
		X	X	Full custom layout	APLE860	Applicon	Via Octal Inc. interface
		X	X	Full custom layout	GDS I	Calma	Via Octal Inc. interface
		X	X	Graphic database	SDL	Silvar-Lisco	
		X	X	Silicon compiler	Genesis & Genesil	Silicon Compilers	
		X	X	Standard cell layout	Tancell	Tangent Systems	
	Output format	X	X	Silicon compiler	C4 Compiler	Seattle Silicon	
		X	X	Silicon compiler	C5 Compiler	Seattle Silicon	
		X	X	Silicon compiler	Compile	Unicorn	
	PCB layout	X	X	PCB layout	APLE870	Applicon	Via Octal Inc. interface
GDS1LU, GDS1DC	Full custom layout		X	Caltech Int. Format	CIF	(Industry standard)	Via Octal Inc. interface
TDL	Graphic database	X		Fault simulator	Aida Fault Simulator	Aida	
		X		Logic design rule ck	Aida LDRC	Aida	
		X		Logic simulator	Aida Logic Simulator	Aida	
		X		Logic simulator	VERILOG	Gateway Des. Auto.	
		X	X	Schematic capture	Hierarch Schem Edit	Cadnetix	
		X		Test prgm edit/gen	Aida ATPG	Aida	
		X		Timing analysis	TimVer	Aida	
TEGAS-5	Logic simulator	X		ATE	Sentry	Fairchild	via T.S.S.I.
		X		ATE	Sentry	Fairchild	
		X		ATE	(various)	Genrad	via T.S.S.I.
		X		ATE	(various)	Genrad	via T.S.S.I.
		X		ATE	Hewlett-Packard	Hewlett-Packard	via T.S.S.I.
		X		ATE	Logic Master	IMS	via T.S.S.I.
		X		ATE	Semi Test Solutions	Semi Test Solutions	via T.S.S.I.
		X		ATE	Advantest	Takeda Riken	
		X		ATE	Advantest	Takeda Riken	via T.S.S.I.
		X		ATE	(various)	Teradyne	
		X		ATE	Teradyne	Teradyne	via T.S.S.I.
		X		ATE	Trillium	Trillium	via T.S.S.I.
			X	Database	SCALD	Valid Logic Systems	
			X	Design database	CIEDS	IBM	
			X	Design database	IDEA System	Mentor Graphics	
			X	Graphic database	SDL	Silvar-Lisco	Via TDLNET
		X		Logic sim. accel.	MX/MXT/NSE	XCAT	
		X		Logic simulator	SALT	CAD Group, Inc.(CGI)	
		X	X	Netlist + ->schematic	Schematic Generator	Trimeter Tech.	
		X	X	Schematic capture	Vanguard Stellar	Case Technology	Netlist
		X	X	Schematic capture	ED-Schematics	Control Data	
		X	X	Schematic capture	Ed-Schematics	Control Data	Via CYBERNET®EXPRESS
		X	X	Schematic capture	Lognet	Elec. Software Prod.	
		X	X	Schematic capture	NETED	Mentor Graphics	Via TLDNET
		X	X	Schematic capture	Grale/Lognet	NCA	via CYBERNET®EXPRESS
		X	X	Schematic capture	NX-TDL	P-CAD	
		X	X	Schematic capture	PC-CAPS	P-CAD	
		X	X	Standard cell layout	Tancell	Tangent Systems	
TEXSIM/B	Logic simulator	X		ATE	Sentry	Fairchild	via T.S.S.I.
		X		ATE	Sentry	Fairchild	
		X		ATE	(various)	Genrad	via T.S.S.I.
		X		ATE	(various)	Genrad	via T.S.S.I.
		X		ATE	Hewlett-Packard	Hewlett-Packard	via T.S.S.I.
		X		ATE	Logic Master	IMS	via T.S.S.I.
		X		ATE	Semi Test Solutions	Semi Test Solutions	via T.S.S.I.
		X		ATE	Advantest	Takeda Riken	
		X		ATE	Advantest	Takeda Riken	via T.S.S.I.
		X		ATE	(various)	Teradyne	
		X		ATE	Teradyne	Teradyne	via T.S.S.I.
		X		ATE	Trillium	Trillium	via T.S.S.I.
		X		Fault sim. accel.	Logic Evaluator	Zycad	
		X		Logic sim. accel.	Logic Evaluator	Zycad	
CALOS							
CALOS 6000	Schematic capture	X		Circuit simulator	PSpice	MicroSim	
		X		Des verification sys	CATS	HHB Systems	
		X		Logic simulator	CADAT	HHB Systems	
		X		Logic simulator	PC CADAT	HHB Systems	
		X	X	Output format	Auto Insertion Sys.	Universal	
		X	X	PCB layout	V04	Calay Systems	
		X	X	PCB layout	CADDS 4X	Computervision	
		X	X	PCB layout	DSM-6,Maxi-II	Racal-Redac	
		X	X	PCB layout	MAXI-II	Racal-Redac	
		X	X	PCB layout	Maxi-II	Racal-Redac	
		X	X	PCB layout	Redboard	Racal-Redac	
		X	X	PCB layout	SCICARDS	Sci. Calculations	
		X	X	PCB layout	EDA-3000	Telesis	
Case Technology							
CT-1000	Schematic capture	X		Circuit simulator	SPICE	(Industry standard)	Via Torric Inc. FRENED
		X	X	Circuit simulator	HSpice	Meta-Software	
		X	X	Circuit simulator	PSpice	MicroSim	
		X	X	Gate array layout	GARDS	Silvar-Lisco	Via Torric Inc. FRENED
		X	X	Logic simulator	LIBSIM	ACASI	
		X	X	Logic simulator	SALT	CAD Group, Inc.(CGI)	
		X	X	Logic simulator	HILO	Genrad	Via Torric Inc. FRENED
		X	X	Logic simulator	HELIX	Silvar-Lisco	Via Torric Inc. FRENED
		X	X	Logic simulator	SILOS	Simucad	
		X	X	Logic simulator	SILOS	Simucad	Via Torric Inc. FRENED
		X	X	PCB layout	V04	Calay Systems	
		X	X	PCB layout	CADDS 4X	Computervision	
		X	X	PCB layout	CBDS	IBM	
		X	X	PCB layout	PATHLINK/AUTOLINK	Mentor Graphics	
		X	X	PCB layout	Model 100	Paragon	
		X	X	PCB layout	EDMS	Prime Computer	
		X	X	PCB layout	Redboard	Racal-Redac	



DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→) (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Case Technology (Cont'd) CT-1000	Schematic capture	X X X X X X	X	PCB layout PCB layout PCB layout PCB layout PLD development sys. Standard cell layout	SCICARDS Crystal Router EDA-3000 Allegro CUPL CAL-MP	Sci. Calculations Shared Resources Telesis Valid Logic Systems P-CAD Silvar-Lisco	Netlist Xfer & back annotation  Via Torric Inc. FREND
CT-2000	Schematic capture	X X	X X	Reliability predict Reliability predict	PC-Predictor Predictor	MSI MSI	Via SYS call Circuit Base PC-1 Via SYS call Circuit Base PC-1
Vanguard Stellar	Schematic capture	X X					

DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→)   (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Daisy DLS	Logic simulator	X X X X X X X X X X X		ATE ATE ATE ATE ATE ATE ATE ATE ATE ATE ATE	Sentry Sentry (various) Hewlett-Packard Logic Master Semi Test Solutions Advantest Advantest (various) Teradyne Trillium MIMIC Genesil	Fairchild Fairchild Genrad Genrad Hewlett-Packard IMS Semi Test Solutions Takeda Riken Takeda Riken Teradyne Teradyne Teradyne Trillium GE/RCA Silicon Compilers	via T.S.S.I.  via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I.  via T.S.S.I.  via T.S.S.I. via T.S.S.I.
DRAWING EDITOR II	PLD library Schematic capture	X X X X X X X X X X X	X	PLD development sys. Cell based layout Logic simulator Logic simulator Logic simulator Logic simulator PCB layout PCB layout PCB layout PCB layout Silicon compiler Simulation models Standard cell layout	ABEL Harris/SDA Worksta. VERILOG HILO LDS LASAR LASAR V04 Visula PCB Koloa PCB Allegro ULA Silicon Compiler Lin Cad II Tancell	Data I/O Harris Semiconductor Gateway Des. Auto. Genrad LSI Logic Teradyne Teradyne Calay Systems Racal-Redac Shared Resources Valid Logic Systems Ferranti Interdesign Micro Linear Tangent Systems	ABLE PLD simul in DAISY lib.          Netlist Xfer & back annotation
Gatemaster	Gate array layout	X X	X	Gate array layout Logic/fault sim.	APPLE860 MIMIC	Applicon GE/RCA	
Data I/O ABEL	PLD development sys	X  X X  X	X	Database Graphic database Logic simulator Logic simulator Schematic capture Schematic capture Schematic capture	SCALD SDL LIBSIM LIBSIM DRAWING EDITOR II DASH NETED Expert Schematics	Valid Logic Systems Silvar-Lisco ACASI ACASI Daisy FutureNet Mentor Graphics XEROX	ABLE PLD simul. in PAL library  Simulates PLDs/fuse maps  Partitioning/generic gate lib. ABLE PLDs simul./Mentor Lib.
DataCon WRAPID2	Wire wrap		X X	Schematic capture Schematic capture	SCHEMA Redlog	Omaton Racal-Redac	
Design Computation DC/Autorouter II	PCB layout		X X X X X X X	Schematic capture Schematic capture Schematic capture Schematic capture Schematic capture Schematic capture Schematic capture	DASH Design Capture Sys. SCHEMA SDT PC-CAPS Redlog SCICARDS	FutureNet Hewlett-Packard Omaton OrCad P-CAD Racal-Redac Sci. Calculations	
Drafting Dynamics Auto. Schematic	Schematic capture	X X	X	PCB layout PCB layout	V04 CADD5 4X	Calay Systems Computervision	
ECAD Dracula	IC layout verify	X X	X	Full custom layout Silicon compiler	CHIPGRAPH Compile	Mentor Graphics Unicorn	
SIMON	Circuit simulator		X	Parameter extraction	TOPEX	Tech Modeling Assoc	
Symbad BPR	Block place & route	X	X	Silicon compiler	Compile	Unicorn	
Elec Software Prod. Lognet	Schematic capture	X X		Logic simulator PCB layout	TEGAS-5 DSM-6, Maxi-II	Calma Racal-Redac	
Elec. Eng. Software PRECISE	Circuit simulator	X X X X X	X	Circuit simulator Circuit simulator Schematic capture Schematic capture Schematic capture	MSPICE Analog Designer CIEDS Visula CAE ViewDraw	Mentor Graphics Valid Logic Systems IBM Racal-Redac Viewlogic	
ELXSI Parallel SPICE	Circuit simulator		X	Schematic capture	Lin Cad II	Micro Linear	
Excellon CNC	NC drill		X	PCB layout	Route Editor	Cadnetix	
Mark/3	NC drill		X	PCB layout	Expert PCB	XEROX	
Fairchild Sentry	ATE		X	Logic sikulator Logic simulator Logic			



DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→) (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Fairchild (Cont'd) Sentry	ATE		X	Logic simulator	LASAR	Teradyne	via T.S.S.I.
			X	Logic simulator	Validsim	Valid Logic Systems	via T.S.S.I.
			X	Logic simulator	ViewSim	Viewlogic	via T.S.S.I.
			X	Logic simulator	LOGIC	Western Des. Center	Generates test vectors
			X	Logic simulator	ZILOS	Zycad	via T.S.S.I.
		X	X	Silicon compiler	Compile	Unicorn	
			X	Standard cell layout	Tancell	Tangent Systems	
			X	Test prgm edit/gen	LIBTEST	ACASI	
			X	Test prgm edit/gen	VITEST	NCR Microelectronics	
	ATE S		X	Logic simulator	SILOS	Simucad	via T.S.S.I.
Ferranti Interdesign ULA Silicon Compiler	Silicon compiler		X	Database	SCALD	Valid Logic Systems	
			X	Logic simulator	HILO	Genrad	
			X	Schematic capture	DRAWING EDITOR II	Daisy	
			X	Schematic capture	NETED	Mentor Graphics	
FutureNet DASH	Schematic capture	X		Circuit simulator	SPICE	(Industry standard)	Via Torric Inc. FREND
		X		Circuit simulator	PSPice	MicroSim	
		X		Gate array layout	GARDS	Silvar-Lisco	Via Torric Inc. FREND
		X		Logic sim. accel.	MX/MXT/HSE	XCAT	
		X		Logic simulator	LIBSIM	ACASI	Dir. interface/no translation
		X		Logic simulator	LIBSIM	ACASI	
		X		Logic simulator	HILO	Genrad	Via Torric Inc. FREND
		X		Logic simulator	LDS	LSI Logic	
		X		Logic simulator	HELIX	Silvar-Lisco	Via Torric Inc. FREND
		X		Logic simulator	SILOS	Simucad	Via Torric Inc. FREND
		X		PCB layout	V04	Calay Systems	
		X		PCB layout	DC/Autorouter II	Design Computation	
		X		PCB layout	PC800 Model 4	Gerber	
		X		PCB layout	PC-CARDS	P-CAD	
		X		PCB layout	Koloa PCB	Shared Resources	
		X		PCB layout	Crystal Router	Shared Resources	
		X	X	PCB layout	Allegro	Valid Logic Systems	Netlist Xfer & back annotation
		X		PCB layout	DNA2000	Vectron Graphics	
		X		PLD development sys.	PLE20	Altera	
		X		PLD development sys.	ABEL	Data I/O	Partitioning/generic gate lib.
		X		Schematic capture	SCH/DE	B&C Microsystems	
		X	X	Schematic capture	Vanguard Stellar	Case Technology	Netlist, graphics
		X		Standard cell layout	CAL-MP	Silvar-Lisco	Via Torric Inc. FREND
DASH-CADAT	Logic simulator		X	Logic/fault sim.	MIMIC	GE/RCA	
DASH-PCB	PCB layout		X	Schematic capture	SCHEMA	Omaton	
Gateway Des. Auto. AIDSSIM	Fault simulator	X		Logic simulator	VERILOG	Gateway Des. Auto.	
	Logic simulator		X	Schematic capture	Ed-Schematics	Control Data	
AIDSTG	Fault simulator	X		Schematic capture	Ed-Schematics	Control Data	Via CYBERNET®EXPRESS
VERILOG	Test prgm edit/gen	X		Logic simulator	VERILOG	Gateway Des. Auto.	
		X		Logic simulator	VERILOG	Gateway Des. Auto.	
VERILOG	Logic simulator	X		ATE	Sentry	Fairchild	via T.S.S.I.
		X		ATE	(various)	Genrad	via T.S.S.I.
		X		ATE	Hewlett-Packard	Hewlett-Packard	via T.S.S.I.
		X		ATE	Logic Master	IMS	via T.S.S.I.
		X		ATE	Semi Test Solutions	Semi Test Solutions	via T.S.S.I.
			X	ATE	Advantest	Takeda Riken	via T.S.S.I.
			X	ATE	Teradyne	Teradyne	via T.S.S.I.
			X	ATE	Trillium	Trillium	via T.S.S.I.
			X	Database	SCALD	Valid Logic Systems	
			X	Fault simulator	AIDSSIM	Gateway Des. Auto.	
			X	Graphic database	TDL	Calma	
			X	Schematic capture	Schematic Capture	CAECO	
			X	Schematic capture	ED-Schematics	Control Data	
			X	Schematic capture	Ed-Schematics	Control Data	
			X	Schematic capture	DRAWING EDITOR II	Daisy	
			X	Schematic capture	NETED	Mentor Graphics	
			X	Test prgm edit/gen	AIDSTG	Gateway Des. Auto.	
GE/RCA MIMIC	Logic/fault sim.	X	X	Gate array layout	Gatemaster	Daisy	
		X	X	Logic simulator	DLS	Daisy	
		X		Logic simulator	DASH-CADAT	FutureNet	
	Logic/fault Sim. Logic/fault sim.	X		Logic simulator	Quicksim	Mentor Graphics	
		X		Logic simulator	PC-LOGS	P-CAD	
		X		Logic simulator	Validsim	Valid Logic Systems	
		X	X	PCB layout	MERLYN-P	Tektronix/CAE	
Genrad (various)	ATE		X	Database	SCALD	Valid Logic Systems	
			X	Logic simulator	TEGAS-5	Calma	
			X	Logic simulator	TEXSIM/B	Calma	
			X	Logic simulator	TEGAS-5	Calma	via T.S.S.I.
			X	Logic simulator	TEXSIM/B	Calma	via T.S.S.I.
			X	Logic simulator	DLS	Daisy	
			X	Logic simulator	DLS	Daisy	via T.S.S.I.
			X	Logic simulator	VERILOG	Gateway Des. Auto.	via T.S.S.I.
			X	Logic simulator	HILO	Genrad	
			X	Logic simulator	HILO	Genrad	via T.S.S.I.
			X	Logic simulator	Quicksim	Mentor Graphics	
			X	Logic simulator	Quicksim	Mentor Graphics	via T.S.S.I.
			X	Logic simulator	HELIX	Silvar-Lisco	
			X	Logic simulator	HELIX	Silvar-Lisco	via T.S.S.I.
			X	Logic simulator	LOGIX	Silvar-Lisco	via T.S.S.I.
			X	Logic simulator	SILOS	Simucad	via T.S.S.I.
			X	Logic simulator	LASAR	Teradyne	
			X	Logic simulator	LASAR	Teradyne	via T.S.S.I.
			X	Logic simulator	Validsim	Valid Logic Systems	via T.S.S.I.

DESIGN AUTOMATION—Design Tool Interfaces							
Source Name	Function	Interface Direction (→) (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Genrad (Cont'd) (various)	ATE		X	Logic simulator	ViewSim	Viewlogic	via T.S.S.I.
			X	Logic simulator	ZILOS	Zycad	via T.S.S.I.
			X	PCB layout	Allegro	Valid Logic Systems	Pin list information
			X	Standard cell layout	Tancell	Tangent Systems	
			X	Test prgm edit/gen	LIBTEST	ACASI	
HICHIP	Physical modeler	X	X	Schematic capture	HSD	Intergraph	
HILO	Fault simulator		X	Silicon compiler	Genesil	Silicon Compilers	
	Logic simulator	X	X	ATE	Sentry	Fairchild	via T.S.S.I.
		X	X	ATE	(various)	Genrad	
		X	X	ATE	(various)	Genrad	via T.S.S.I.
		X	X	ATE	Hewlett-Packard	Hewlett-Packard	via T.S.S.I.
		X	X	ATE	Logic Master	IMS	via T.S.S.I.
		X	X	ATE	Semi Test Solutions	Semi Test Solutions	via T.S.S.I.
		X	X	ATE	Advantest	Takeda Riken	
		X	X	ATE	Advantest	Takeda Riken	via T.S.S.I.
		X	X	ATE	(various)	Teradyne	
		X	X	ATE	Teradyne	Teradyne	via T.S.S.I.
		X	X	ATE	Trillium	Trillium	via T.S.S.I.
			X	Design database	CIEDS	IBM	
			X	Graphic database	SDL	Silvar-Lisco	
		X	X	Logic simulator	LIBSIM	ACASI	
			X	Schematic capture	CT-1000	Case Technology	
			X	Schematic capture	Schedit	Computeruision	
			X	Schematic capture	DRAWING EDITOR II	Daisy	Via Torric Inc. FRENED
			X	Schematic capture	DASH	FutureNet	
			X	Schematic capture	IEDS	Intergraph	
		X	X	Schematic capture	NETED	Mentor Graphics	
			X	Schematic capture	NX-HILO	P.CAD	
			X	Schematic capture	PC-CAPS	P.CAD	
			X	Schematic capture	PC-CAPS	P.CAD	Via Torric Inc. FRENED
		X	X	Schematic capture	Redlog	Racal-Redac	Post process waveform analysis
		X	X	Schematic capture	Visula CAE	Racal-Redac	
			X	Schematic capture	Designer's Edge	SDA	
		X	X	Schematic capture	DDSC	Tektronix/CAE	
			X	Schematic capture	Expert Schematics	XEROX	
			X	Silicon compiler	Genesil	Silicon Compilers	
		X	X	Standard cell layout	TANCELL	Intergraph	Netlist interconnect delay
		X	X	Standard cell layout	Tancell	Tangent Systems	
		X	X	Standard cell layout	Tancell	Tangent Systems	Netlist transfer
		X	X	Waveform display	Waveform Display	SDA	
Gerber Sci. Instr. PC800 Model 4	PCB layout		X	Schematic capture	DASH	FutureNet	
Harris Semiconductor Harris/SDA Worksta.	Cell based layout		X	Schematic capture	DRAWING EDITOR II	Daisy	
			X	Schematic capture	NETED	Mentor Graphics	
Hewlett-Packard Design Capture Sys	Schematic capture	X	X	PCB layout	V04	Calay Systems	
		X	X	PCB layout	CADDS 4X	Computeruision	
		X	X	PCB layout	DC/Autorouter II	Design Computation	
		X	X	PCB layout	Visula PCB	Racal-Redac	
		X	X	PCB layout	SCICARDS	Sci. Calculations	
DTS-70	Board-test system		X	Logic simulator	LASAR	Teradyne	
Hewlett-Packard	ATE		X	Logic simulator	TEGAS-5	Calma	via T.S.S.I.
			X	Logic simulator	TEXSIM/B	Calma	via T.S.S.I.
			X	Logic simulator	DLS	Daisy	via T.S.S.I.
			X	Logic simulator	VERILOG	Gateway Des. Auto.	via TSSI
			X	Logic simulator	HILO	Genrad	via T.S.S.I.
			X	Logic simulator	Quicksim	Mentor Graphics	via T.S.S.I.
			X	Logic simulator	HELIX	Silvar-Lisco	via T.S.S.I.
			X	Logic simulator	LOGIX	Silvar-Lisco	via T.S.S.I.
			X	Logic simulator	SILOS	Simucad	via T.S.S.I.
			X	Logic simulator	LASAR	Teradyne	via T.S.S.I.
			X	Logic simulator	Validsim	Valid Logic Systems	via T.S.S.I.
			X	Logic simulator	ViewSim	Viewlogic	via T.S.S.I.
			X	Logic simulator	ZILOS	Zycad	via T.S.S.I.
HP9000	IC prototype test		X	Schematic capture	Lin Cad II	Micro Linear	
Plotter	Output format		X	Silicon compiler	C4 Compiler	Seattle Silicon	
			X	Silicon compiler	C5 Compiler	Seattle Silicon	
HBB Systems CADAT	Logic simulator	X	X	Circuit + -> logic sim	PSpice:Digital Files	MicroSim	
		X	X	Logic simulator	LIBSIM	ACASI	
			X	Schematic capture	CALOS 6000	CALOS	Netlist, waveforms
			X	Schematic capture	Vanguard Stellar	Case Technology	
			X	Schematic capture	Ed-Schematics	Control Data	
			X	Schematic capture	Grale/Lognet	NCA	
			X	Schematic capture	NX-CADAT	P.CAD	
			X	Schematic capture	Redlog	Racal-Redac	
		X	X	Schematic capture	Visula CAE	Racal-Redac	Post process waveform analysis
		X	X	Schematic capture	Visula CAE	Racal-Redac	
		X	X	Schematic capture	Expert Schematics	XEROX	
CATS	Verification system		X	Schematic capture	CALOS 6000	CALOS	
PC CADAT	Logic simulator		X	Schematic capture	CALOS 6000	CALOS	
Hughes Aircraft RTRC	Logic simulator	X		Logic simulator	SALT	CAD Group, Inc.(CGI)	
IBM CBDS	PCB layout	X	X	Database	SCALD	Valid Logic Systems	
			X	Design database	CIEDS	IBM	
			X	Graphic database	SDL	Silvar-Lisco	
		X	X	PCB layout	Koloa PCB	Shared Resources	
		X	X	Schematic capture	CT-1000	Case Technology	



Source Name	Function	Interface Direction (→)   (←)	Function	Name	Source	Comments
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IBM (Cont'd)							
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DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→)   (←)		Function	Name	Source	Comments		
Design Tool Interfaces (Cont'd)									
Mentor Graphics (Cont'd) NETED	Schematic capture	X		PCB layout	CADDS 4X	Computervision	Via CVNET		
		X	X	PCB layout	IEDS	Intergraph			
		X		PCB layout	DSM-6,Maxi-II	Racal-Redac	Via REDACNET		
		X	X	PCB layout	SCICARDS	Sci. Calculations	CAE interface via MS-CINT		
		X		PCB layout	EDA-3000	Telesis	Via TELESISNET		
		X		PLD development sys.	ABEL	Data I/O	ABEL PLD simul in Mentor libr.		
		X	X	Schematic capture	Vanguard Stellar	Case Technology	Graphics		
		X	X	Schematic capture	ED-Schematics	Control Data			
		X		Silicon compiler	ULA Silicon Compiler	Ferranti Interdesign			
		X		Test prgm edit/gen	Aida ATPG	Aida			
X		Timing analysis	TimVer	Aida					
PATHLINK/AUTOLINK	PCB layout	X	X	Schematic capture	CT-1000	Case Technology			
PFG	Fault grader		X	Logic simulator	SALT	CAD Group, Inc.(CGI)			
Quicksim	Logic simulator	X		ATE	Sentry	Fairchild	via T.S.S.I.		
		X		ATE	Sentry	Fairchild			
		X		ATE	(various)	Genrad			
		X		ATE	(various)	Genrad	via T.S.S.I.		
		X		ATE	Hewlett-Packard	Hewlett-Packard	via T.S.S.I.		
		X		ATE	Logic Master	IMS	via T.S.S.I.		
		X		ATE	Semi Test Solutions	Semi Test Solutions	via T.S.S.I.		
		X		ATE	Advantest	Takeda Riken			
		X		ATE	Advantest	Takeda Riken	via T.S.S.I.		
		X		ATE	(various)	Teradyne			
		X		ATE	Teradyne	Teradyne	via T.S.S.I.		
		X		ATE	Trillium	Trillium	via T.S.S.I.		
		X		Logic sim. accel.	Logic Evaluator	Zycad			
		X	X	Logic/fault sim.	MIMIC	GE/RCA			
Meta-Software HSpice	Circuit simulator	X	X	Schematic capture	CT-1000	Case Technology			
		X	X	Schematic capture	PC-CAPS	P-CAD			
		X	X	Schematic capture	Designer's Edge	SDA			
		X	X	Silicon compiler	Compile	Unicorn			
	Waveform display			Waveform Display	Waveform Display	SDA			
Micro Linear Lin Cad II	Schematic capture	X		ATE	HP9000	Hewlett-Packard			
		X		Circuit sim. accel.	Parallel SPICE	ELXSI			
	Simulation models	X		Circuit simulator	Analog Workbench	Analog Design Tools			
		X		Schematic capture	DRAWING EDITOR II	Daisy			
MicroSim PSpice	Circuit simulator		X	Schematic capture	IDEEL	Automated Images			
		X	X	Schematic capture	CALOS 6000	CALOS			
		X	X	Schematic capture	CT-1000	Case Technology			
		X	X	Schematic capture	Vanguard Stellar	Case Technology	Netlist, waveforms		
		X	X	Schematic capture	Vanguard Stellar	Case Technology			
		X	X	Schematic capture	Schematic Capture	Chancellor			
		X	X	Schematic capture	DASH	FutureNet			
		X	X	Schematic capture	SCHEMA	Omaton			
		X	X	Schematic capture	SDT	OrCad			
		X	X	Schematic capture	PC-CAPS	P-CAD			
		X	X	Schematic capture	Captast CF-1000	Phase III Logic			
		X	X	Schematic capture	ViewDraw	Viewlogic			
		PSpice MixedMode Opt	Circuit simulator	X	X	Logic simulator	ViewSim	Viewlogic	True mixed A/D sim w/feedback
		PSpice:Digital Files	Circuit + →logic sim	X	X	Logic simulator	CADAT	HHB Systems	
		X	X	Logic simulator	VST	OrCad			
		X	X	Logic simulator	SILOS	Simucad			
		X	X	Logic simulator	ViewSim	Viewlogic			
MMI PALASM	PLD development sys		X	Graphic database	SDL	Silvar-Lisco			
		X		Logic simulator	LIBSIM	ACASI			
MOSAID MOSFIT	MOS transistor model	X		Circuit simulator	SimIC	MOSAID			
SimIC	MOS transistor model	X		Circuit simulator	MOSFIT	MOSAID			
Motorola MCA Design System	Gate array layout		X	Schematic capture	PC-CAPS	P-CAD			
MSI PC-Predictor	Reliability predict	X	X	Design database	CYBERNET*EXPRESS	Control Data			
		X	X	Schematic capture	CT-2000	Case Technology			
		X	X	Design database	CYBERNET*EXPRESS	Control Data			
		X	X	PC circuit simulator	SYSCAP	Control Data			
Predictor	Reliability predict	X	X	Schematic capture	CT-2000	Case Technology			
		X	X	Schematic capture	Ed-Schematics	Control Data			
NCA DVS	IC layout verify		X	Graphic database	SDL	Silvar-Lisco			
			X	Schematic capture	NETED	Mentor Graphics	NETED		
		X		Circuit simulator	SPICE	(Industry standard)			
		X		Logic simulator	TEGAS-5	Calma			
Grate/Lognet	Schematic capture	X		Logic simulator	CADAT	HHB Systems			
		X		Logic simulator	SILOS	Simucad			
MDL	IC layout verify		X	Design database	IDEA System	Mentor Graphics			
NCR Microelectronics VIGEN	Generate/Compile Schematic capture	X		Schematic capture	NETED	Mentor Graphics			
		X		Logic simulator	CADAT	Cadnetix	Workstation-Resident		
	VILAY	Standard cell layout	X	X	Gate array layout	Gate Station	Mentor Graphics		
			X	X	Standard cell layout	Cell Station	Mentor Graphics		
	VITA	Timing analysis	X		Logic simulator	CADAT	Cadnetix	Workstation-Resident	
VITEST	Test prgm edit/gener	X		ATE	Sentry	Fairchild			
			X	Logic simulator	CADAT	Cadnetix	Workstation-Resident		



DESIGN AUTOMATION—Design Tool Interfaces											
Source Name	Function	Interface Direction (→)   (←)		Function	Name	Source	Comments				
Design Tool Interfaces (Cont'd)											
Omation SCHEMA	Schematic capture	X	X	Circuit simulator	SPICE	(Industry standard)	Pin List				
		X		Circuit simulator	PSpice	MicroSim	Pin List				
		X		Circuit simulator	PSpice	MicroSim	Net List				
		X		Intermediate format	EDIF	(Industry standard)					
		X		Logic simulator	LIBSIM	ACASI					
		X		Logic simulator	SALT	CAD Group, Inc.(CGI)					
		X		PCB layout	Route Editor	Cadnetix					
		X		PCB layout	V04	Calay Systems					
		X		PCB layout	CADDS 4X	Computervision					
		X		PCB layout	DC/Autorouter II	Design Computation					
		X		PCB layout	DASH-PCB	FutureNet					
		X		PCB layout	IEDS	Intergraph					
		X		PCB layout	PC-CARDS	P-CAD					
		X		PCB layout	Redboard	Racal-Redac					
		X		PCB layout	SCICARDS	Sci. Calculations					
		X		PCB layout	EDA-3000	Telesis					
		X		Schematic capture	SCHEMA	Omation					
X	Schematic capture	SCHEMA	Omation								
X	Wire wrap	WRAPID/QUIKDRAW	Augat								
X	Wire wrap	WRAPID2	DataCon								
Optima OPTIMATE	PCB layout	X X X	X X X	Database Design database Graphic database	SCALD IDEA System SDS	Valid Logic Systems Mentor Graphics Silvar-Lisco	With back annotation With Back Annotation With Back annotation				
OrCad SDT	Schematic capture	X X X		Circuit simulator Logic simulator PCB layout	PSpice SALT DC/Autorouter II	MicroSim CAD Group, Inc.(CGI) Design Computation					
VST	Logic simulator	X	X	Circuit + →logic sim	PSpice:Digital Files	MicroSim					
P-CAD CUPL	PLD development sys	X X	X X	Logic simulator Schematic capture Schematic capture	LIBSIM CT-1000 Vanguard Stellar	ACASI Case Technology Case Technology	Netlist				
	NX-CADAT	Schematic capture	X		Logic simulator	CADAT	HHB Systems				
	NX-CALAY	Schematic capture	X		PCB layout	V04	Calay Systems				
	NX-CBDS	Schematic capture	X	X	PCB layout	CBDS	IBM				
	NX-CV	Schematic capture	X	X	PCB layout	CADDS 4X	Computervision				
	NX-HILO	Schematic capture	X		Logic simulator	HILO	Genrad				
	NX-SCI	Schematic capture	X	X	PCB layout	SCICARDS	Sci. Calculations				
	NX-SPICE	Schematic capture	X		Circuit simulator	SPICE	(Industry standard)				
	NX-TDL	Schematic capture	X		Logic simulator	TEGAS-5	Calma				
	PC-CAPS	Schematic capture	X X X X X X X X X X X X X X X X X	X	Circuit simulator Circuit simulator Gate array layout Gate array layout Logic simulator Logic simulator Logic simulator Logic simulator Logic simulator Logic simulator PCB layout PCB layout PCB layout PCB layout PCB layout PCB layout PCB layout PCB layout PCB layout PLD development sys. Standard cell layout	HSpice PSpice MCA Design System GARDS TEGAS-5 HILO HILO LDS HELIX SILOS V04 CADDS 4X DC/Autorouter II CBDS SCICARDS Koloa PCB Crystal Router TI Design System PLE20 CAL-MP	Meta-Software MicroSim Motorola Silvar-Lisco Calma Genrad Genrad LSI Logic Silvar-Lisco Simucad Calay Systems Computervision Design Computation IBM Sci. Calculations Shared Resources Shared Resources Texas Instruments Altera Silvar-Lisco	Via Torric Inc. FRENED  Via Torric Inc. FRENED Semi-custom IC layout Via Torric Inc. FRENED Via Torric Inc. FRENED Hardware P.C.B. layout engine  Via Torric Inc. FRENED			
					X	Schematic capture	DASH	FutureNet			
					X	Schematic capture	SCHEMA	Omation			
			PC-CARDS		PCB layout		X	Logic/fault sim. PCB layout PLD development sys.	MIMIC V04 PLDSMOD1	GE/RCA Calay Systems Altera	12-state simulator
			PC-LOGS		Logic simulator	X X					
			Paragon Model 100		PCB layout	X X	X	PCB layout Schematic capture	Koloa PCB CT-1000	Shared Resources Case Technology	
			Phase III Logic Capfast CF-1000		Schematic capture	X		Circuit simulator	PSpice	MicroSim	
Phillips Philpac			PCB layout			X	Valid Logic	SCALD	Schematic capture		
Phoenix Data Systems LOGCAP			Logic simulator			X X X X	Database Design database Graphic database Schematic capture	SCALD IDEA System SDL NETED	Valid Logic Systems Mentor Graphics Silvar-Lisco Mentor Graphics	Via LOGCAP	
						X X	Design database Schematic capture	IDEA System NETED	Mentor Graphics Mentor Graphics	Via LOGICV	
Praxis Systems ELLA			Behavioral language		X		Hardware descr. lang	ISIS HDL	Racal-Redac		
Prime Computer EDMS			PCB layout Schematic capture		X X	X X	Schematic capture Schematic capture	CT-1000 ED-Schematics	Case Technology Control Data		
Racal-Redac DSM-6			PCB layout		X	X	PCB layout	Visula PCB	Racal-Redac		
DSM-6, Maxi-II			PCB layout			X	Database	SCALD	Valid Logic Systems		

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DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→) (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Seattle Silicon (Cont'd) C5 Compiler	Silicon compiler	X X X X X X X	X X X X X	Circuit simulator Database Design database Output format Output format Output format Schematic capture	SPICE SCALD IDEA System GDS II Plotter Plotter DDSC	(Industry standard) Valid Logic Systems Mentor Graphics Calma Hewlett-Packard Versatec Tektronix/CAE	Database link with all tools Database link with all tools     Database link with all tools
Secmai Secmai	PCB layout	X	X	Database	SCALD	Valid Logic Systems	
Semi Test Solutions Semi Test Solutions	ATE		X X	Logic simulator Logic simulator	TEGAS-5 TEXSIM/B DLS VERILOG HILO Quicksim HELIX LOGIX SILOS LASAR Validsim ViewSim ZILOS	Calma Calma Daisy Gateway Des. Auto. Genrad Mentor Graphics Silvar-Lisco Silvar-Lisco Simucad Teradyne Valid Logic Systems Viewlogic Zycad	via T.S.S.I. via T.S.S.I.
Shared Resources Crystal PCB	PCB layout		X	Schematic capture	DASH	FutureNet	
Crystal Router	PCB layout		X X X X X X X X X	Database Fault simulator PCB layout Schematic capture Schematic capture Schematic capture Schematic capture Schematic capture	SCALD Aida Fault Simulator PCB Layout CT-1000 CBDS PC-CAPS DDSC	Valid Logic Systems Aida Algorex Case Technology IBM P-CAD Tektronix/CAE	
Koloa PCB	PCB layout		X X	Database PCB layout PCB layout PCB layout PCB layout PCB layout PCB layout PCB layout PCB layout Schematic capture Schematic capture Schematic capture	SCALD PCB Layout PRANCE CBDS Model 100 SCICARDS EDA-3000 DRAWING EDITOR II DASH PC-CAPS	Valid Logic Systems Algorex ASI IBM Paragon Sci. Calculations Telesis Daisy FutureNet P-CAD	
Shiva Multisystems Power SPICE	Circuit simulator		X	Graphic database	SDL	Silvar-Lisco	
Sierra Semiconductor MIXsim	Analog/digital sim		X	Schematic capture	NETED	Mentor Graphics	
Signetics Signetics Prgm Table	PLA fuse map	X		Logic simulator	LIBSIM	ACASI	
Silicon Compilers GenesisI	Silicon compiler	X X X X X		Fault simulator IC prototpye verify IC prototype verify Intermediate format Logic simulator	HILO Logic Master Logic Master EDIF DLS	Genrad IMS IMS (Industry standard) Daisy	
GenesisI & Genesis	Silicon compiler	X X		Caltech Int. Format Full custom layout	CIF GDS II	(Industry standard) Calma	
Genesis	Silicon compiler	X		Circuit simulator	SPICE	(Industry standard)	
Silvar-Lisco CAL-MP	Standard cell layout	X	X X				

[illegible]



DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→)   (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Tektronix/CAE (Cont'd) DDSC	Schematic capture		X	Microwave circ. des.	SuperCompact V04	Compact Software	Automatic back annotation Automatic back annotation
		X	X	PCB layout	CADDS 4X	Calay Systems	
		X	X	PCB layout	DSM-6,Maxi-II	Computervision	
		X	X	PCB layout	SCICARDS	Racal-Redac	
		X	X	PCB layout	Crystal Router	Sci. Calculations	
		X	X	PCB layout	MERLYN-P	Shared Resources	
		X	X	Silicon compiler	C3 Compiler	Tektronix/CAE	
		X	X	Silicon compiler	C4 Compiler	Seattle Silicon	
		X	X	Silicon compiler	C5 Compiler	Seattle Silicon	
		X	X	Standard cell layout	CAL-MP	Silvar-Lisco	
		X	X	Standard cell layout	MERLYN-S	Tektronix/CAE	
MERLYN-G	Gate array layout	X	X	Logic/fault sim.	MIMIC	GE/RCA	
		X	X	Schematic capture	DDSC	Tektronix/CAE	
MERLYN-P	PCB layout	X	X	Schematic capture	DDSC	Tektronix/CAE	
MERLYN-S	Standard cell layout	X	X	Schematic capture	DDSC	Tektronix/CAE	
Telesis EDA-1000	Schematic capture	X	X	Logic simulator Logic simulator	LASAR LASAR	Teradyne Teradyne	
EDA-3000	PCB layout		X	Database Design database PCB layout Schematic capture Schematic capture Schematic capture Schematic capture Schematic capture Schematic capture Schematic capture	SCALD IDEA System Koloa PCB CALOS 6000 CT-1000 Vanguard Stellar ED-Schematics NETED SCHEMA DATAView	Valid Logic Systems Mentor Graphics Shared Resources CALOS Case Technology Case Technology Control Data Mentor Graphics Omation Teradyne	Netlist, back annotate  Via TELESISNET
Teradyne DATAView	Schematic capture	X	X	Logic simulator PCB layout PCB layout	LASAR SCICARDS EDA-3000	Teradyne Sci. Calculations Telesis	
J900 Series	ATE		X	Logic simulator	LASAR	Teradyne	
L100/200 Series	ATE		X	Logic simulator	LASAR	Teradyne	
LASAR	Fault simulator Logic simulator	X 					

DESIGN AUTOMATION—Design Tool Interfaces

Source Name	Function	Interface Direction (→)   (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Trillium (Cont'd) Trillium	ATE		X	Logic simulator Logic simulator Logic simulator HELIX Logic simulator SILOS Logic simulator X Logic simulator X Logic simulator X Logic simulator	VERILOG HILO Quicksim HELIX LOGIX SILOS LASAR Validsim ViewSim ZILOS	Gateway Des. Auto. Genrad Mentor Graphics Silvar-Lisco Silvar-Lisco Simucad Teradyne Valid Logic Systems Viewlogic Zycad	via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I.
Trimeter Tech. Logic Consultant	ASIC optimization		X	Schematic capture	NETED	Mentor Graphics	
Schematic Generator	Netlist + ->schematic	X	X	Logic simulator Schematic capture	TEGAS-5 NETED	Calma Mentor Graphics	
Unicorn Compile	Silicon compiler	X	X	ATE Block place & route Caltech Int. Format Circuit simulator Fault simulator IC layout verify Logic simulator Output format Standard cell layout	Sentry Symbad BPR CIF HSpice SILOS Dracula SILOS GDS II CAL-MP	Fairchild ECAD (Industry standard) Meta-Software Simucad ECAD Simucad Calma Silvar-Lisco	For Macroblock IC'S P.G. tape out Accurate timing information        P.G. tape out
United Technologies MCLDL	Logic simulator		X	Database	SCALD	Valid Logic Systems	
Valid Logic Systems Allegro	PCB layout	X	X	ATE Schematic capture Schematic capture Schematic capture	(various) CT-1000 DRAWING EDITOR II DASH	Genrad Case Technology Daisy FutureNet	Pin list information Netlist Xfer & back annotation Netlist Xfer & back annotation Netlist Xfer & back annotation
Analog Designer	Circuit simulator	X	X	Circuit simulator	PRECISE	Elec. Eng. Software	
Real Chip	Physical modeler	X	X	Logic simulator Logic simulator	LASAR LASAR	Teradyne Teradyne	
SCALD	Database	X	X	ATE ATE Circuit simulator SPICE Fault simulator LASAR ADL/STL Logic array design TEGAS-5 Logic simulator VERILOG HILO LDS LOGCAP Logic simulator LOGIX LASAR MCLDL PCB layout PCB layout PCB layout PRANCE PCB layout V04 CADD5 4X PCB layout CBDS PCB layout OPTIMATE Philpac PCB layout DSM-6,Maxi-II Visula PCB PCB layout SCICARDS Secmai PCB layout Koloa PCB Crystal Router EDA-3000 PCB layout PLD development sys. ABEL Silicon compiler Silicon compiler Silicon compiler Standard cell layout	(various) (various) (various) SPICE LASAR ADL/STL TEGAS-5 VERILOG HILO LDS LOGCAP LOGIX LASAR MCLDL PCB Layout APLE860 PRANCE V04 CADD5 4X CBDS PCB layout OPTIMATE Philpac DSM-6,Maxi-II Visula PCB SCICARDS Secmai Koloa PCB Crystal Router EDA-3000 ABEL ULA Silicon Compiler C3 Compiler C5 Compiler Tancell	Genrad Zehntel (Industry standard) Teradyne Texas Instruments Calma Gateway Des. Auto. Genrad LSI Logic Phoenix Data Systems Silvar-Lisco Teradyne United Technologies Academi Applicon Cadam Calay Systems Computervision IBM Optima Phillips Racal-Redac Racal-Redac Sci. Calculations Secmai Shared Resources Shared Resources Telesis Data I/O Ferranti Interdesign Seattle Silicon Seattle Silicon Tangent Systems	US & European versions   <



DESIGN AUTOMATION—Design Tool Interfaces							
Source Name	Function	Interface Direction (→)   (←)		Function	Name	Source	Comments
Design Tool Interfaces (Cont'd)							
Viewlogic (Cont'd) ViewSim	Logic simulator	X X X X X X X X X X X		ATE ATE ATE ATE ATE ATE ATE ATE Circuit simulator Circuit + ->logic sim	Sentry (various) Hewlett-Packard Logic Master Semi Test Solutions Advantest Teradyne Trillium PSPice MixedMode Opt PSPice:Digital Files	Fairchild Genrad Hewlett-Packard IMS Semi Test Solutions Takeda Riken Teradyne Trillium MicroSim MicroSim	via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. True mixed A/D sim w/feedback
Western Des. Center LOGIC	Logic simulator	X		ATE	Sentry	Fairchild	Generates test vectors
Wire Graphics Pen Entry	Wire wrap		X	PCB layout	Expert PCB	XEROX	
XCAT MX/MXT/HSE	Logic sim. accel.		X	Schematic capture	DASH	FutureNet	V19 FutureNet Translator
MX/MXT/NSE	Logic sim. accel.		X X X	Intermediate format Logic simulator Schematic capture	EDIF TEGAS-5 NETED	(Industry standard) Calma Mentor Graphics	Via EDIF Translator Via MX Net Translator
XEROX Expert PCB	PCB layout	X X X		Output format Output format Wire wrap	NC drill Photoplot Pen Entry	Excellon Gerber Wire Graphics	
Expert Schematics	Schematic capture	X X X X X X X X X X	X   X  X X	Circuit simulator Circuit simulator Logic simulator Logic simulator Logic simulator PCB layout PCB layout PLD development sys.	SPICE Analog Workbench HILO CADAT LASAR CADD5 4X SCICARDS ABEL	(Industry standard) Analog Design Tools Genrad HHB Systems Teradyne Computervision Sci. Calculations Data I/O	
Zehntel (various)	ATE		X	Database	SCALD	Valid Logic Systems	
Zycad Fault Evaluator	Fault sim. accel.		X	Graphic database	SDL	Silvar-Lisco	
Logic Evaluator	Fault sim. accel. Logic sim. accel.		X X X X X X X	Logic simulator Graphic database Logic simulator Logic simulator Logic simulator Schematic capture	TEXSIM/B SDL LIBSIM TEXSIM/B Quicksim DDSC	Calma Silvar-Lisco ACASI Calma Mentor Graphics Tektronix/CAE	Graphical post processing disp
ZIF	Intermediate format		X	Logic simulator	SALT	CAD Group, Inc.(CGI)	
ZILOS	Logic simulator	X X X X X X X X X		ATE ATE ATE ATE ATE ATE ATE ATE ATE	Sentry (various) Hewlett-Packard Logic Master Semi Test Solutions Advantest Teradyne Trillium	Fairchild Genrad Hewlett-Packard IMS Semi Test Solutions Takeda Riken Teradyne Trillium	via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I. via T.S.S.I.

DESIGN AUTOMATION—Hardware Vs. Software			
Computing Platform	Design Automation Software	Function	Source
Computing Platforms for Design Automation Software			
APOLLO	BOARD Series AUTOART MiCAD PATHLINK/AUTOLINK OPTIMATE Place and Route VISULA KOLOA PCB Design System Crystal Router OPTIMATE MERLYN-P PCB Design	Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool	Calma Compact Software EEsof Mentor Graphics Optima Technology Racal-Redac Shared Resources Shared Resources Silver-Lisco Tektronix CAE Systems Vectron Graphics
	PACSIM (see Simucad) Compute Engine running MSIMON Compute Engine running MSPICE	Circuit Simulation Accelerator Circuit Simulation Accelerator Circuit Simulation Accelerator	Harris Semiconductor Mentor Graphics Mentor Graphics
	I-G Spice SPICE PLUS SABER S-SPICE ASPEC SIMON Microwave SPICE TOUCHSTONE 1.5 PRECISE PSpice (see MicroSim) MSIMON MSPICE HSPIICE RADSPICE SPICE/HSPIICE Interface MIXsim Lsim SPICE 2G.6 Interface HSPIICE (see Meta-Software) VTIspice	Circuit Simulator Circuit Simulator	A.B. Associates, Inc. Analog Design Tools Analogy Clarity Systems Control Data ECAD EEsof EEsof Electrical Engr'ng Software EXAR Mentor Graphics Mentor Graphics Meta-Software Meta-Software SDA Systems Sierra Semiconductor Silicon Compiler Systems Tektronix CAE Systems Tektronix CAE Systems VLSI Technology
	Aida CoSimulator Processor Aida PerSimulator Processor CATS (see HHB Systems) TESTGRADE-A Mach 1000F MX/MXT Fault/Logic Accelerator Fault Evaluator	Fault Simulation Accelerator Fault Simulation Accelerator Fault Simulation Accelerator Fault Simulation Accelerator Fault Simulation Accelerator Fault Simulation Accelerator Fault Simulation Accelerator	Aida Aida Case Technology Gateway Design Automation Silicon Solutions/Zycad XCAT Zycad
	Aida Fault Simulator Aida Fault Inferencer Probabalistic Fault Grading TCAT SOLO 1000/SOLO 1200 BITGRADE STATGRADE TESTGRADE MIMIC Fault Simulator HILO-3 CADAT (see HHB Systems) CADAT 6.0 QuickFault VISULA CADAT SILOS Interface TestEdge Lsim SILOS TANTEST HILO-3 (see Genrad)	Fault Simulator Fault Simulator	Aida Aida Caedent Calma ES2/US2 Gateway Design Automation Gateway Design Automation Gateway Design Automation GE Solid State Division Genrad Harris Semiconductor HHB Systems Mentor Graphics Racal-Redac SDA Systems SDA Systems Silicon Compiler Systems Simucad Tangent Systems Tektronix CAE Systems
	Layout Design System TopSet and GeoSet Harris/SDA Workstation CHIPGRAPH LAYOUT Generator Development Tools PRINCESS ChipTool VTIcustom	Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool Full Custom Layout Tool	Caeco Clarity Systems Harris Semiconductor Mentor Graphics SDA Systems Silicon Compiler Systems Silver-Lisco VIA Systems VLSI Technology
	MIDAS LDSIII Layout GATEGRAPH,GATEPLACE,GATEROUTE GARDS MERLYN-G	Gate Array Layout Tool Gate Array Layout Tool Gate Array Layout Tool Gate Array Layout Tool Gate Array Layout Tool	Control Data LSI Logic Mentor Graphics Silver-Lisco Tektronix CAE Systems
	ECAD GeoSet DRACULA II DRACULA III Harris/SDA Workstation REMED1 PDCHECK PDCOMPARE PDEXTRACT ERC Generator Development Tools Fast Mask Engine DVS VTIverify	IC Layout Verification IC Layout Verification	Calma Clarity Systems ECAD ECAD Harris Semiconductor Mentor Graphics SDA Systems SDA Systems SDA Systems SDA Systems SDA Systems Silicon Compiler Systems Silicon Solutions/Zycad Silver-Lisco VLSI Technology
	Aida CoSimulator Processor Aida PerSimulator Processor	Logic Simulation Accelerator Logic Simulation Accelerator	Aida Aida



Computing Platform	Design Automation Software	Function	Source
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DESIGN AUTOMATION—Hardware Vs. Software

Computing Platform	Design Automation Software	Function	Source
<b>Computing Platforms for Design Automation Software (Cont'd)</b>			
COMPUTER AUTOMATION (Cont'd)	Graphic System	Workstation	Drafting Dynamics
CONTROL DATA	Vanguard Stellar System PEPPER AutoMate Physical Design Sys.	Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool	Case Technology Control Data Royal Digital Systems
	I-G Spice ASPEC AutoMate Circuit Simulator	Circuit Simulator Circuit Simulator Circuit Simulator	A.B. Associates, Inc. Control Data Royal Digital Systems
	Fault Evaluator	Fault Simulation Accelerator	Zycad
	MIDAS TESTGRADE	Fault Simulator Fault Simulator	Control Data Gateway Design Automation
	Expediter Logic Evaluator System Development Engine	Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator	Zycad Zycad Zycad
	SALT MIDAS	Logic Simulator Logic Simulator	CAD Group, Inc. (CGI) Control Data
	AutoMate Schematic Capture	Schematic Capture	Royal Digital Systems
	Vanguard Stellar System MIDAS Gateway Design Automation AutoMate	Workstation Workstation Workstation Workstation	Case Technology Control Data Gateway Design Automation Royal Digital Systems
	HSPICE RADSPICE	Circuit Simulator Circuit Simulator	Meta-Software Meta-Software
	SALT	Logic Simulator	CAD Group, Inc. (CGI)
CONVEX	PEPPER AutoMate Physical Design Sys.	Circuit Board Layout Tool Circuit Board Layout Tool	Control Data Royal Digital Systems
	I-G Spice PRECISE HSPICE RADSPICE AutoMate Circuit Simulator	Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator	A.B. Associates, Inc. Electrical Engr'ng Software Meta-Software Meta-Software Royal Digital Systems
	Fault Evaluator	Fault Simulation Accelerator	Zycad
	FAIRCAD/PFault	Fault Simulator	Fairchild
	MERLYN-G	Gate Array Layout Tool	Tektronix CAE Systems
	Expediter Logic Evaluator System Development Engine	Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator	Zycad Zycad Zycad
	SALT TEGAS 5 FAIRCAD	Logic Simulator Logic Simulator Logic Simulator	CAD Group, Inc. (CGI) Calma Fairchild
	Microwave Harmonica AutoMate	Workstation Workstation	Compact Software Royal Digital Systems
	AutoMate Physical Design Sys.	Circuit Board Layout Tool	Royal Digital Systems
	ASPEC HSPICE AutoMate Circuit Simulator	Circuit Simulator Circuit Simulator Circuit Simulator	Control Data Meta-Software Royal Digital Systems
DATA GENERAL	Fault Evaluator	Fault Simulation Accelerator	Zycad
	CADAT (see HHB Systems) CADAT 6.0 SILOS	Fault Simulator Fault Simulator Fault Simulator	Harris Semiconductor HHB Systems Simucad
	CustomPlus GDSII	Full Custom Layout Tool Full Custom Layout Tool	Calma Calma
	DRACULA II	IC Layout Verification	ECAD
	Expediter Logic Evaluator System Development Engine Magnum	Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator	Zycad Zycad Zycad Zycad
	TEO/Electronics Simulator CADAT (see HHB Systems) CADAT 6.0 SILOS	Logic Simulator Logic Simulator Logic Simulator Logic Simulator	Data General Harris Semiconductor HHB Systems Simucad
	TEO/Electronics Design System AutoMate Schematic Capture	Schematic Capture Schematic Capture	Data General Royal Digital Systems
	GDSII/32 DS/7500 Workstation CADAT 6.0 AutoMate	Workstation Workstation Workstation Workstation	Calma Data General HHB Systems Royal Digital Systems
	Interactive/Automatic Layout Vanguard Stellar System AUTOART BOARDMASTER MICAD Intergraph Hybrid Design Printed Circuit Board Design OPTIMATE Place and Route	Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool	Applicon Case Technology Compact Software Daisy Systems EEsof Intergraph Intergraph Optima Technology

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Computing Platform	Design Automation Software	Function	Source
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Computing Platform	Design Automation Software	Function	Source
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DEC MicroVAX (Cont'd)			
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Computing Platform	Design Automation Software	Function	Source
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Computing Platform	Design Automation Software	Function	Source
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DESIGN AUTOMATION—Hardware Vs. Software

Computing Platform	Design Automation Software	Function	Source
<b>Computing Platforms for Design Automation Software (Cont'd)</b>			
ELXSI	KOLOA PCB Design System Crystal Router	Circuit Board Layout Tool Circuit Board Layout Tool	Shared Resources Shared Resources
	SIMON PRECISE USPICE Parallel SPICE 2G.5 HSPICE Parallel HSPICE RADSPICE MIXsim VTIspace	Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator	ECAD Electrical Engr'ng Software Electronic Software Products Elxsi Meta-Software Meta-Software Meta-Software Sierra Semiconductor VLSI Technology
	TESTGRADE-A	Fault Simulation Accelerator	Gateway Design Automation
	TESTGRADE CADAT (see HHB Systems) CADAT 6.0 SILOS	Fault Simulator Fault Simulator Fault Simulator Fault Simulator	Gateway Design Automation Harris Semiconductor HHB Systems Simucad
	VTIcustom	Full Custom Layout Tool	VLSI Technology
	DRACULA II DRACULA III Parallel DVS VTIverify	IC Layout Verification IC Layout Verification IC Layout Verification IC Layout Verification	ECAD ECAD Silvar-Lisco VLSI Technology
	SALT CADAT (see HHB Systems) CADAT 6.0 Circuit Pathfinder MIXsim SILOS VTIsim	Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator	CAD Group, Inc. (CGI) Harris Semiconductor HHB Systems Meta-Software Sierra Semiconductor Simucad VLSI Technology
	VTIschematic	Schematic Capture	VLSI Technology
	VTICellLib	Silicon Compiler	VLSI Technology
	VTIlogicComp	Standard Cell Layout Tool	VLSI Technology
	Gateway Design Automation CADAT 6.0 VTItools	Workstation Workstation Workstation	Gateway Design Automation HHB Systems VLSI Technology
HEWLETT-PACKARD	AUTOTOOLS AUTOART PC800 Model 4 Printed Circuit Design System	Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool	Aptos Systems Compact Software Gerber Scientific Instrument Hewlett-Packard
	SPICE PLUS Microwave SPICE TOUCHSTONE 1.5 PC Circuit Design Tools P Spice MIXsim VTIspace	Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator	Analog Design Tools EEsof EEsof Intusoft MicroSim Sierra Semiconductor VLSI Technology
	Precision Architecture Mach 1000F	Fault Simulation Accelerator Fault Simulation Accelerator	Hewlett-Packard Silicon Solutions/Zycad
	HILO-3 HILO-3 (see Genrad) CADAT 6.0	Fault Simulator Fault Simulator Fault Simulator	Genrad Hewlett-Packard HHB Systems
	VTIcustom	Full Custom Layout Tool	VLSI Technology
	VTIverify	IC Layout Verification	VLSI Technology
	Precision Architecture Mach 1000	Logic Simulation Accelerator Logic Simulation Accelerator	Hewlett-Packard Silicon Solutions/Zycad
	HILO-3 HILO-3 (see Genrad) CADAT 6.0 MIXsim VTIsim	Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator	Genrad Hewlett-Packard HHB Systems Sierra Semiconductor VLSI Technology
	HICHIP HICHIP (see Genrad)	Physical Modeler Physical Modeler	Genrad Hewlett-Packard
	81810S	Prototype IC Test System	Hewlett-Packard
	AnalogWorkbench Circuit Editor PC Workbench Circuit Editor Design Capture System VTIschematic	Schematic Capture Schematic Capture Schematic Capture Schematic Capture	Analog Design Tools Analog Design Tools Hewlett-Packard VLSI Technology
	VTICellLib	Silicon Compiler	VLSI Technology
	VTIlogicComp	Standard Cell Layout Tool	VLSI Technology
	Analog Workbench ICD-One RGRAPH CDX-3000/CDX-3150 Super-Compact PC800 Model 4 Electronic Design System CADAT 6.0 CustomEdge VTItools C2000	Workstation Workstation Workstation Workstation Workstation Workstation Workstation Workstation Workstation Workstation Workstation	Analog Design Tools Aptos Systems Aptos Systems Cadnetix Compact Software Gerber Scientific Instrument Hewlett-Packard HHB Systems SDA Systems VLSI Technology Zuken
IBM MAINFRAME/MINI	QWIKCHECK PRANCE	Circuit Board Layout Tool Circuit Board Layout Tool	Augat Automated Systems

DESIGN AUTOMATION—Hardware Vs. Software				
Computing Platform	Design Automation Software	Function	Source	
Computing Platforms for Design Automation Software (Cont'd)				
IBM MAINFRAME/MINI (Cont'd)	IPC Interactive PRANCE CT2500 AUTOART CIEDS/CBDS KOLOA PCB Design System Crystal Router	Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool	Cadarn Cadarn Case Technology Compact Software IBM Shared Resources Shared Resources	
	I-G Spice SABER ASPEC PRECISE USPICE CIEDS/Analog-Digital Simulator CIEDS/Switched Capacitor Sim. HSPICE RADSPICE	Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator	A.B. Associates, Inc. Analogy Control Data Electrical Engr'ng Software Electronic Software Products IBM IBM Meta-Software Meta-Software	
	Mach 1000F Fault Evaluator	Fault Simulation Accelerator Fault Simulation Accelerator	Silicon Solutions/Zycad Zycad	
	Digital Fault Simulation BITGRADE STATGRADE TESTGRADE MIMIC Fault Simulator HILO-3 CADAT (see HHB Systems) CADAT 6.0 COFIS Design Automation System SILOS	Fault Simulator Fault Simulator Fault Simulator Fault Simulator Fault Simulator Fault Simulator Fault Simulator Fault Simulator Fault Simulator Fault Simulator Fault Simulator	Cadarn Gateway Design Automation Gateway Design Automation Gateway Design Automation GE Solid State Division Genrad Harris Semiconductor HHB Systems Matra Design Systems National Semiconductor Simucad	
	PRINCESS	Full Custom Layout Tool	Silvar-Lisco	
	LDSIII Layout Design Automation System GARDS MERLYN-G	Gate Array Layout Tool Gate Array Layout Tool Gate Array Layout Tool Gate Array Layout Tool	LSI Logic National Semiconductor Silvar-Lisco Tektronix CAE Systems	
	DRACULA II DRACULA III Design Automation System	IC Layout Verification IC Layout Verification IC Layout Verification	ECAD ECAD National Semiconductor	
	VERILOG-XL Mach 1000 Expediter Logic Evaluator System Development Engine Magnum	Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator	Gateway Design Automation Silicon Solutions/Zycad Zycad Zycad Zycad Zycad	
	SALT Digital Circuit Simulation TEGAS 5 TEXSIM/B VERILOG VERILOG-XL MIMIC Logic Simulator HILO-3 CADAT (see HHB Systems) CADAT 6.0 CIEDS/Analog-Digital Simulator CIEDS/Behavioral Simulator CIEDS/Logic Simulator LSIM/LDEL Design Automation System HELIX LOGSIM SILOS	Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator Logic Simulator	CAD Group, Inc. (CGI) Cadarn Calma Calma Gateway Design Automation Gateway Design Automation GE Solid State Division Genrad Harris Semiconductor HHB Systems IBM IBM IBM LSI Logic National Semiconductor Silvar-Lisco Silvar-Lisco Simucad	
	HICHIP	Physical Modeler	Genrad	
	PALASM2	Programmable Device Development System	Monolithic Memories	
	CADEX CIEDS/Design Capture LSED (LSI Logic Schematic Ed.) Design Automation System	Schematic Capture Schematic Capture Schematic Capture Schematic Capture	Cadarn IBM LSI Logic National Semiconductor	
	LDSIII Cell Layout Design Automation System CAL-MP MERLYN-S	Standard Cell Layout Tool Standard Cell Layout Tool Standard Cell Layout Tool Standard Cell Layout Tool	LSI Logic National Semiconductor Silvar-Lisco Tektronix CAE Systems	
	Super-Compact EDGE Gateway Design Automation CADAT 6.0 CIEDS Des. Cap./Sim. for RT PC CIEDS/Design Capture for PC/AT LDS ASIC Design System Design Automation System SL2000	Workstation Workstation Workstation Workstation Workstation Workstation Workstation Workstation Workstation	Compact Software Electronic Software Products Gateway Design Automation HHB Systems IBM IBM LSI Logic National Semiconductor Silvar-Lisco	
	IBM PC/XT/AT	AUTOTOOLS QWIKDRAW WRAPID PRANCE/SIGMA REMOTE PCB/DE Pathfinder	Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool	Aptos Systems Augat Augat Automated Systems B&C Microsystems Bishop Graphics



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Computing Platform	Design Automation Software	Function	Source
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IRM PC/YT/AT (Cont'd)			
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DESIGN AUTOMATION—Hardware Vs. Software

Computing Platform	Design Automation Software	Function	Source
<b>Computing Platforms for Design Automation Software (Cont'd)</b>			
IBM PC/XT/AT (Cont'd)	KAD System	Workstation	Kontron
	PDS 2400 Automated Wiring Sys	Workstation	M2M Robotics
	MDS	Workstation	Matra Design Systems
	Linear CAD II	Workstation	Micro Linear
	MCAD	Workstation	Micro Power Systems
	Design Automation System	Workstation	National Semiconductor
	CAE-1	Workstation	P-CAD
	CAE-2	Workstation	P-CAD
	EDA-1	Workstation	P-CAD
	PCB-1	Workstation	P-CAD
	PCB-2	Workstation	P-CAD
	PCB-3	Workstation	P-CAD
	REDCAD	Workstation	Racal-Redac
	REDSIM	Workstation	Racal-Redac
	VISULA 3.0	Workstation	Racal-Redac
	AutoMate	Workstation	Royal Digital Systems
	SCIDESIGN	Workstation	Scientific Calculations
	STANSURE	Workstation	Standard Microsystems Corp.
	Analog Design System	Workstation	Valid Logic Systems Inc.
	Design Entry System	Workstation	Valid Logic Systems Inc.
	Logic Design System	Workstation	Valid Logic Systems Inc.
	Design Validation System	Workstation	Valid Logic Systems Inc.
	Personal Design Station	Workstation	Vectron Graphics
	Workview 1.2	Workstation	Viewlogic Systems
	EE Designer	Workstation	Visionics
	Electronic CAD Software Tools	Workstation	Wintek
	MX/MXT/HSE Logic/Fault Accel.	Workstation	XCAT
	ZyP-AT	Workstation	ZyMOS
MASSCOMP	PCB Design	Circuit Board Layout Tool	Vectron Graphics
	PACSIM (see Simucad)	Circuit Simulation Accelerator	Harris Semiconductor
	SLICE	Circuit Simulator	Harris Semiconductor
	SPICE/HSPICE Interface	Circuit Simulator	SDA Systems
	CATS Accelerator	Fault Simulation Accelerator	HHB Systems
	CADAT (see HHB Systems)	Fault Simulator	Harris Semiconductor
	CADAT 6.0	Fault Simulator	HHB Systems
	SILOS Interface	Fault Simulator	SDA Systems
	TestEdge	Fault Simulator	SDA Systems
	SILOS	Fault Simulator	Simucad
	Harris/SDA Workstation	Full Custom Layout Tool	Harris Semiconductor
	LAYOUT	Full Custom Layout Tool	SDA Systems
	Harris/SDA Workstation	IC Layout Verification	Harris Semiconductor
	PDCHECK	IC Layout Verification	SDA Systems
	PDCOMPARE	IC Layout Verification	SDA Systems
	PDEXTRACT	IC Layout Verification	SDA Systems
	ERC	IC Layout Verification	SDA Systems
	CATS Accelerator	Logic Simulation Accelerator	HHB Systems
	CADAT (see HHB Systems)	Logic Simulator	Harris Semiconductor
	CADAT 6.0	Logic Simulator	HHB Systems
	SILOS Interface	Logic Simulator	SDA Systems
	Timing Analyzer	Logic Simulator	SDA Systems
	SILOS	Logic Simulator	Simucad
	CATS Modeler	Physical Modeler	HHB Systems
	Harris/SDA Schematic Capture	Schematic Capture	Harris Semiconductor
	Schematic Editor	Schematic Capture	SDA Systems
	Compilers	Silicon Compiler	Harris Semiconductor
	Structure Compiler	Silicon Compiler	SDA Systems
	Module Generation Development	Silicon Compiler	SDA Systems
	Harris/SDA Workstation	Standard Cell Layout Tool	Harris Semiconductor
	Place and Route	Standard Cell Layout Tool	SDA Systems
	Harris/SDA Workstation	Workstation	Harris Semiconductor
	CADAT 6.0	Workstation	HHB Systems
	CustomEdge	Workstation	SDA Systems
	Design Framework	Workstation	SDA Systems
	Stand Alone Design Station	Workstation	Vectron Graphics
MOTOROLA	PC	Circuit Board Layout Tool	Drafting Dynamics
	PC800 Model 4	Circuit Board Layout Tool	Gerber Scientific Instrument
	Graphic System	Workstation	Drafting Dynamics
	PC800 Model 4	Workstation	Gerber Scientific Instrument
	PDS 2400 Automated Wiring Sys	Workstation	M2M Robotics
NEC PC	Vanguard Stellar System	Circuit Board Layout Tool	Case Technology
	Dasoft-16	Circuit Board Layout Tool	Dasoft Design Systems
	PSpice	Circuit Simulator	MicroSim
	DRACULA II	IC Layout Verification	ECAD
	SCEPTRE II	IC Layout Verification	Gould Semiconductor Division
	SALT	Logic Simulator	CAD Group, Inc. (CGI)
	SCEPTRE II	Logic Simulator	Gould Semiconductor Division
	CUPL	Programmable Device Development System	P-CAD
	Vanguard Stellar System	Schematic Capture	Case Technology
	SCEPTRE II	Standard Cell Layout Tool	Gould Semiconductor Division
	CT2000	Workstation	Case Technology
	Vanguard Stellar System	Workstation	Case Technology

DESIGN AUTOMATION—Hardware Vs. Software			
Computing Platform	Design Automation Software	Function	Source
<b>Computing Platforms for Design Automation Software (Cont'd)</b>			
NEC PC (Cont'd)	Dasoft-16	Workstation	Dasoft Design Systems
PRIME	AutoMate Physical Design Sys. Crystal Router	Circuit Board Layout Tool Circuit Board Layout Tool	Royal Digital Systems Shared Resources
	I-G Spice HSPICE RADSPICE AutoMate Circuit Simulator CIRCUIT	Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator	A.B. Associates, Inc. Meta-Software Meta-Software Royal Digital Systems The Western Design Center
	Fault Evaluator	Fault Simulation Accelerator	Zycad
	Expediter Logic Evaluator System Development Engine	Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator	Zycad Zycad Zycad
	AutoMate Logic Simulator LOGIC	Logic Simulator Logic Simulator	Royal Digital Systems The Western Design Center
	AutoMate Schematic Capture	Schematic Capture	Royal Digital Systems
	AutoMate	Workstation	Royal Digital Systems
	CADAT (see HHB Systems) LDSIII Layout	Fault Simulator Gate Array Layout Tool	Harris Semiconductor LSI Logic
	CADAT (see HHB Systems) LSIM/LDEL	Logic Simulator Logic Simulator	Harris Semiconductor LSI Logic
PYRAMID	LSED (LSI Logic Schematic Ed.)	Schematic Capture	LSI Logic
	LDSIII Cell Layout	Standard Cell Layout Tool	LSI Logic
	LDS ASIC Design System	Workstation	LSI Logic
RAMTEK	LDSIII Layout	Gate Array Layout Tool	LSI Logic
RIDGE	AUTOART	Circuit Board Layout Tool	Compact Software
	ASPEC MIXsim VTIspice	Circuit Simulator Circuit Simulator Circuit Simulator	Control Data Sierra Semiconductor VLSI Technology
	Fault Evaluator	Fault Simulation Accelerator	Zycad
	HILO-3	Fault Simulator	Genrad
	VTIcustom	Full Custom Layout Tool	VLSI Technology
	DRACULA II VTIverify	IC Layout Verification IC Layout Verification	ECAD VLSI Technology
	Expediter Logic Evaluator System Development Engine	Logic Simulation Accelerator Logic Simulation Accelerator Logic Simulation Accelerator	Zycad Zycad Zycad
	SALT HILO-3 MIXsim VTIsim	Logic Simulator Logic Simulator Logic Simulator Logic Simulator	CAD Group, Inc. (CGI) Genrad Sierra Semiconductor VLSI Technology
	HICHIP	Physical Modeler	Genrad
	VTIschematic	Schematic Capture	VLSI Technology
	VTIcellLib	Silicon Compiler	VLSI Technology
	VTIlogicComp	Standard Cell Layout Tool	VLSI Technology
	Super-Compact VTITools	Workstation Workstation	Compact Software VLSI Technology
SUN	Vanguard Stellar System AUTOART MiCAD AutoMate Physical Design Sys. KOLOA PCB Design System Crystal Router Allegro	Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool Circuit Board Layout Tool	Case Technology Compact Software EEsof Royal Digital Systems Shared Resources Shared Resources Valid Logic Systems Inc.
	PACSIM (see Simucad)	Circuit Simulation Accelerator	Harris Semiconductor
	I-G Spice SPICE PLUS SABER CDX-3200 PSpice (see MicroSim) SIMON Microwave SPICE TOUCHSTONE 1.5 PRECISE SLICE HSPICE RADSPICE PSpice AutoMate Circuit Simulator SPICE/HSPICE Interface MIXsim Lsim VTIspice	Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator Circuit Simulator	A.B. Associates, Inc. Analog Design Tools Analog Cadnetix Case Technology ECAD EEsof EEsof Electrical Engr'ng Software Harris Semiconductor Meta-Software Meta-Software MicroSim Royal Digital Systems SDA Systems Sierra Semiconductor Silicon Compiler Systems VLSI Technology
	Aida CoSimulator Processor CATS (see HHB Systems) CATS Accelerator Mach 1000F	Fault Simulation Accelerator Fault Simulation Accelerator Fault Simulation Accelerator Fault Simulation Accelerator	Aida Case Technology HHB Systems Silicon Solutions/Zycad



Computing Platform	Design Automation Software	Function	Source
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4650-C

Computing Platform	Design Automation Software	Function		Source	
		Function	Source	Function	Source

SUN (Cont'd)			SDA Systems
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[illegible]



# CAE WORKSTATION

- Mixed-mode design entry allows you to describe your circuit using any combination of schematics, equations, truth tables, or state diagrams.
- Automatic logic synthesis eliminates redundant circuitry and optimizes your design for size/speed trade-offs.
- Design simulation allows you to easily verify complex circuits with the speed and computational power of a mainframe, for a fraction of the price.
- An open architecture allows you to easily integrate your FutureNet workstation into your engineering environment.



FutureNet® is your complete source for CAE. To build a system, start with FutureDesigner™ and describe your circuit with any combination of schematics, equations, truth tables, or state diagrams. FutureDesigner is the only advanced design entry workstation that lets you describe your circuit in compact, high-level terms and create more complex designs faster. Then, use DASH-CADAT Plus to simulate logic, timing, and circuit faults with the speed and power of a mainframe. For analog designs, DASH-Analog Workbench™ allows you to breadboard in software, before you build a hard prototype. FutureNet's powerful CAE tools are described below.

## **FUTUREDESIGNER:**

FutureDesigner is a new design entry system, substantially different from any other system on the market. Its sophisticated new design techniques, such as logic synthesis, eliminate the time-consuming parts of the design entry process, allowing you to work more productively.

With FutureDesigner, you can describe your circuit with any combination of structural and behavioral representations. Use schematics to enter the structural portions of the design, such as data paths or memory arrays. For portions easier to describe behaviorally, like sequencers or decoders, simply enter equations, truth tables or state diagrams using on-screen input forms.

For the behavioral portions of your design, use FutureDesigner as a "what if" tool to try different design approaches. Immediately verify that your circuit works as you intended. For the structural portions, design check tools detect and help you correct connectivity and other common design errors. Together these features significantly shorten the design iteration cycle.

Once you've entered equations, state diagrams or truth tables, FutureDesigner's logic synthesizer eliminates redundant circuitry and optimizes your design for size/speed trade-offs. FutureDesigner is the only design entry workstation that will then automatically produce the correct schematics and integrate them with the total structural design.

## **DASH-CADAT PLUS:**

DASH-CADAT Plus allows you to verify complex circuits easily. It not only speeds logic development, it helps you ensure your designs are 100% testable. DASH-CADAT Plus is ideally suited for verifying application-specific integrated circuit (ASIC) designs, as well as designs using standard parts and programmable logic devices (PLDs). DASH-CADAT Plus can simulate ASIC designs up to 35,000 gates, with the speed and computational power of a mainframe at a fraction of the cost.

## **DASH-ANALOG WORKBENCH:**

DASH-Analog Workbench lets you design your analog circuit and do breadboarding in software, before you build a hard prototype. You'll interact with the simulator using interfaces that are as familiar to you as test instruments — an oscilloscope, network analyzer, function generator and frequency sweeper. Optional modules add advanced capabilities such as parametric plotting, statistical analysis and more.

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## FutureNet

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# **TOPAZ HIGH SPEED ASIC VERIFICATION**

## **EVALUATES COMPLEX ASIC PROTOTYPES IN REAL-TIME**



### **TOPAZ PROVIDES A TOTAL SOLUTION**

The Topaz VLSI Design Verification System delivers the horse-power needed to evaluate complex custom and semi-custom ICs, including VHSIC devices.

These are real time systems which accept test vectors from a CAE workstation, stimulate the device under test (DUT) and compare the output vectors with the predicted response. Extensive post-processing routines aid diagnostics by analyzing failure data.

### **UNMATCHED FLEXIBILITY AND PERFORMANCE**

The Topaz systems are available in several versions for convenient price/speed tradeoff. All models feature complete capability at the full test rate across all 288 signal pins. Topaz systems provide high resolution edge placement, I/O control, and real-time compare without sacrificing either test rate or pin count.

### **HIGH PERFORMANCE FEATURES**

- 50MHz Data Rates with Real-Time Compare
- Up to 288 Signal Pins
- 100ps Picosecond Timing Resolution
- Programmable Driver/Receivers with 10mV Resolution
- Six Programmable Data Formats
- Dynamic I/O Control
- Programmable Edge or Window Compare Modes

MODEL SELECTION GUIDE		
TEST RATE	TOPAZ MODEL	TIMING RESOLUTION
25MHz	TOPAZ-25	500ps
30MHz	TOPAZ-FX	500ps
50MHz	TOPAZ-50	500ps
50MHz	TOPAZ-II	100ps

- 4K, 16K, or 64K Stimulus/Expected Response Vector Depth
- DC Parametric Measurements
- LSSD Test Option
- Interactive Control of Stimulus/Expected Response Patterns
- Error Bit Mapping
- High Performance Logic Analysis for Fault Diagnostics
- 4 Nanosecond Glitch Capture
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## Modular Design Environment™

### Description

LSI Logic's Modular Design Environment (MDE™) is the industry's most advanced and proven array and cell-based design system from the leader in ASIC technologies. MDE software products and third party offerings—CAE design tools as well as testers and accelerators—can meet any ASIC design requirement and run in almost any workstation or mainframe environment. The MDE Integrator™ Series—the Logic Integrator™, Silicon Integrator™ and System Integrator™—offers a diversity of high performance graphic and non-graphic design entry tools and standard TTL, LSI, VLSI and proprietary technology libraries. Integrator Series packages accommodate channeled and Channel-Free™ array designs and feature full upward and downward compatibility. The entry-level single-chip Logic Integrator is for designs with complexities up to 6700 gates. It can be traded up for Silicon Integrator modules for building ASICs with 7,000 to 100,000 usable gates. The Silicon Integrator is easily coupled to the System Integrator's multi-chip mixed-mode simulation capabilities. The Integrator Series operates from a variety of popular

hardware platforms including stand-alone workstations, distributed minicomputer networks and mainframe-based systems. Another path to MDE is LSI Logic's CAD Connection Program, which links licensed third party CAE design environments to MDE tools.

Highly integrated yet expandable MDE configurations incorporate optional silicon compilers, logic synthesis, hardware accelerators, behavioral model libraries, PAL converters as well as automated schematic and production test pattern generators. Modular construction allows migration into leading-edge technologies and anticipates emerging CAE standards. MDE also links the design environment to LSI Logic wafer fabs that guarantee accuracy with a right-the-first-time record for over 4,000 successful MDE designs. LSI Logic MDE offerings include software and technology training, a user hotline, complete documentation, system consulting and maintenance. MDE tools are also available through LSI Logic's global Design Resource Center network.

### MDE Integrator Series System/ASIC Design Flow

Compilation	Design Entry	Pre-Simulation Analysis	Simulation	Systems Modeling	Post Simulation Analysis
Logic Synthesizer	Schematic Editor	Path Timing Analyzer	LDS® Simulator	Multi-Chip Behavioral Simulator	Waveform Editor
PAL Synthesizer	Waveform Editor	Delay Prediction	Accelerated Logic Simulator	Standard Product Gate modeling	Path Timing Analyzer
Logic Compilers	Schematic Builder	Chip Planning	Accelerated Fault Simulator		Power Analyzer
Multiplier Compiler	Netlist Description Language		Multi-ASIC Logic Simulator		Package Planning
Memory Compiler	Simulation Control Language		Behavioral Simulator		
	Behavioral Specification Language		Test LSI		

*The Integrator Series System/ASIC Design Flow lists the MDE modules available for each design step. The Logic Integrator, Silicon Integrator and System Integrator design packages each include a subset of these modules as standard and optional offerings.*

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## Modular Design Environment

### CAD Connection Program Overview

The **CAD Connection Program** extends LSI Logic's Modular Design Environment (MDE) capabilities to remote CAD/CAE environments with ASIC design kits that run on most popular workstations. The ASIC design kits are developed to LSI Logic specifications and maintained by original CAD/CAE system suppliers and manufacturers under license to LSI Logic. The design kits link stand-alone CAD systems to LSI Logic's foundry-integrated MDE tools and databases. Design kits feature macrocell libraries for channeled or Channel-Free HCMOS arrays, including the LL7000, LL9000, the LMb6000 and LMA9000 Series. Using generic tools with specialized libraries and features such as post-layout wirelength back-annotation, customers build designs on their in-house CAE system. Verified design interface files are automatically generated for transfer to an LSI Logic Design Resource Center for final MDE design processing and fabrication. CAE manufacturer development assures

that the LSI Logic design kit blends into the customer's design environment. Close integration of remote design tools with LSI Logic layout and fabrication allows reliable "right-the-first-time" design accuracy. Designs are certified by LSI Logic's Modular Design Environment before they are committed to silicon and are guaranteed to function according to designer specification.

A variety of design kits are available for most commercial CAE products (see CAD Connection Design Kit Matrix table). A full CAD connection design kit includes schematic capture, simulation with accurate delays, post-layout back-annotation, error checking and design/test vector interface to MDE via an LSI Logic Design Resource Center. This product support is aimed at customers who intend to design low to medium complexity ASICs using general purpose third party CAE design tools.

### Features

- CAD connection integrates the ASIC design flow using Customer in-house third party CAE environment LSI Logic Design Resource Centers, manufacturing and test facilities
- Design kits bring silicon-specific performance to general purpose CAE systems
- CAE manufacturer develops and maintains design kit as integral part of customer's in-house CAE environment
- LSI Logic ASIC technology specs and kit certification ensure MDE compatibility, accuracy
- Expert support from CAE manufacturer and LSI Logic

### Design Kits

A full CAD connection certified design kit includes

- Macrocell symbol library
- Macrocell models
- Timing libraries
- Delay calculation tools
- Design verification tools
- Netlist and test vector interface programs
- Back-annotation programs
- Documentation from the licensee and from LSI Logic

### LSI Logic CAD Connection Design Kit Matrix

	AIDA	CADnetix	CASE	Daisy	FutureNet	Ikos	Mentor	Tektronix	Valid	ViewLogic
Macrocell Symbol Library	✓	✓	✓	✓	✓		✓	✓	✓	✓
Macrocell Models	✓	✓		✓		✓	✓	✓	✓	✓
Timing Libraries	✓	✓		✓		✓	✓	✓	✓	✓
Delay Calculation Tools	✓	✓		✓		✓	✓	✓	✓	✓
Design Verifier Tools	✓	✓		✓		✓	✓	✓	✓	✓
Interface Programs (Netlist/Test Vectors)	✓	✓		✓		✓	✓	✓	✓	✓
Back-Annotation Programs	✓	✓				✓	✓	✓	✓	✓
Full Documentation	✓	✓		✓		✓	✓	✓	✓	✓

† LSI Logic Software DataBook and Design Verifier offerings are subsumed by the CAD Connection Program.

Note: This table identifies CAE vendors currently active in the CAD Connection Program. It is subject to change. Please contact the factory for an updated list of certified CAE vendors.



## Modular Design Environment

### MDE Integrator Series Platforms

#### Mainframes

IBM

DEC VAX series

#### Workstations

Sun Microsystems 3 series, 4 series

DEC

VAX Station II, MicroVAX GPX-II

Apollo

DN3000, DN570, DN580, DN590, DN4000

VM/CMS

VMS

Sun UNIX

VMS

DOMAIN IX

See your LSI Logic representative for specific configurations and availability.

*The Integrator Series runs in nearly any CAE environment. The Logic Integrator runs on Sun Microsystems 3 and 4 series only. Graphics tools are supported only on Sun Microsystems Workstations.*

### Logic Integrator Overview

The **Logic Integrator** is an economical, entry-level system containing the design and simulation tools for creating single ASIC chips on any Sun 3/UNIX system. Optimized for graphic entry and multi-window tasking, the Logic Integrator boosts CAE productivity for 0.9-micron channel length (1.5-micron drawn gate length) Channel-Free™ HCMOS designs using LSI Logic's LMb6000 Micro bASIC™ technology. The versatile low-end LMb6000 libraries contain hundreds of industry standard logic elements that support designs within a range of 700 to 6700 usable gates.

The Logic Integrator was created as a low-cost entry to LSI Logic's Modular Design Environment that allows ASIC designers to upgrade to more powerful tools and to emerging technologies. A modular expansion path provides application and design portability to a variety of hardware platforms as well as upgrades to dense array technologies and mixed-mode behavioral and gate-level multi-chip simulation. The standard configuration offers near-mainframe design performance with these high-end tools: schematic capture, waveform editor, graphic entry and editing of simulation test patterns, interactive (single-chip) simulation, design verification and production test pattern extraction.

### Features

- Graphic schematic editing with advanced automated features
- Graphic waveform logic editing for precise interactive simulation of all or part of a design
- Automatic extraction of production test program, including patterns to evaluate timing sensitivity
- LMb6000 Macrofunction and Macrocell Library—a diverse set of SSI and MSI building blocks
- Silicon specific designs for a flawless design-to-fab transfer and ASIC performance to simulation specifications
- Upgrade path to Silicon Integrator and System Integrator tools
- PAL-to-ASIC cell conversion software

## Modular Design Environment

### Silicon Integrator Overview

The **Silicon Integrator** is a comprehensive single-chip design system for creating LSI Logic ASICs. Designed to run on high-performance multi-tasking computers, the Silicon Integrator features interactive, event-driven simulation and one of the most extensive ASIC cell library sets in the industry. Graphics and multiple windows provide a high productivity CAE environment. Non-graphic support on popular mainframes extends Silicon Integrator availability to cover most high-power computer hardware in use today. A flexible modular system, the Silicon Integrator anticipates a wide variety of user needs with standard features and add-on capabilities such as silicon compilation, chip planning, hardware acceleration and PAL-to-ASIC cell conversion. The standard configuration includes the following modules: schematic capture, waveform editor, single chip simulator, test program extraction, path timing analysis, power analysis and schematic builder. Customers can select optional library support for specific applications. A toolset designed specifically for LSI Logic silicon technology makes the Silicon Integrator foundry specific.

ety of user needs with standard features and add-on capabilities such as silicon compilation, chip planning, hardware acceleration and PAL-to-ASIC cell conversion. The standard configuration includes the following modules: schematic capture, waveform editor, single chip simulator, test program extraction, path timing analysis, power analysis and schematic builder. Customers can select optional library support for specific applications. A toolset designed specifically for LSI Logic silicon technology makes the Silicon Integrator foundry specific.

### Features

- Precise gate-level simulation with back-annotated wire-lengths—guarantees ASIC performance, eliminates breadboarding
- Extensive HCMOS library support is available to satisfy almost any technology requirement:
  - Macrocell Libraries**—hundreds of fully characterized SSI and MSI logic cells for device families from 700-gate channeled arrays to 100K-gate Compacted Arrays™ as well as Cell-Based HCMOS ASICs
  - Megafunction and Megacell Libraries** (optional library set)—more than 100 complex LSI and VLSI building blocks including industry-standard parts and proprietary LSI Logic functions
- Automatic error checking and reporting catches design problems early, enhances productivity and manufacturability
- Automatic test program formatting for industry standard test equipment
- Add-on-capabilities
  - Silicon Compilers
  - Multi-ASIC Gate-Level Simulator
  - Behavioral Simulator
  - Hardware Accelerated Logic and Fault Simulators
  - Automatic Test Pattern Generator for scan-based synchronous circuits
  - Chip Planner
  - Package Planner

### System Integrator Overview

The **System Integrator** is an advanced and flexible package for designing, simulating and analyzing entire systems. Graphic or non-graphic versions run on a variety of hardware platforms from single-user workstations to minis and mainframes. A multi-chip mixed-mode (for either standard and/or ASIC chips) simulation at the gate and behavioral levels offers precise, interactive electronic breadboarding of technology-diverse systems. System Integrator technology libraries contain gate-level models for standard TTL functions as well as behavioral models for LSI and VLSI functions. An optional library includes behavioral models for the AMD Bit-Slice 29000,

Motorola 68000, and Intel 8000/8200 microprocessor families.

Optional system-level hardware acceleration and standard graphic schematic entry, waveform editing and a structured behavioral modeling language bring unsurpassed CAE productivity to the multi-chip mixed-mode ASIC design process. The System Integrator's modular architecture assures integration across the entire spectrum of LSI Logic design tools and technology libraries, close coupling to LSI Logic wafer fabs and a direct path to emerging design technologies.

### Features

- Accurate, interactive simulation of heterogeneous systems eliminates breadboarding, speeds design implementation of complex systems
- Behavioral modeling language and gate-modeling tools allow broad-based VLSI and TTL design and simulation capability
- Hardware platform versatility to fit almost any standard design environment
- Integration to single-chip LSI Logic design tools (optional) and prototype implementation
- Migration to advanced design technologies for higher performance and densities



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3

# The Full Custom WorkSystem™ Lets You Handcraft High Performance.

IN A SERIES

**Tektronix  
Aided  
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With Tektronix, you've got custom design power well in hand, thanks to the Full Custom WorkSystem.

Developed by Tektronix as part of Tektronix Aided Engineering, the Full Custom WorkSystem combines custom design capture, simulation and layout tools into one powerful solution.

You get the Designer's Database Schematic Capture (DDSC™), logic and circuit simulation, LEIA™ custom IC and hybrid layout editor and DRACULA™ IC mask verification and fracturing tool. All in the same performance-driven design environment.

DDSC provides you with a fast, user-customizable, menu-driven system for design capture of custom IC schematics.

When it's time for layout, you can do so with more design freedom using LEIA, our powerful interactive graphical layout editor. LEIA is especially suited for custom analog bipolar as well as gallium arsenide microwave applications.

Its flexible user interface provides you with multiple windows, macros, pop-up menus and the ability to customize real-time, user-configurable menus. LEIA also provides unparalleled support for hierarchical design and all-angle geometries.

What's more, LEIA's direct read and write of Calma GDSII™ structures speeds the integration of your design into verification and production software, including existing CAD systems.

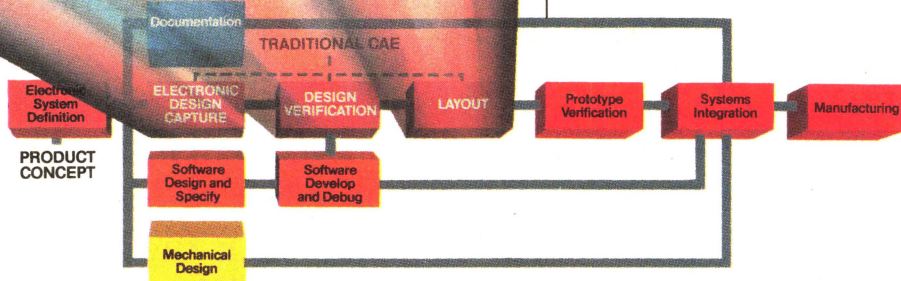
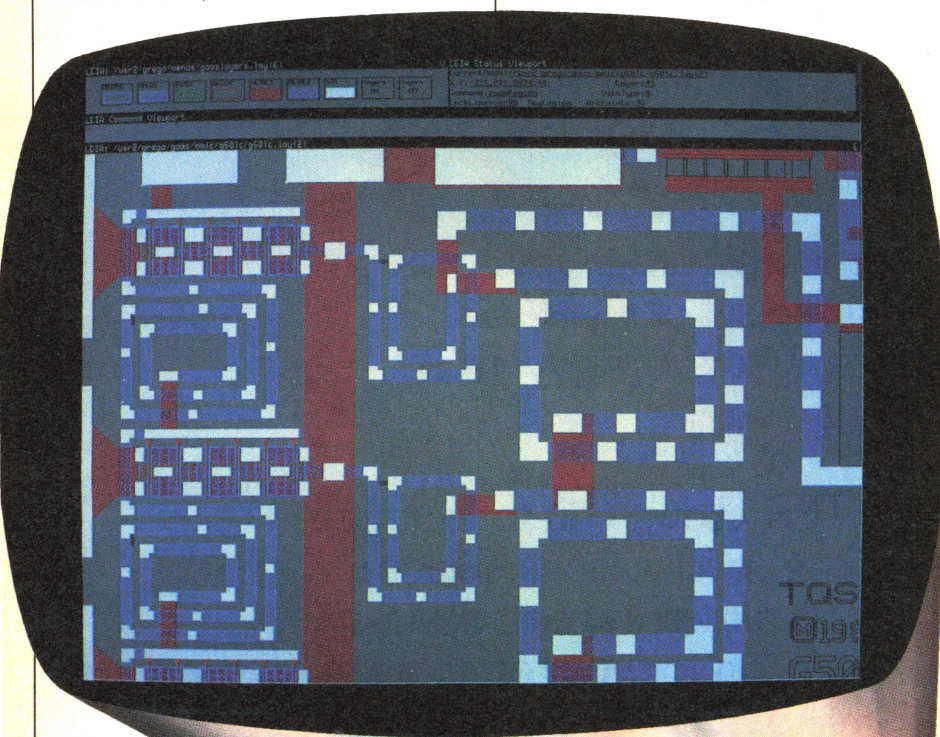
Before you fabricate your custom circuit, you can use DRACULA integrated software to verify your IC mask layout.

DRACULA let you measure and display design rule checker errors, extract parasitic electrical parameters and compare your layout to your schematic. So you can ensure total design integrity before you commit to fabrication. DRACULA's advanced fracture algorithms lower mask-making costs by greatly reducing flash count.

The Full Custom WorkSystem is part of Tektronix Aided Engineering. A family of integrated WorkSystems that takes you beyond traditional CAE solutions. And into prototype verification, software development and testing, systems integration, mechanical design and manufacturing. All running on industry-standard hardware platforms.

Best of all, it's from Tektronix. The name you've always trusted to get the engineering job done. So you're assured of worldwide service, support and training.

If you'd like to try your hand at high performance with the Full Custom WorkSystem, contact your local Tektronix, CAE Systems Division, sales office. Or call 800/547-1512. Tektronix, CAE Systems Division, P.O. Box 4600, Beaverton, OR 97076.



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# 4 The Gate Array WorkSystem™ Makes Layout As Easy As Pushing A Button.

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AUTOMATED  
**PUSH**  
LAYOUT

Now logic designers can control the entire physical layout of gate array designs. From a single schematic entry environment. Just by pushing a button.

Developed by Tektronix as part of Tektronix Aided Engineering, the Gate Array WorkSystem eliminates the need for IC layout expertise. Because it gives you everything you need to quickly develop ASIC vendor-certified layouts.

And since you're controlling the layout from the schematic, you can tune your design using iterations of simulation and automatic layout to achieve your performance requirements.

The Gate Array WorkSystem creates a unique, performance-driven design environment integrating Designer's Database Schematic Capture (DDSC™) and industry-standard HILO®-3 logic simulation with MERLYN-G™ automatic physical layout.

The system also introduces vendor-certified TurnChip® ASIC Layout Modules for knowledge-based, automatic control of MERLYN-G layout of specific array families.

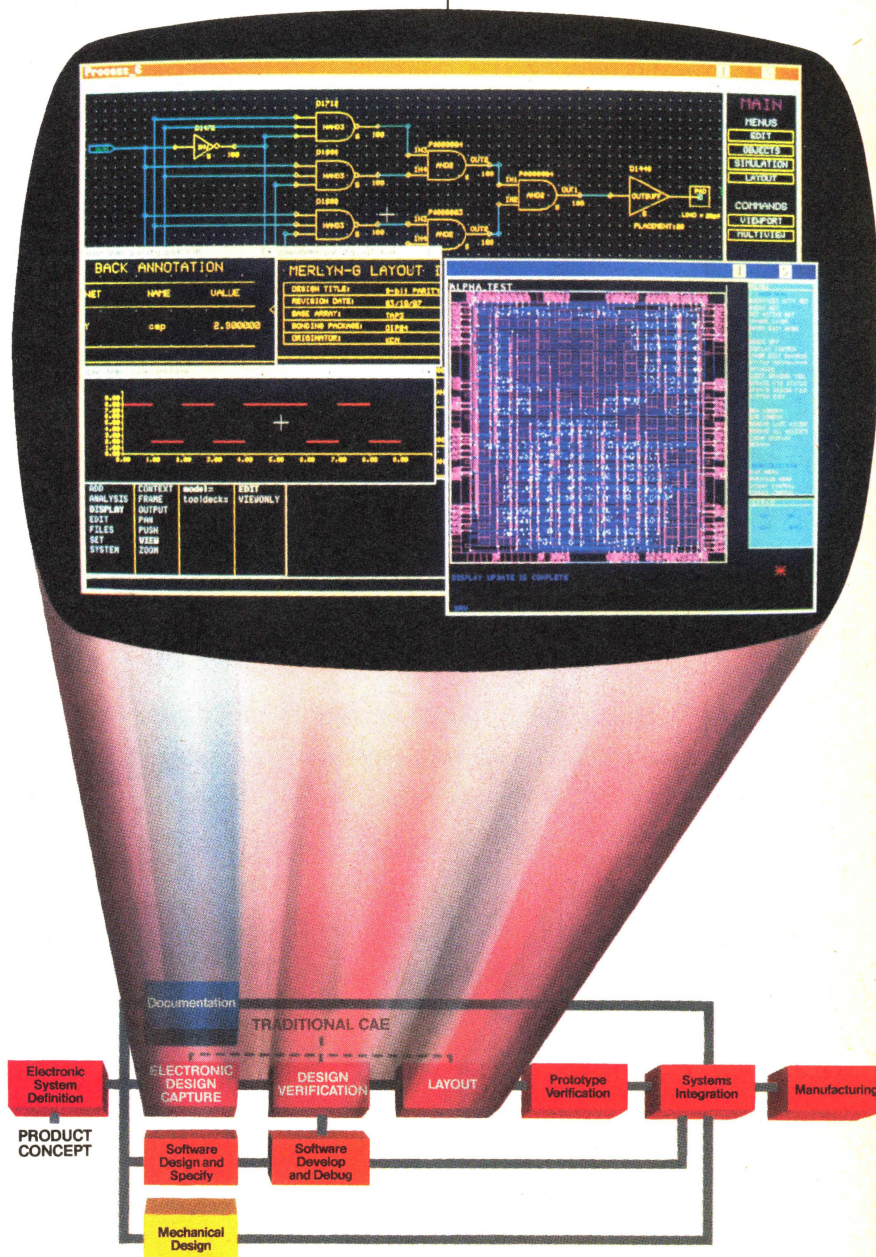
Layout so automated you can place and route a 5000-gate array 100% automatically. Just by pushing a button. With results so accurate that your layout is ASIC vendor-endorsed.

Using TurnChip modules, you can generate ASIC vendor-certified layout designs, then send them directly to the ASIC vendor. Which cuts your design time, lowers your costs and delivers complete control of your sensitive design data.

It's all part of Tektronix Aided Engineering. Integrated WorkSystems that take you beyond traditional CAE solutions. And into prototype verification, software development and testing, systems integration, mechanical design and manufacturing. All running on industry-standard platforms from Apollo® and DEC™. Best of all, it's from Tektronix. The name

you've always trusted to get the engineering job done. So you're assured of worldwide service, support and training.

If you'd like to take control of physical layout, contact your local Tektronix, CAE Systems Division, sales office. Or call 800/547-1512. Tektronix, CAE Systems Division, P.O. Box 4600, Beaverton, OR 97076-4600.



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Valid is now the only electronic design automation vendor to offer systems designers the full spectrum of CAE, IC CAD, and PCB CAD tools on Sun workstations.

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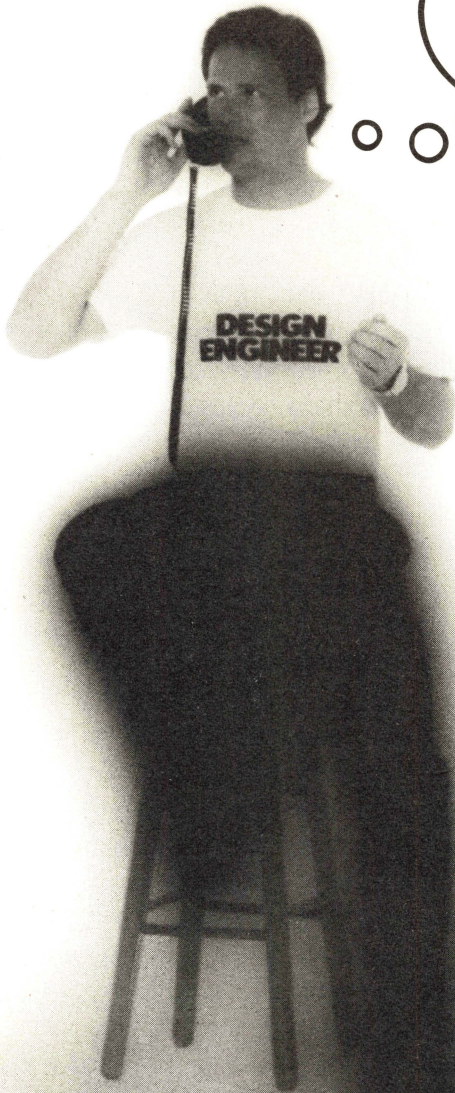


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...POWER!...DELAYS!...  
...REFLECTIONS!...





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...LINE WIDTH?...PLACEMENT?...  
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The solution to this confusion is Rules Driven Design, Valid's new methodology for integrating CAE with IC/PCB design. Simply put, it communicates the design engineer's intentions to the layout designer at the beginning.

Using Rules Driven Design, engineers capture more than a schematic — they capture design intentions which help guide the layout of the critical parts of the design. These intentions or "rules" get transmitted clearly to the layout system via the database. The rules define the criteria for a circuit's logically-correct floorplan, critical nets, noise-free connections and more.

Now the layout designer can develop a layout that follows the design as originally conceived, not just as it was diagrammed. For example, Rules Driven Design allows automatic placement to convert logical groupings to a physical floorplan quickly, while pairing important functions close together. Automatic routing can then prioritize and implement critical connections.

Rules Driven Design makes it easier to meet schedules. There's synergism between new engineering technologies and design rules. And design reviews are minimized. It all adds up to better designs at lower cost by doing them right the first time. That translates to success in any language.

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## WHEN EVERY MINUTE COUNTS, RELY ON THE TIME-SAVING DEVELOPMENT TOOLS OF VLSI TECHNOLOGY, INC.

IF YOU'RE DESIGNING AN ASIC CHIP, you're probably under pressure to deliver as quickly as possible so that your company can beat its competition to the market. And that's only half the challenge. The other half is to make sure that this important new chip will work the first time it's fabricated. Oh, and by the way, your company would appreciate it if you could keep the budget down on this project. Does this scenario sound familiar?

It does to us. We're VLSI Technology, and we've helped hundreds of ASIC customers who have exactly the time, quality and cost concerns that you have. Our ASIC philosophy is very simple – Software, Service, and Silicon. We supply advanced software tools that save you time, expert consulting services to help assure the success of your design in its target system, and high-quality fabrication facilities that deliver working silicon the first time.

### ***Start Fast with Powerful ASIC Design Tools***

To design your ASIC chip, you need software that's easy to learn and use, yet flexible to meet your design needs. VLSI Technology, an early leader in IC design software, has developed a very powerful set of IC design software tools that comes in six different configurations so you can get exactly those tools you need to implement your design quickly. We call these six configurations the Express ASIC design systems. These systems range from the Entry Express™ system that supplies quick, easy-to-use schematic capture capabilities to the powerful Design Express™ system that supplies all the tools and libraries to design complex ASIC chips. The Express systems offer a design environment streamlined to minimize your design time while providing first time silicon success.

VLSI's compiler technology is responsible for the unique capabilities that

significantly speed your design process in the larger Express systems. Our Datapath Compiler and State Machine Compiler are good examples of the VLSI philosophy at work. Not only do these expert compilers automate a large portion of the design process, but they do it in a way that's compatible with your thought process. For example, when you think about designing a datapath, you think of it as a schematic: the Datapath Compiler uses schematics as input. When you think about designing state control logic, it's easy to think of it in terms of equations: our State Machine Compiler uses state equations as input. The result is time saved by eliminating the gate-level design for the datapath and state control logic, plus additional time saved through the tools' ease of use.

### ***The Only Compilers for Cell-Based Designs – AND Gate Arrays***

Our Datapath and State Machine Compilers are also the most flexible game in town. They are the only compilers that will give you two different types of output: a netlist for gate arrays and standard cells, or optimized layout for cell-based designs. And they will do it in either 1.5-micron or 2-micron technology. They save you time getting to market with the short fabrication time of gate arrays. When you're in full production and want to lower costs or increase your system's integration, you can switch to a cell-based design without redesigning your logic or re-entering your schematics.

### ***"Expert" Compilers Optimize Your Design***

We call our Datapath and State Machine Compilers "expert" tools because they are intelligent enough to add extra value to the compilation process. Both compilers execute optimization procedures to provide you with the densest possible

artwork within your parameters. For instance, the Datapath Compiler will automatically optimize the artwork to accommodate any bussing or wiring architecture. The State Machine Compiler uses three different optimization algorithms to minimize the gate logic and the resultant artwork area of this logic. These optimization features are available regardless of the implementation technology you choose.

### ***Cell-Based Compilers for Optimized Designs***

VLSI also has an outstanding family of cell-based compilers including ROM, RAM, PLA and multiplier. These are specifically designed to take advantage of the features of our 1.5-micron fabrication technology to optimally utilize the silicon area in a chip design. And VLSI's new Chip Compiler can quickly combine various cell-based elements into an optimally designed chip – work that used to take a month or two now only takes a couple of days.

### ***Speed of Design Plus Success in Fabrication***

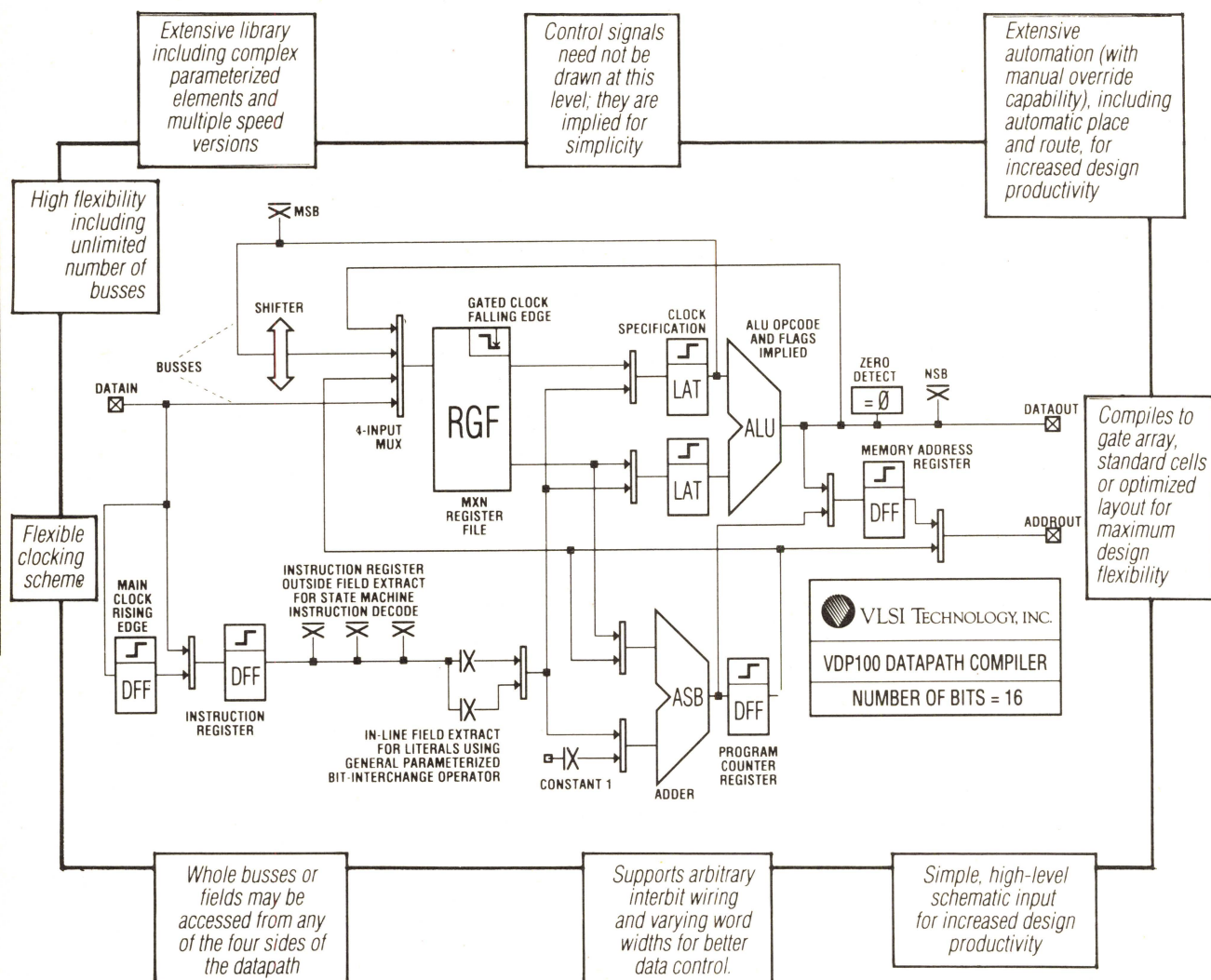
One of the greatest advantages in using VLSI's tools and systems is that we never forget your ultimate goal is a successfully fabricated IC. We engineer success into each step of the process. For example, our expert compilers automatically add structures into the compiled silicon that improve fab yields and device performance. The result is not only a chip that works the first time, but one that is less expensive to produce.

Perhaps the best way to understand the strength and speed of VLSI design tools is to see how an actual design was done, and how our compiler technology can save you weeks of design time. So turn the page and let us show you how we perform in the real world.





## DESIGN A RISC PROCESSOR IN TWO DAYS WITH EXPERT COMPILERS



WITH VLSI'S POWERFUL COMPILERS WE were able to implement a 16-bit reduced instruction set computer (RISC) in only two days. The entire specification contained about 7500 gates of logic and was implemented with one datapath, three state machines and one overall schematic that connected these pieces together.

The 16-bit RISC CPU has 22 instructions including arithmetic and logical operations, literals, conditional jumps, subroutine calls and a wait for coprocessor. As it executes an instruction, it fetches the next instruction and computes the address of the following instruction.

The datapath contains two ALUs –

one for emulation and one for address calculation a shifter and several registers. We entered the schematics for these ALUs using the Datapath Compiler, and it determined the optimal physical block placement. Since the Datapath Compiler can build a chip with any number of busses, we had a lot of flexibility available for our design's architecture.

The control logic naturally fell into three pieces that were implemented using the State Machine Compiler. The first two were very simple: the equations for the register decoding and condition selection only took a few lines. The third, the instruction emulator, was more com-

plicated. We defined multiple-bit busses in the State Machine Compiler for the control signals to the datapath elements and for the extracted fields from the instruction register. Then, we wrote our instruction definitions in terms of the names of the microinstruction registers and ALU operations. At one point, when we changed the number of registers, all we had to do was change the size of the register field and recompile the instruction emulator state machine. We never had to manipulate the actual bits in the control words. The State Machine Compiler translated our equations into logic, optimizing it at the same time.





Simulate directly from this description, without creating final netlist, with special built-in debug features

Three types of optimization are performed

Flexible input/output options

Busses and symbolic constants can be defined for more efficient coding

Automatic or manual state assignment

Allows comparison and assignment of busses

Default values can be specified

User-specifiable performance requirements

Used for combinatorial logic, not just state machines

"Don't cares" are supported, resulting in further optimization

Compiles to gate array, standard cells or PLA for design flexibility

Simple, high-level language description increases design productivity

DESIGN AUTOMATION

VLSI Technology

```
sm idec;          # state machine for RISC instruction sequencing and decode

# define bus types & symbolic values for instruction decode & control signals
define riscOP      jump='d0 call='d1 load='d2 store='d3 loadr='d4 storer='d5
                  move='d6 add='d7 sub='d8 and='d9 or='d10 xor='d11

define dpalu       alu_add='b00000 alu_sub='b01000 alu_xor='b00100

# declare inputs and outputs - some are control signals from/to datapath
latched inputs    op[3:0] op2[3:0] cwait cc shiftmsb_bit[15];
load .35 outputs  memWr=0; # memory write enable
RS=1 outputs      signextend
                  wenable=1; # right shift msb input
                  alu:dpalu   # register file write enable
                  selrgf:dpmux4=mux0 # alu op (a bus of type dpalu)
                  # register file input mux select

# specify desired performance
clock cp[10];          # 10 MHz
maxdelay 10 cp -> memWr memRd memPC wenable; # 10 ns critical paths

reset r -> FETCH;      # specify reset signal and state

let rgf_wl[0] = (r0[3:0]='d1 & !reg0) & wenable;

state FETCH -> EXECUTE seladda=muxnone wenable=0;
                  # i.e. go to EXECUTE state and set these signals

state EXECUTE = 001
  op=add -> alu=alu_add load_cc, # set these signals
  op=sub -> alu=alu_sub load_cc,
  op=addLit -> alu=alu_add selalub=mux1,
  op=xor -> alu=alu_xor load_cc signextend=?,
  op=op1 & op2=shl -> selrgf=mux1 shift=shiftup,

end
```

One of the biggest advantages to VLSI's Datapath and State Machine Compilers is the flexibility of implementation. From exactly the same specifications, we were able to generate an optimized layout as well as a netlist for gate arrays and standard cells. We compared our options by building gate array, standard cell and optimized layout versions. With the gate array and standard cell versions, the physical artwork was automatically placed and routed.

To generate the optimized layout version, we utilized VLSI's Chip Compiler. After specifying the general block floorplan of the chip, the program allowed us

to "pour" the standard cell logic into the free spaces between megacells or compiled blocks. Although our logic design was organized into three logic netlists that were generated by the State Machine Compiler, these netlists could be routed into any number of standard cell regions automatically. This allowed us the freedom of optimizing the chip's floorplan independently from the constraints of our logic design's organization.

In addition to routing the standard cells, the Chip Compiler also connected the power, ground and all the routes to the optimized layout of the datapath. By automatically compacting the routing

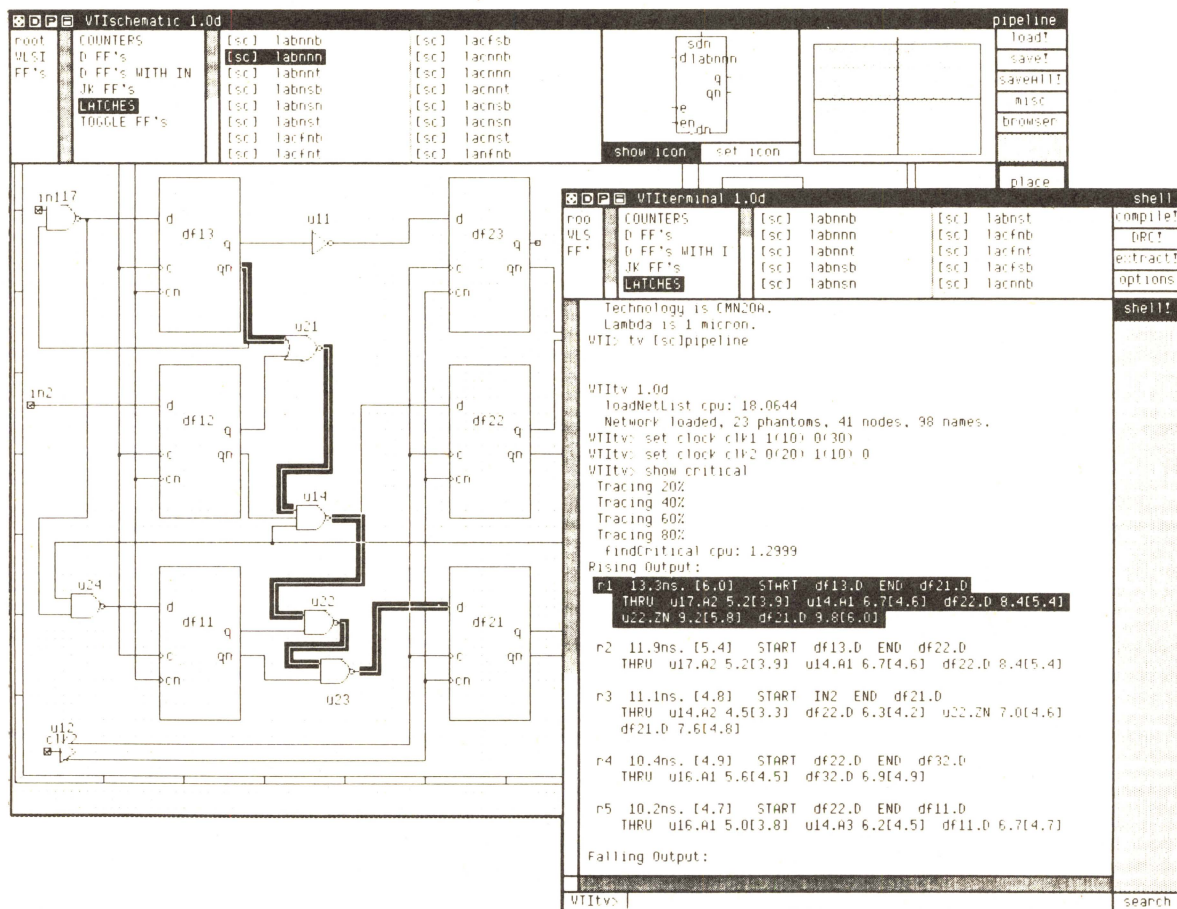
areas, the Chip Compiler also cut the chip's size by about 10%. The Chip Compiler then built a pad ring from our schematic's specifications, and we were finished - all in less than a day.

How did the sizes of these implementations compare? The gate array version fit on an 8000-gate base, which is 280 mils on each side. The standard cell version was 214 by 244 mils. And the optimized version was 169 by 178 mils. The ratio of the areas was roughly 3:2:1.



# TIMING VERIFIER

- ◆ Identification of any specified number of critical timing paths in the circuit so that a designer can concentrate on those paths during simulation.
- ◆ Analysis of either an entire chip for global system checks, or specific paths which are defined by the user for more specific analysis.
- ◆ Estimation of a circuit's maximum frequency of operation, to assure that the finished ASIC chip will perform to design specifications.
- ◆ Identification of any clock skew problems that might be prevalent in a design before they cause logic problems during simulation.
- ◆ Checks for setup and hold time violations in the circuit to verify that the input to a storage element does not change before the specified setup or hold time for that element.



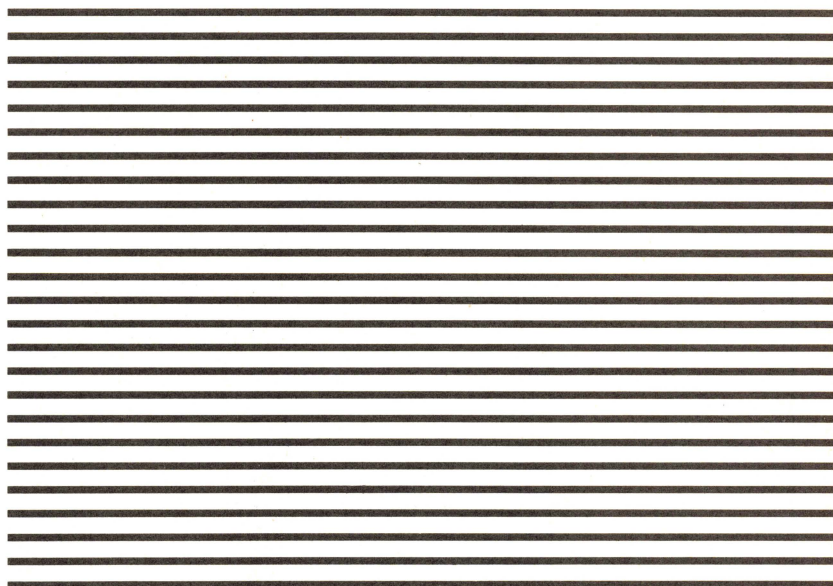


## TIMING VERIFIER

The scope of highly integrated systems and logic designs has increased dramatically over the past few years. The complexity of these designs makes it impractical to use simulation to discover critical timing nets through these circuits. VLSI's timing verifier offers a quick means of filtering through a complex circuit to identify any critical timing paths which limit the performance of the design.

The timing verifier performs a static timing analysis of a circuit. No input vectors are needed and no assertions need be provided for analysis. All system clocks are defined as program input prior to analysis. The program then provides an analysis of synchronous systems that are composed of alternating levels of storage elements and combinational logic.

After functional logic simulation has verified a design, the timing verifier assists in identifying the potential timing problems in the design's circuitry. These nodes and paths can then be examined more closely during timing simulation for their effects on the circuit's performance.



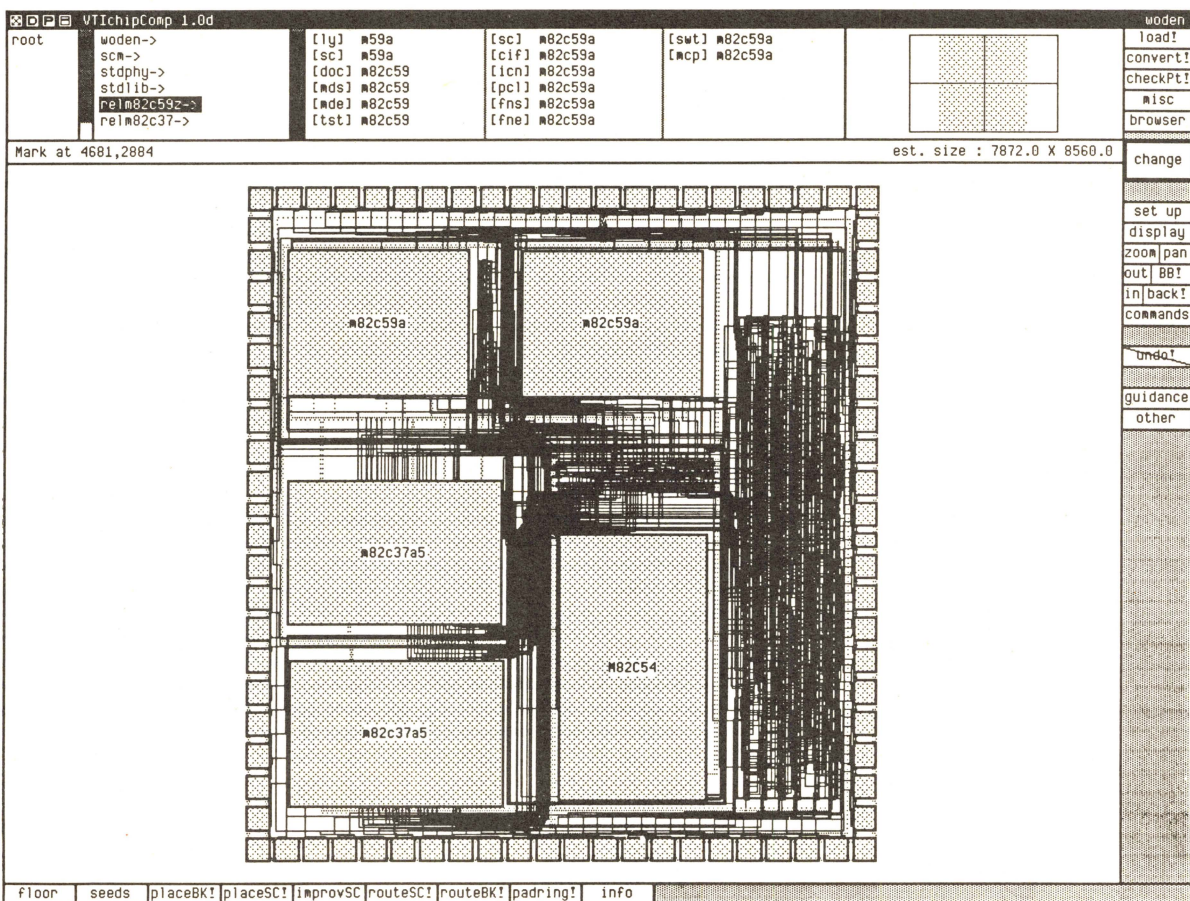
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# CHIP COMPILER

- ◆ Seed placement and net weights can be specified for the standard cell regions to optimize critical routes and to minimize timing problems within the design.
- ◆ Optimized sub-netlists are created automatically to assign standard cells to defined regions within the physical design. This frees the designer from having to optimize these regions within the logic design of the chip.
- ◆ Routing channel density between arbitrary blocks can be displayed prior to routing to help evaluate the efficiency of the design's floorplan.
- ◆ The system automatically identifies free channels for the second routing layer of metal within the standard cells, and routes over the top of the cells to minimize the routing area of the chip.
- ◆ The chip compiler's router eliminates any unnecessary via's in the interconnections in order to improve the timing characteristics and the process yields of the chip.
- ◆ Power busses are sized automatically during routing to optimize them, based on the operating frequency and power consumption of the design.
- ◆ Interconnection wiring capacitance can be extracted from the chip's routing to improve the accuracy of post-route simulation and verification.





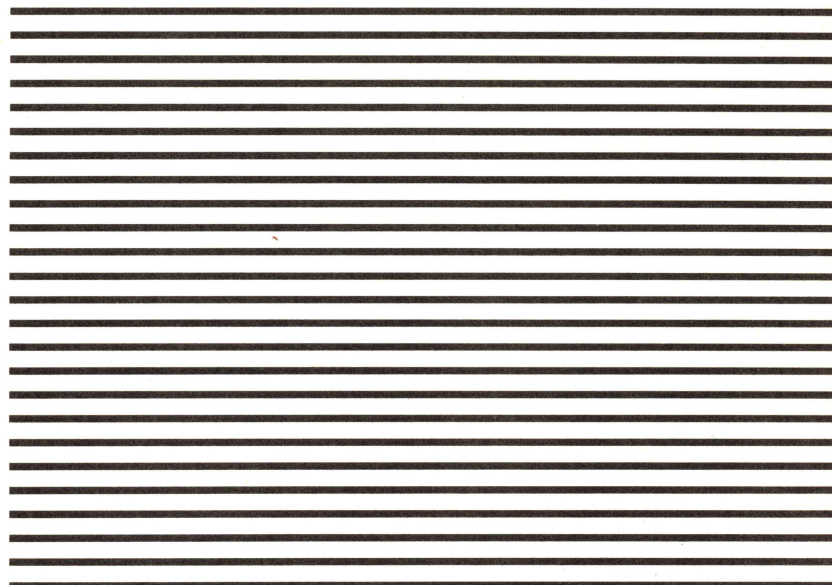
## CHIP COMPILER

The VLSI chip compiler is an integrated arbitrary block and standard cell placement and routing system. It provides a highly automated methodology for chip assembly. The system offers designers the capability to place arbitrary blocks interactively, and to define regions between those blocks for standard cells within their designs. Analysis tools are provided to evaluate the efficiency of the chip's floorplan on the basis of interconnect routing density. The chip compiler automatically sizes the defined standard cell regions to properly accommodate all the standard cells and their interconnections as they are listed in the design. After automatic placement of the standard cells, these regions and the interconnections between them are routed using a compaction algorithm to minimize the area of the chip.

Routing guidance for interconnection paths, and wire widths can be specified with rough diagrams within the floorplan. The chip compiler follows this guidance to help optimize the floorplan, and minimize the routing area for critical routes such as power or highly propagated signals.

If a pad ring is specified in the design's schematic, the chip compiler assembles it around the chip automatically. The system evaluates the area of the design, and selects the proper pad type based on the pitch for a core limited or pad limited design. Static latch up problems for CMOS designs are alleviated with the use of a guard ring within the pad ring's design.

By using the chip compiler for chip assembly, the ASIC designer has more freedom to optimize the layout and floorplan of his chip. The standard cell regions can be defined and optimized at chip assembly independently from the way they are listed in the schematic for the design. The program automatically optimizes the placement of the standard cells within these regions to minimize standard cell and macro block interconnect.



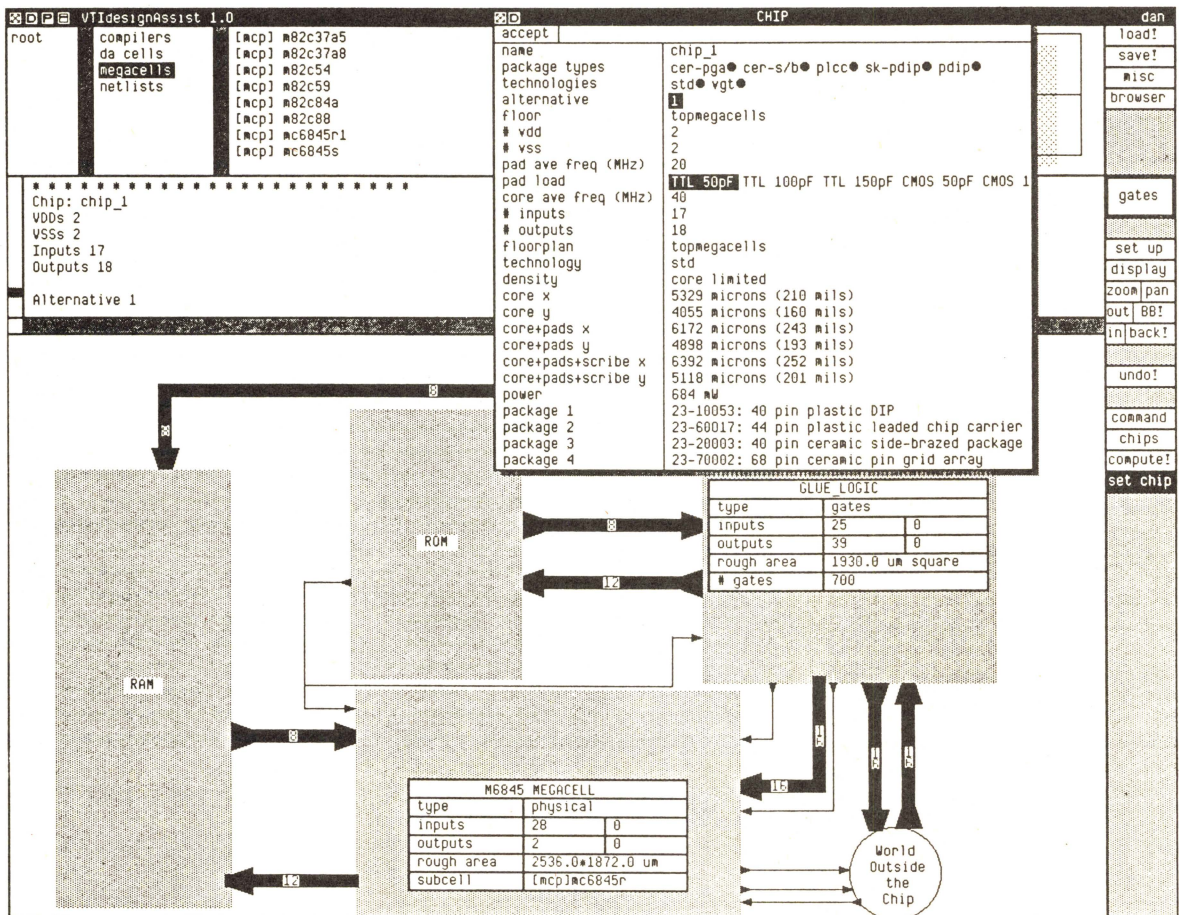
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# DESIGN ASSISTANT

allows the customer to partition his system into components on the basis of packaging, and technology to help minimize system costs.

- Designs can be entered as generalized block diagrams. This enables the customer to analyze design alternatives without having to execute a detailed schematic or physical design.
- Block diagrams are entered in graphical form with data flow indicated with arrows. This facilitates system conception, and helps document the various design alternatives.
- Data for system blocks can be entered as gate count, a list of TTL parts, a captured netlist, or physical artwork. Accuracy of the design estimates improves with the accuracy of the design details.
- The system evaluates partitioning alternatives based on: chip size, chip power, routing area, packaging alternatives, and relative costs. It illustrates the most effective ways to complete the design of the system's parts.
- The Design Assistant generates icons for the schematic editor from functional block descriptions. This facilitates a project's flow from design partitioning to logic design.
- Engineers can add their own estimation rules to the system to tailor the tool to their own needs or other available technologies.

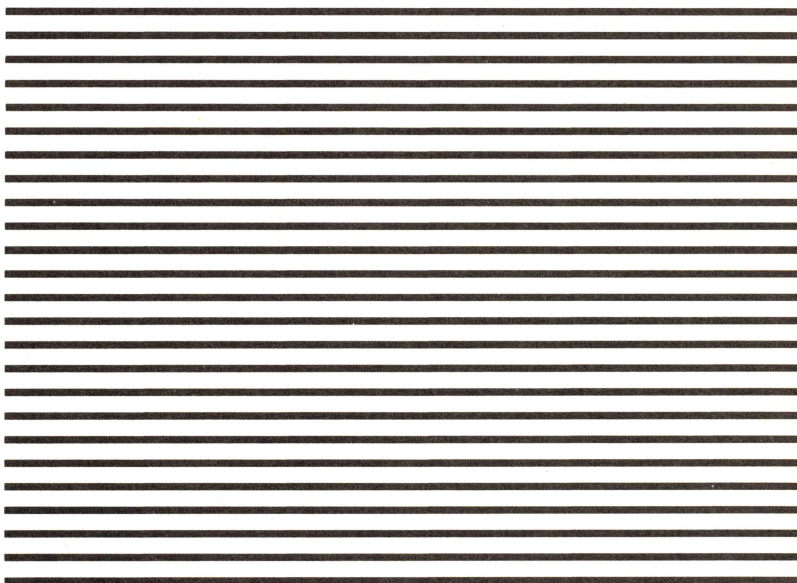




## DESIGN ASSISTANT

**I**n the past few years, the complexity of integrated circuits, has grown beyond the abilities of the average engineer to make effective decisions on the complex design alternatives that are available on the market. VLSI Technology is the first company to provide a Design Assistant program for the system engineer to evaluate these design alternatives based on a simple system partitioning methodology. The system evaluates the different implementation technologies such as: Gate Array, Standard Cell, Full Custom, and Silicon Compilation to identify the most efficient and effective method in which to implement a chip. Feasibility studies for different chip designs can be implemented at whatever level of design detail is available. Through the use of artificial intelligence algorithms, the system provides a list of design alternatives rationalized by power, size, cost, and packaging requirements. The Design Assistant helps the systems engineer decide which system blocks belong in ASICs, and which should be purchased as standard products for PC boards. By eliminating the guesswork out of ASIC design, VLSI Technology can provide its customers with the most cost effective solutions for the development of their systems.

**Availability.** The Design Assistant will be released on the VAX, MicroVAX, Apollo, Elxsi, Ridge, HP9000 Series 320, Sun and Alliant computers. The product will be available in VLSI Technology's design centers in January, 1987. The product will be available as an integrated part of the ASIC design system in Q2, 1987.



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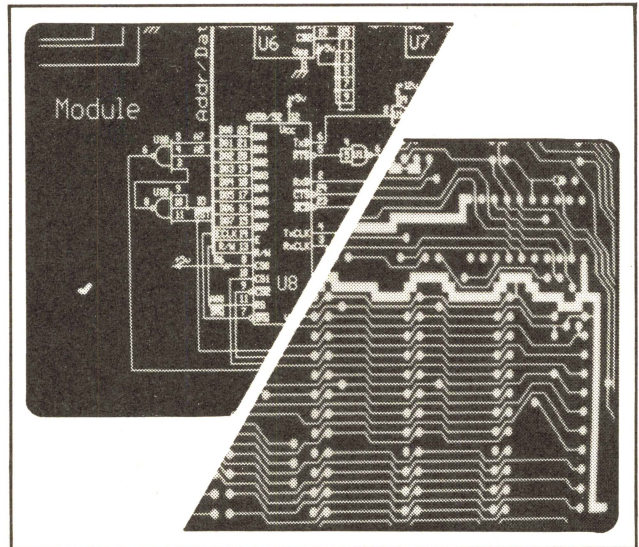
# Start the job right with HiWIRE<sup>®</sup>, schematic-capture software. Finish the job right with smARTWORK<sup>®</sup>, printed-circuit-board design software.

**HiWIRE:** HiWIRE provides a better alternative to the traditional pencil-and-paper approach of drawing electronic schematics. With HiWIRE and your IBM PC, you can create and revise precise schematics quickly and simply.

Use symbols from HiWIRE's extensive library, modify them, or create your own quickly and painlessly. When you need hard-copy output, print your schematics quickly on a dot-matrix printer, or plot superior-quality output on a pen plotter.

**smARTWORK:** Use smARTWORK and your IBM PC to create and revise printed-circuit artwork in a fraction of the time that conventional methods require. In a couple of hours, you can create single- or double-sided boards of any complexity and up to 10-by-16 inches.

And once you've created a schematic, you can automatically route it from the HiWIRE netlist. smARTWORK also lets you interactively route your board and verify it with a schematic-to-layout cross-checking program.



Use your IBM PC to create schematics with HiWIRE (left) and PCB layouts with smARTWORK (right).

## System Requirements

- IBM PC, PC XT, or PC AT with 512K RAM, 2 disk drives\* and DOS 2.0 or later
  - IBM Color/Graphics Adapter or EGA with RGB color monitor or IBM Enhanced Color Display
  - Microsoft Mouse (optional for smARTWORK)
  - IBM Graphics Printer or Epson FX/MX/RX-series dot-matrix printer, and/or:
  - Houston Instrument or Hewlett-Packard pen plotter
- \*HiWIRE requires a parallel printer port.

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of ICs

Designing

Prototyping

Purchasing  
of  
Parts

Production  
of the  
Product

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The best time for an engineer to pick the integrated circuits that will go into his next design is at an early stage in the design process when the engineer's plans are still flexible enough to take full advantage of the features selected.

There is a point in the early phases of every design when engineers focus on selecting integrated circuits. They examine specifications, weigh relative strengths and weaknesses of various devices, and choose the field of candidates. This critical time in the design cycle when designers want to be sure the right devices are in serious contention for their applications.

This is when the engineer reaches into his technical reference library. Of the material on his shelves, **IC MASTER** is the only reference source that has been especially prepared for this moment.

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**SEE PAGE 4701 FOR  
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Microprocessors

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# **INTRODUCTION TO MICROPROCESSOR DEVELOPMENT SYSTEMS**

This section describes the tools used in developing software programs for microprocessors. Microprocessors supported range from 2-bit slice families and 4-bit processors to 32-bit machines. Development systems described in the Master Selection Guide range from simple, single-user text-editing stations to multi-user computers dedicated to software development. Also included are In-Circuit Emulators, a device which emulates functions and timing as if it were in a target system. Manufacturers are sequenced alphabetically, and each system is described by a listing of performance parameters.

## MPU DEVELOPMENT SYSTEMS

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
1802, 1805, 1806, 6301R, 6301X, 6303R, 6303X, 6303Y, 6305U0, 6305V0, 6309, 6309E, 63701Y, 64180R0, 6502, 65C02, 6503, 6504, 6505, 6506, 6507, 6512, 6513, 6514, 6515, 6800, 68000, 68008, 6801, 68010, 6802, 6803, 6805C4, 6805C8, 6805D2, 6805E2, 6805E3, 6808, 6809, 6809E, 68HC11A2, 68HV11A8, 80186, 80188, 80286, 8031, 8032, 8035, 8039, 8040, 8049, 8050, 8051, 8085, 8086, 8088, 8096, 8097, 80C31, 80C32, 80C39, 80C49, 80C51, 80C86, 80C88, 8344, 8396, 8397, 83C44, 8748, 8749, 8796, 8797, 8X300, 8X305	1	1	N/A	16 or 64	192		as per host	as per host	as per host	x	x	x
Z80, Z80B, 8080, 8085, 6800, 6802, 6808, 6809, 6809E, 8035, 8039, 8040, 8048, 8059, 8050, 8748, 8749	1	1		64								
8035, 8039, 8040, 8048, 8050, 8748, 8749, 8080, 8085, Z80, MK3880/4, NSC-800	1	1		64	64							
Z8001, Z8002, Z8003, 68000, 68010, 68020, 8086, 80186, 80286	1	2		64	2 MB					Opt.		
68000, 68008, 68010, 68020, Z8001, Z8002, 8086, 8088, 80186, 80188, 80286	1	2		128	2 MB					opt.		
WE32100	1	2		56						Opt.	Opt.	Opt.
8031, 8032, 8051, 8052	1	1	5	16	40						x	
8085	1	1	4	64		2	8	2M				
8086	1	1	3	128	16Mb	2	8	2M				
8085	1	1	4	64		1	8	1M	26M			
8086	1	1	3	128	16Mb	1	8	1M	26M			
8086	16	5	3	1Mb	16Mb	1	8	1M	52M			
Z-80	1	2	0	64	64	2	3.5	790 K	Opt.		Opt.	Opt.
Z-80	1	2	1	64	64	2	3.5	790 K	Opt.		Opt.	Opt.
Z80	1	2		64	64	2	8	560	Opt.		Opt.	Opt.
Z-80	1	2	0	64	64	1	8	560 K	5 MB		Opt.	Opt.
Z80	1	2	1		64						Opt.	x
8085	1	2	1		64						Opt.	x
8086, 8088	1	2	1		1MB						Opt.	x
80186, 80188	1	2	1		1MB						Opt.	x



Software Support		Comments	Model	Source	Line
Standard	Optional				
Macro Cross-Assembler, Relocating Linker, Symbolic Debugger	C Cross-Compilers w/Source-Level Debugging	Over 75 microprocessors supported on the IBM PC; many are also supported on the Sun Workstation and Macintosh II. C Source Debugging available now; Performance Analysis System	<b>EZ-PRO</b>	<b>AMA</b>	<b>(4751)</b>
	Remote control and symbolic debug package for DOS operating systems.	Stand-alone in-circuit emulator. Real time trace: 32 bits wide, 256 traces deep with disassembly. Diagnostic functions: standard and user-defined for debugging hardware in design, test and service.	EM-SERIES	AppMicroSys	
Stand-alone or hosted in-circuit emulator, real-time and transparent operation, diagnostic functions, in-line assembler, memory and trace disassembler, real-time trace 256x32 bits.	Remote control and symbolic debug package for MS/DOS operating systems.		EM Series	AppMicroSys	
	High level debuggers, host emulation control software, cross compilers	Stand-alone in-circuit emulator. Real time trace: 72 bits wide by 2048 deep.	ES-SERIES	AppMicroSys	
Stand-alone or hosted in-circuit emulator, real-time and transparent operation, diagnostic functions, in-line assembler, memory and trace disassembler, real-time trace 2048x72 bits.	Full high-level and symbolic debug packages available for various hosts (SUN, APOLLO, VAX (Unix), PC and MicroVAX.	Mainframe convertible to different microprocessor families by changing only board and pod.	ES Series	AppMicroSys	5
WE32150 development software program. I/O library and assembly-level debugger for host side support	Ferret high level language debugger, software support for logic analyzer 64000. Bus state analysis option, symbolic hardware debugging, disassembly of hardware bus traces.	Zero wait state emulation of CPU and MMU, display of CPU and MMU Registered. Disassembly of instructions stored in memory.	<b>WE321DS</b>	<b>AT&amp;T</b>	<b>(2525)</b>
Cross Assembler, Communications		Works in conjunction with IBM PC or compatibles.	PDK51	BinaryTech	
CP/M operating system	High-level languages	Programmable serial port, floating-point processor	Diskstor M-1	Comark	
MS-DOS, CP/M86 operating system	High-level languages	Programmable serial port, floating-point processor	Diskstor M-2	Comark	
CP/M operating system	High-level languages	Programmable serial port, floating-point processor	Diskstor M-3	Comark	10
MS-DOS, CP/M86 operating system	High-level languages	Programmable serial port, floating-point processor	Diskstor M-4	Comark	
MP/M86 operating system	High-level languages	Programmable serial port, floating-point processor	Diskstor M-6	Comark	
CDI-CP/M	Basic, C Assemblers, Pascal	Uses CPU-2, the optional 3.5 inch hard disk drive can be mounted on the Winchester controller board.	CDI300	CompDyn	
CDI-CP/M	Basic, C Assemblers, Pascal	Uses CPU-2, the optional 3.5 inch hard disk drive can be mounted on the Winchester controller board.	CDI400	CompDyn	
CDI-CP/M	Basic C Assemblers, Pascal	16-Slot Card Cage	CDI5000	CompDyn	15
CDI-CP/M	Basic, C Assemblers, Pascal	9 slot card cage, optional power supply	CDI5050	CompDyn	
Downloads code from PC to STD, debugger.		Target STD system acts as emulator.	DSZ80	Devtek	
Download code from PC to STD, debugger.		Target STD system acts as emulator	DS8085	Devtek	
Downloads code from PC to STD, Debugger.		Target STD system acts as emulator.	DS8088	Devtek	
Downloads code from PC to STD, debugger.		Target STD system acts as emulator.	80188	Devtek	20

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
8080	1	2		256		1		2M			x	x
8080	1	3		1Mb		1		2M			x	x
1802		2		16		2					Opt.	Opt.
68000, 68010, 68020, 8086, 8088, 80186, 80286	60	1	1	32	1 MB					x		
68000, 68010, 8086, 8088, 8085, Z80A, Z80B, NSC800, 6809, 6502, 8048 family	1	2		128		2	8		40M	x	x	
68000, 68010, 8086, 8088, 8085, Z80A, Z80B, NSC800, 6809, 6502, 8048 family	15	1		128						x	x	
68000, 68010, 8086, 8088, 8085, Z80A, Z80B, NSC800, 6809, 6502, 8048 family	60	4								x	x	
F3, F3870 family	1			16		2					Opt.	Opt.
F8, F3870, F6800, F9445, F16,000	1	2		128		2		1M			Opt.	Opt.
9440, 9445	1	1		64		2	5 1/4					150
6802, 6808 or 6809	1	2	1	8								
68000, 68010, 68020	16	8	1	1MB		1	5 1/4	1MB	170MB			
68000, 68010, 68020	16	8	1	5MB		1	5 1/4	1MB	170MB			
6800, 6801, 6802, 6803, 6805, 6805P, 6805R, 6805U, 146805E2, 146805G2, 6808, 6809, 6809E, 68000, 68008, 68010, 68020; 8031, 8035, 8039, 8048, 8049, 8051, 8080, 8085, 8086/8087, 80C86/8087, 8088/8087, 80C88/8087, 8096, 80186, 80188, 80286; Z8 (assembler only), Z80, Z80A, Z80B, Z80H, Z80L, Z8001, Z8002; TMS9900, TMS32010; TMS7000, SBP9900 and SBP9989 with user-definable emulation; NSC800; 1802 and 6502 with user-definable emulation; F9450; 6301V/X/Y, 63P01M, 6303R/X/Y, 63701X/Y; 70108, 70116, HD64	6/cluster 16/Host computer	2 (4 Prog.)	1	System Memory 96Kbyte	876Kbyte	2	5.25	240Kbyte	132M	See comments	opt.	opt.



Software Support		Comments	Model	Source	Line
Standard	Optional				
CPM/80, complete disk operating system with editor, assembler, debugger and utilities.	Fortran, Pascal, Basic, PL/I, "C", Cobol, PLMX; Cross-assemblers for all 8-bit microprocessors; multi-tasking operating system.	Hardware options include 1/2-inch magnetic tape, Winchester drive, in-circuit emulation, cassette tape, modem.	DCS/80	DistComp	5
Complete disk operating system with editor, assembler, debugger and utilities.	High-level language, Fortran, Cobol, Pascal, Basic, PL/I Cross-assemblers for all 8-bit microprocessors; multi-user, multi-tasking operating system.	Hardware options include 1/2-inch magnetic tape, Winchester drive, in-circuit emulation, cassette tape, modem.	DCS/86	DistComp	
MicroForth compiler, disk operating system, macroassembler, interactive debug, emulation string and line editor.		Self diagnostics, in-circuit emulator.	EiCOMPuMOS	DiversTech	
Slice-Source language, in-circuit emulation, High level symbolic debugging, Hunter and Ready VRTX Real-Time Executive.	C Compilers and Cross Compilers, Assemblers.	New generation of high-power, low-cost microprocessor development systems and in circuit emulators which runs under users Host computer: MS-DOS, PC-DOS, VMS, Micro VMS, UNIX, XENIX, etc.	DE1000	Emulogic	
RT-11 operating system, macro-relocatable cross-assemblers, linker, symbolic debugger, screen-oriented editor, HELP files.	PASCAL and "C" cross-compilers for most processors. All standard DEC software options.	In-circuit emulation of all chips supported. Real-time trace captures all bus activity.	ECL3211	Emulogic	
RT-11 Operating system, macro-relocatable cross-assemblers, linker, symbolic debugger, screen-oriented editor, HELP files.	PASCAL and "C" cross-compilers for most processors. All standard DEC software options.	Multi-user system based on DEC PDP-11 family of host processors. Supports multiple ECL-3211 satellite software/hardware stations as well as standard VT100 software-only stations on host.	EMUNET-1	Emulogic	10
RT-11 Operating system, macro-relocatable cross-assemblers, linker, symbolic debugger, screen-oriented editor, HELP files.	PASCAL and "C" cross-compilers for most processors.	Multi-user system based on DEC VAX-11/730, 11/750, and 11/780 host processors. Supports multiple ECL-3211 satellite software/hardware stations as well as standard VT100 software-only stations on host.	EMUNET-2	Emulogic	
Assembler, editor, debug package.		Options: In-circuit emulator, PROM boards, communications boards, floppy disc interface.	Formulator Mark III	Fairchild	
IMDOS multi-user disk operating system and Basic language packages.	Fortran, Pascal, Crossassemblers, PEPLINK, loaders, debugger, and EMUTRAC, control software for F8, F3870, F6800 and F16000 families.	Optional Real-Time Executive Operating System for multitasking in F9445-based systems. Optional video terminal, peripheral controller boards and I/O boards.	FS1	Fairchild	
Multitasking time-share oriented disc operating system; macroassembler, test editor, utilities, debuggers; real-time executive.		Peripherals purchased from independent vendors.	Microflame 1	Fairchild	
ROM-based debugging monitor with utility routines and friendly prompts.		Six 8-bit parallel I/O ports with control signals. 50 thru 19.2K bps, independently selectable, serial ports. 16 memory map configurations, switch selectable. Six sockets for ROM/PROM 2K, 4K or 8K types. Requires serial display terminal and 5V power. Asynchronous multibus compatible.	PEP68	Fairchild	
PDOS, Assembler C.	Pascal, Fortran 77, Basic.	High-performance target development, to 25 MHz CPU.	FOCUS32	Force	
UNIX, Assembler, C Debug.	Fortran 77, Pascal, Basic.	High-performance Unix box to 20 MHz CPU includes 125 MB Streamer tape.	FOCUS32/25U	Force	
Operating software supplied with each subsystem.	C Pascal, Assemblers, Linkers,	Logic Development System: 200/400MHZ Timing/125 MHz state 8 to 32 channels. 20 to 120 channels of state analysis. Real-time high-level analysis. Software performance analysis. Structured Analysis/Design.	HP64000	HP	

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
6801, 6803, 6805, 6805P, 6805R, 6805U, 146805E2, 146805G2, 6809, 6809E, 68008, 68010, 68020, 8031, 8035, 8039, 8048, 8049, 8051, 8080, 8085, 8086/8087, 80C86/87, 8087, 80C88, 80C87, 8096, 80186, 80188, Z8 (assembler only), Z8001, Z8002; TMS9900, TMS32010, TMS7000, SBP9900 and SBP9989 with user-definable emulation; NSC800; 1802 and 6502 with user-definable emulation; F9450; 6301V/X/Y, 6303R/X/Y, 63P01M, 63701X/Y, 70108, 70208, 70116, 70216, HD64180R/Z, 80386.	6/cluster 16/Host computer	4	2	4MB	6MB			Opt.	55M	See comments	Opt.	Opt.
All microcoded and bit-slice devices	6/cluster	2 (4 Prog.)	1	32/64	34/64	2	5 1/4	240	132M	See comments	Opt.	Opt.
Z80, Z80A, Z80B, Z80H, 68000, 68010, 80186, 80188, 8086, 8088, TMS32020, TMS320C25	16	2								x		
All bit slices, 2901, 2903, 29203, 29501, 29116, 8X300, 8X305, 74S481, 3000, and macrologic. Also ECL10800, 10220. 1 to 4 WCS arrays.	4	3	1	512	160	2	5 1/4	2M		x	x	x
All Microcode devices (e.g., 29116, 2901, 29300, 29500, AS888, 2910, AS890, 29PC141, Weitek 1064)	1	3	2	640	640	1	5-1/4	1.4 M	20 M	x	Opt.	Opt.
All Microcoded Devices (e.g., 29116, 2901, 29300, 29500, AS888, 2910, AS890, 29PC141, Weitek 1064), All Bit-Slice Devices	1	3	2	640	640	2	5-1/4	740 K		x	Opt.	Opt.
All Microcoded Devices (e.g., 29116, 2910, 29300, 29500, AS888, 2910, AS890, 29PC141, Weitek 1064), All Bit-Slice Devices	1	3	2	640	640	1	5-1/4	370 K	10 MB	x	Opt.	Opt.
All Microcoded Devices (e.g., 29116, 2901, 29300, 29500, AS888, 2910, AS890, 29PC141, Weitek 1064)	1	3	2	640	640	2	5-1/4	740 K		x	Opt.	Opt.
Any	1	3	1			2	5-1/4	360	20 MB	x		
EC-1000	1	1								x		opt.
EM29PL141	1	3	2	640	640	1	5-1/4	1.4M	20M	x	opt.	opt.
HY65C02, HY65C816, HY65C00/1, HY6500/11	1	1		16						x		
IMST414												
IMST414												
MCS-86, MCS-85, MCS-80 and MCS-48 families	1				64			250			Opt.	Opt.



Software Support		Comments	Model	Source	Line
Standard	Optional				
Operating software supplied with each subsystem.	C, Pascal, Assemblers, Linkers,	Logic Development System: 200/400 MHz Timing/125 MHz state 8 to 32 channels. 20 to 120 channels of state analysis. Real-time high-level analysis. Software performance analysis. Structured Analysis/Design	HP64000-UX	HP	5
Operating software supplied. Includes soft key driver interface.	User-definable microassembler/linker, with error checking, macros, nested macros, and link to analysis environment.	25 MHz state analysis.	HP64276	HP	
Operating software supplied with each subsystem.	C, Assemblers, Linkers	Logic development system; 100/200 MHz; Timing/25 MHz state, 16 channels, coverage analysis.	HP64700	HP	
MENU Prompts: Editing, Target Control, Remote operation, display formatter, diagnostics, download models, TRACE dump, multiple arrays.	Universal meta-assembler up to 80 bits, MACRO's FORTRAN IV compatible or CP/M version.	Performance analysis measures target activity in 16 user categories. TRACE has 16-level Trigger logic.	DS370	HiLevel (4752)	
PC utilities, EPL programming language, patchwork-source code editor, META disassembler, PCTERM-VT00 terminal emulator	HALE-relocatable Linkable MACRO META assembler, EPL-VMS & EPL-UNIX programming language for VAX, DU-VMS, UNIX upload/download for Vax.	Also available are in-circuit emulators for 29116, 2910, AS888 and AS890.	DS3700/ CSIBM-AT	HiLevel (4752)	
PC Utilities, EPL-Programming Language, Patchwork-Source Code Editor, META Disassembler, PC TERM-V100 Terminal Emulator	HALE-Relocatable, Linkable, MACRO META Assembler, EPL-VMS & EPL-UNIX Programming Language for VAX, DU-VMS, UNIX Upload/Download for Vax.	Also available are in-circuit emulators for 29116, 2910, AS888, and AS890	DS3700/ CSIBM-PC	HiLevel (4752)	
PC Utilities, EPL-Programming Language, Patchwork-Source Code Editor, META Disassembler, PC TERM-V100 Terminal Emulator	HALE-Relocatable, Linkable, MACRO META Assembler, EPL-VMS & EPL-UNIX Programming Language for VAX, DU-VMS, UNIX Upload/Download for Vax.	Also available are in-circuit emulators for 29116, 2910, AS888, and AS890	DS3700/ CSIBM-XT	HiLevel (4752)	
PC Utilities, EPL-programming language, patchwork-source code editor, META disassembler, PC TERM-VT100 terminal emulator	HALE-Relocatable Linkable MACRO META Assembler, EPL-VMS & EPL-UNIX Programming Language for VAX, DU-VMS, UNIX-Upload/Download for VAX	Also Available are in-circuit emulators for 29116, 2910, AS888 and AS890.	DS3700/ CSTI-PC	HiLevel (4752)	
Menu-driven operating system		Logic State Analyzer, 256 Channels x 4K	DT3700	HiLevel (4752)	
Menu Prompts: Editing target control, remote operation, display formatter, diagnostics, download models, TRACE dump, multiple arrays	HALE-relocatable Linkable MACRO META assembler, EPL-VMS & EPL-UNIX programming language for VAX, DU-VMS, UNIX upload/download for VAX		EC1000	HiLevel (4752)	10
PC utilities, EPL programming language, patchwork-source code editor, META disassembler PCTERM-VT00 terminal emulator	HALE-relocatable Linkable MACRO META assembler, EPL-VMS & EPL-UNIX programming language for VAX, DU-VMS, UNIX upload/download for VAX		EM29PL141	HiLevel (4752)	
Host driver	Cross assembler	In-circuit emulator for Hyundai MPU and MCP	HMDS1	Hyundai	
Stride 440		Cross-Software Package	IMSD100	Inmos	15
VAX-VMS		Cross-Software Package	IMSD600	Inmos	
ISIS-11 disk operating system with relocating macroassembler, linker, locator, and CRT-based CREDIT editor.	iPDS-FTRANS option enables file transfer between iPDS and any Inteltec Development System. PL/M, Fortran, Basic, Pascal and Cobol software packages available.	Self-test diagnostic capability, built-in interfaces for high-speed paper tape reader/punch, printer and universal PROM programmer. iMDX557, iAPX resident processor card package is available to upgrade existing iMDX225 series II Development System to Series III. This package supports development of iAPX86/88 processors.	iMDX225	Intel	

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
8080, 8085, 8088, 8048, 8051, all 8-bit Intel microprocessors or microcontrollers	1	2			64						Opt.	
8080A, 8085A, 8086 (iAPX86), 8088 (iAPX88), 8089, 8021, 8022, 8041A, 8741A, 8035, 8048, 8748, 8039, 8049, 8051	1	2	4			1		250			Opt.	Opt.
8080A, 8085A, 8086 (iAPX86), 8088 (iAPX88), 8089, 8021, 8022, 8041A, 8741A, 8035, 8048, 8748, 8039, 8049, 8051	1	2	4		64			250	7.3M		Opt.	
8080A, 8085A, 8086 (iAPX86), 8088 (iAPX88), 8089, 8021, 8022, 8041A, 8741A, 8035, 8048, 8748, 8039, 8049, 8051	8	2	4								Opt.	Opt.
Work station dependent	8	1	2	256		2						Opt.
8086, 8087, 8088, 8085, 8080, 68000, 6809, 6809E, 6502, 6507, Z80B, Z8001, Z8002, NSC-800, 80186, 6510, 65C02, 65802, 80C85, 80C87, 80188, 68008, 68010	8	4	1	256		2						Opt.
TMS320, TMS32010, 80286, 68008, 6301/3, 8031/51, 8048/49, 8035/39, 68000, 68010, 8086, 80C86, 8086/7/8, 80186, Z8001, Z8002, 6502 family, 65C02, 6510, 6809, 6809E, 8080, 8085, 80C85, 8088, 80188, NSC800, Z80.	1	3	x	256	1MB	2	5 1/4	640	10	x	x	x
8080, 8085, 8086, 8087, 8088, 80186, 80188, 6809, 6809E, 68000, 68008, 68010, Z8001, Z8002, NSC-800, 65XX, 16032	4	2	1	1000		2	5 1/4	1.2M	40	x	x	x
TMS320, TMS32010, 80286, 68008, 6301/3, 8031/51, 8048/49, 8035/39, 68000, 68010, 8086, 80C86, 8086/7/8, 80186, Z8001, Z8002, 6502 family, 65C02, 6510, 6809, 6809E, 8080, 8085, 80C85, 8088, 80188, NSC800, Z80.	12 +	7	2	1MB	2MB	3	5 1/4	640	260	x	x	x
8080, 8085, 8086, 8087, 8088, 80186, 80188, 6809, 6809E, 68000, 68008, 68010, Z8001, Z8002, NSC-800, 65XX, 16032	8	2	1	256		2	5 1/4	1.2M	10	x	x	x
TMS320, TMS32010, 80286, 68008, 6301/3, 8031/51, 8048/49, 8035/39, 68000, 68010, 8086, 80C86, 8086/7/8, 80186, Z8001, Z8002, 6502 family, 65C02, 6510, 6809, 6809E, 8080, 8085, 80C85, 8088, 80188, NSC800, Z80.	1	5	x	256	1MB	2	5 1/4	640	10	x	x	x
8080, 8085, Z80, 6809, 6809E, 6502 series 8084, 8086, 68000, Z8001, Z8002	8	4		256		2	5 1/4					Opt.
TMS320, TMS32010, 80286, 68008, 6301/3, 8031/51, 8048/49, 8035/39, 68000, 68010, 8086, 80C86, 8086/7/8, 80186, Z8001, Z8002, 6502 family, 65C02, 6510, 6809, 6809E, 8080, 8085, 80C85, 8088, 80188, NSC800, Z80.	1	3	x	256	1MB	2	5 1/4	640	10	x	x	x



Software Support		Comments	Model	Source	Line
Standard	Optional				
ISIS-PDS disk operating system with relocating macroassembler, and CRT-based editor.	CP/M operating system on disc. Fortran/80, PL/M80, PL/M88/86 and Basic. Multiprocessor emulator functions.	Portable, dual processing capability, expandable using multimodule cards. Bubble memory option.	iPDS	Intel	5
ISIS operating system, credit full screen copier, macroassembler for 8086/88 and 8080/85, linker and loader, debug-86 debugger.	Pascal, Fortran, PL/M, Cobol, Basic, assemblers for 8089, 8048, 8051 families, utility packages for 8080/85/86/87/88/89 support mainframe link software.		IntellecIII	Intel	
ISIS 11 disk operating system; ASM-80 macroassembler for 8080, 8085; credit editor; link and locate utilities.	PL/M-80, Fortran, Pascal, Basic, Cobol, Utilities FSP arithmetic package for 8080 and 8085; AMS-86 macroassembler, PL/M-86, link and locate utilities for 8086; assemblers for 8048 and 8089.	In-circuit emulators for all CPUs.	INTELLEC11-MODEL245	Intel	
ISIS operating system at workstations, MDS-I operating system at network manager.		Network manager provides shared hard disk and printer spooling for use by up to 8 stations.	NDS-I	Intel	
High level language debugging network, management tools, export/import software, Ethernet Protocol.		Network resource manager provides shared Winchester hard disc, Model 740 cartridge disks and spooled line printer interface for work stations. All existing Intel development systems can be upgraded to be NDS-II work stations. Work stations communicate with the network resource manager via 10M bit Ethernet or local net interconnected with coax.	NDS-II	Intel	
CP/M operating system, macro assembler, editor linker, emulation support, mainframe link.	Pascal for system programming; PASCAL compiler for development; 3rd party CP/M software. (Basic, Fortran, C)	Ergonomic terminal, distributed computing and central mass storage for multi-users, multi-processor emulation.	KDS	Kontron	10
CP/M O.S., editor macro-assemblers, linker development libraries, utilities	Pascal-compilers, C-compilers third party CP/M software	Development Station	KDS908-04	Kontron	
UNIX, assemblers, "C" linear, emulator	PASCAL, Fortran	Runs CP/M as task under UNIX	KDS968	Kontron	
UNIX V7, SCCS, csh, make, lint, 200 UNIX utilities, CP/M, CP/NET.	C cross-compilers, PASCAL cross assemblers, third party UNIX and CP/M Software Ethernet to VAX, IBM PCs.	UNIX System	KDS968-07	Kontron	
CP/M, editor, assembler, linear, emulator	PASCAL		KDS980	Kontron	
CP/M O.S., editor macro-assemblers, linker development libraries, utilities	Pascal-compilers, C-compilers, third party CP/M software	Development Station with separate monitor, 5 RS232 GPIB ports	KDS980-02	Kontron	
CP/M operating system, editor utilities (MP/M, CP/Net for multiuser).	Pascal Compilers, Cross assemblers, symbolic debug for emulators.		KDS980	Kontron	
CP/M O.S., editor macro-assemblers, linker development libraries, utilities	Pascal-Compilers, C-Compilers, third party CP/M software	Portable Development System	KPDS	Kontron	

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
TMS320, TMS32010, 80286, 68008, 6301/3, 8031/51, 8048/49, 8035/39, 68000, 68010, 8086, 80C86, 8086/7/8, 80186, Z8001, Z8002, 6502 family, 65C02, 6510, 6809, 6809E, 8080, 8085, 80C85, 8088, 80188, NSC800, Z80.	1	2	x	256	640	2	5 1/4	640	10	x	x	x
TMS320, TMS32010, 80286, 68008, 6301/3, 8031/51, 8048/49, 8035/39, 68000, 68010, 8086, 80C86, 8086/7/8, 80186, Z8001, Z8002, 6502 family, 65C02, 6510, 6809, 6809E, 8080, 8085, 80C85, 8088, 80188, NSC800, Z80.	1	3	x	256	640	2	5 1/4	640	10	x	x	x
TMS320, TMS32010, 80286, 68008, 6301/3, 8031/51, 8048/49, 8035/39, 68000, 68010, 8086, 80C86, 8086/7/8, 80186, Z8001, Z8002, 6502 family, 65C02, 6510, 6809, 6809E, 8080, 8085, 80C85, 8088, 80188, NSC800, Z80.	1	3	x	512	3MB	2	5 1/4	1.2MB	30	x	x	x
8086, 8087, 8088, 8085, 8080, 68000, 6809, 6809E, 6802, 6502, 6507, Z8002, Z8002, Z80B, NSC-800, 6510, 65C02, 80C85, 68008, 80C86, 68010, 80186	8	2	1	64		2						Opt.
80286, 80186, 80188, 8088, 8086	11	3	1	1MB	16MB							
80286, 80186, 80188, 8088, 8086	11	3	1	1MB	16MB	1	5 1/4	1.6M	20MB			
80286, 80186, 80188, 8088, 8086	11	3	1	1MB	16MB				20MB			
68000, 68008	15	2	2	256	14 MB	1	3 1/2, 5 1/4	820K	20 MB			
68010	15	4		512	16 MB	1	3 1/2, 5 1/4	820K	20 MB			
Z80	1	2		64		2	8	1M	5MB		x	
Z80	1	2	2	64			5 1/4				x	
8088	1	1	2	128								
V20	1	1	2	128	1 MB							
8088	1	1	2	128								
V20	1	1	2	128	1 MB							
8088	1	1	2	128	1 MB							
V20	1	1	2	128	1 MB							
Z80	1	2	2	64								
NSC800	1	1	2	64	64							
Z80	1	2	2	64								
NSC800	1	1	2	64	64							
68020	16/32	2/34	1	1 M	16 MB	1	5/8	Opt	40 MB			x
68020	16/32	2/34	1	1 M	32 MB	1	5/8	Opt	40 MB			x
MIL-STD-1750A	4	1	0	128	2Mb	2	8	400/800	40Mb			x
Z80, 68000	1	1	1	256	768	1	5 1/4	800	10MB			
Z80, Z80B, 80186	1	2	1	512	1Mb	2	3.5	814K				
DSP56000, DSP56001	1	1		8				As per Host	As per Host			



Software Support		Comments	Model	Source	Line
Standard	Optional				
DOS O.S., Macro-assemblers, linker, utilities, slave emulator/slave analyzer softwares	C cross-compilers, PASCAL cross assemblers, third party DOS software	Works with users IBM PCXT or AT	KPI/KSE/KSA	Kontron	
DOS O.S., Macro-assemblers, linker, utilities, slave emulator/slave analyzer softwares	C cross-compilers, PASCAL cross assemblers, third party DOS software	IBM PCXT-based development system	KPS100	Kontron	
DOS O.S., Macro-assemblers, linker, utilities, slave emulator/slave analyzer softwares	C cross-compilers, PASCAL cross assemblers, third party DOS software	IBM PCAT-based development system	KPS200	Kontron	
UDOS operating system, editor, macro assemblers emulation support, mainframe link.	Basic, Pascal compilers for development.	Simultaneous multi-position emulation.	2300	Kontron	5
UNIX, XENIX, iRMX286, C, ASM, PASCAL, FORTRAN, COBOL, PLM, ADA	Ethernet Node for local diskless multi-user work station, gateway, development system		DN16	LitMach	
	UNIX, XENIX, iRMX286, C, ASM, PASCAL, COBOL, FORTRAN, PLM, ADA	Same as WN16 series with extensive expansion capability	SA16	LitMach	
	UNIX, XENIX, iRMX286, C, ASM, PASCAL, FORTRAN, COBOL, PLM, ADA	Same as DN16 plus 20Mbyte 3 1/2 inch Winchester Hard Disk Drive	WN16	LitMach	10
PDOS Operating System, Monitor EPROM	PDOS Basic, C, Pascal, Fortran, RUNGEN	STD bus, Desktop, rackmount, industrial grade, nine user slots.	STD1000	Micro-Link	
PDOS Operating System, Monitor EPROM	PDOS Basic, C, Pascal, Fortran, RUNGEN	VMEbus, Desktop, rackmount, industrial grade.	VME1000	Micro-Link	
CP/M, Assembler, Debugger	BASIC, FORTRAN, C		DS22/S	MicroSys	15
CP/M, Assembler, Debugger	BASIC, FORTRAN, C		SB8952-4	MicroSys	
Link to IBM-PC, 8088 Assembler, Linker			STD16-1	MicroSys	
Link to PC Assembler		Language completely integrated into hardware.	STD16-2	MicroSys	20
Link to IBM-PC, ROMable 8088 C-Compiler			STD16-21	MicroSys	
Link to PC, ROMable C Compiler		Language completely integrated into hardware.	STD16-22	MicroSys	
Link to PC, ROMable BASIC Compiler		Language completely integrated into hardware.	STD16-31	MicroSys	25
Link to PC, ROMable BASIC Compiler		Language completely integrated into hardware.	STD16-32	MicroSys	
Link to IBM-PC Z80 Assembler			STD8-1	MicroSys	
Link to PC Assembler		Language completely integrated into hardware.	STD8-2	MicroSys	25
Link to IBM-PC, ROMable Z80 C-Compiler			STD8-21	MicroSys	
Link to PC, ROMable Z80 C Compiler		Language completely integrated into hardware.	STD8-22	MicroSys	
C, Assembly Language, AT&T Unix 5.2	Ada (Verdix) VRTX Real Time Executive	Plug and go kit for any standard Multibus backplane	SDU-I	Microbar	
C, Assembly Language, AT&T Unix 5.2	Ada (Verdix) VRTX Real Time Executive	Single-board Unix engine for Multibus II	SDU-II	Microbar	
MMMON resident monitor/executive	VRTX/1750 Executive	MIL-STD-1750A software development system	MKS1750/C	Mikros	
Assembler, Debugger, C-Compiler			MTI1000	Miller	
CP/M80, Concurrent CP/M86-iRMX86 Operating System		Six-slot portable Multibus	MSC8807	MonSys	
MS-DOS, Assembler		Digital Signal Processor Development System	DSP56000ADS	Motorola (2893, 4754)	

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
M6805, M146805, M6804	1	1	1	8								
MC68HC11, MC6809, MC6801, MC6803, MC68010	1	2	2	32	256	1	5 1/4	655		1		opt.
MC68000	1	1	1	32	256							
MPU6805 Core		1		As Per Host	As Per Host			As Per Host	As Per Host			
MC68000, 68010, 6800, 6809, 6802, 6805, 146805, 6801, 68120	2	2		256						Opt.	Opt.	Opt.
68020, 68010, 68008, 68000, 6801, 6809, 68HC11	8	6		2 MB		1	5 1/4	655K	70 MB			
MC68HC11, MC6809, MC6801, MC6803, MC68000, MC68008, MC68010, MC68020, MC6804, MC6805, MC68120	3	opt.	opt.	384	16	1	5 1/4	655	40Mb	opt.	opt.	opt.
NS32008, NS32016, NS32032	2	2	1	128	128							
NS32008, NS32016	2	2	1	128	512							
NS32008, NS32016, NS32032, NS32132, NS32232	4	4	1	4 M	8				40 MB			x
NS32032	1	2	0	32	32	0						
NS32032	1	2	0	128	128	0						
COP400 Series, NS455	1	3										Opt.
8080, 8085, 8048, 3049, 3050, 3070, Z8	1			64		2		512			Opt.	
NSC800, INS8070, INS8048, INS80C48, 8080, 8085, Z80, COP400	1	2		128		2					Opt.	Opt.
NS32008, NS32016, NS32032, NS32132, NS32232	2	2	1	1 M	8 MB	1	5 1/4	1.2 MB	40 MB			x
μPD70108, μPD70116 (V20/V30)		2	1	320	610	1	8	1M				
μPD70108, μPD70116 (V20/V30)		2	1	320	610	1	8	1M				
μPD70108, μPD70116 (V20/V30)	5	10	2	512	1MB	2	8	1M	32M			
NC4016	1			56		1	5 1/4	360K	10 MB			
12.5 MHz 68000, 10 MHz 68000, 8 MHz 68000, 10 MHz 68010, 12.5 MHz 68010	32	8	2	512	2Mb	1	8	1.6Mb	500Mb			



Software Support		Comments	Model	Source	Line
Standard	Optional				
In host.		Operates as a remote hardware/software development station to a host such as EXORMacs, VME/10.	HDS200	Motorola	5
In host.		Operates as a hardware/software development station.	HDS300	Motorola (4755)	
In host.		Operates as a remote hardware/software development station to a host such as EXORMacs, VME/10.	HDS400	Motorola	
Monitor, Debugger		Evaluation board for the MPU6805 microprocessor core. Provides design development tools for downloading programs from the host computer to user RAM.	MPU6805EVB	Motorola (4284, 4291)	
VERSAdos multiasking, real-time, multiuser, logical I/O file management; Pascal compiler; macro and linking assembler; page, screen and file-oriented editor, symbolic debugger.	Fortran IV.	Optional real-time trace; ROM, RAM and disk autotest at power-on; board-level fault isolation.	M68000 (EXORMacs)	Motorola (2895)	
UNIX System V, C, Pascal	MC68020 Source Level Debugger for C Compiler		SYS1131DVLP	Motorola	10
VERSAdos real-time operating system.	UNIX System V/68 operating system, Pascal, Fortran, "C"		VME/10	Motorola	
TDS Firmware	EXEC	Development board for NS32008, NS32016, NS32032	DB32000	National	
TDS Firmware	MON16, EXEC, UNIX System V	Development board for NS32008, NS32016	DB32016	National	
UNIX System V	EXEC	Integrated Computer Module	ICM3216	National	
IDBG16		In system emulator for NS32016	ISE16	National	
IDBG32		In system emulator for NS32032	ISE32	National	
In host CPU		Microcontroller On Line Emulator; consists of a host CPU, a MOLE Brain Board, and a MOLE Personality board.	MOLE	National	
Disk operating system; Fortran compiler; Basic interpreter; on-board ROM diagnostics, utilities.	Text editor, cross-assemblers.	Optional in-circuit emulators for 8048, Z80; personality modules; Starplex-to-Intel MDS link.	STARPLEX	National	
Disk-based operating system, debugger, text editor, assembler, linker, Fortran, Basic, utilities and diagnostics.	PL/M, Pascal.	Starplex II support packages are identical to those of Starplex.	STARPLEXII	National	15
UNIX System V	EXEC	Series 32000 Multibus target development system	VR32	National	20
	Assembler, C	In-Circuit emulator operational on DEC VAX, Intel Series III and IBM PC.	IE70108-5	NEC	
	Assembler, C	In-Circuit emulator operational on DEC VAX, Intel Series III and IBM PC.	IE70116-5	NEC	
MP/M-86	Assembler, C		MD086FD-10	NEC	
polyFORTH		Development System for the NC4016 Utilizing the NB4000 Beta Board.	ND4000	Novix	
Idris 2.3—a Unix-like O/S with real-time enhancements, poly-FORTH 32, real-time, multiuser, compact O/S.	Absoft's Fortran 77, JMI's C-Exec, and a 68000 assembler from OASYS all run under Idris.	Intelligent Diagnost Front Panel monitors current, voltage, temp., 100MB streaming tape.	OB68K/SYSII	Omnibyte	

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
146805E2; 1802, 1804AC/05AC/06AC; 63P01, 6301V1/X0/Y, 6303R/X/Y, 63L05E0/F1, 6305V0/X0/X1/X2/Y0, 63P05Y0, 6305Y1/Y2, 6309E, 64180, 6500/1/11/12/13/15/16/1E/41/42/43, 65010, 6502/C02/03/04/05/06/07/10; 65C102/112; 6511/12/13/14/15, 65/41, 6800, 68000/008/010, 6801/02/03, 6805E2/E3/F2/S1/S2/S6/U1, 68HC11R4/R8; 68701/U4; 78310, 8001/02/03/04, 80186/188/252/286, 8031/C31, 8032/35/39/40/44/48/C48/49/50/51/C51, 8052, 8080, 8085/C85, 8086/C86, 8088/C88, 8094/95/96/97, 8344/94/95/96/97, 8400, 8601/03/11		1		As Per Host	As Per Host			As Per Host	As Per Host		x	As Per Host
146805E2; 1802, 1804AC/05AC/06AC; 63P01, 6301V1/X0/Y, 6303R/X/Y, 63L05E0/F1, 6305V0/X0/X1/X2/Y0, 63P05Y0, 6305Y1/Y2, 6309E, 64180, 6500/1/11/12/13/15/16/1E/41/42/43, 65010, 6502/C02/03/04/05/06/07/10; 65C102/112; 6511/12/13/14/15, 65/41, 6800, 68000/008/010, 6801/02/03, 6805E2/E3/F2/S1/S2/S6/U1, 68HC11R4/R8; 68701/U4; 78310, 8001/02/03/04, 80186/188/252/286, 8031/C31, 8032/35/39/40/44/48/C48/49/50/51/C51, 8052, 8080, 8085/C85, 8086/C86, 8088/C88, 8094/95/96/97, 8344/94/95/96/97, 8400, 8601/03/11		1		As Per Host	As Per Host			As Per Host	As Per Host		x	As Per Host
1802/4/5/6, 6301/3, 6500/02/C02, 6800/2/8, 6801/3, 6805, 6809E, 68000/008/010/020, 68HC11, 8048/35/39/40/49/50, 8051/31/32/52/C51, 8085/80, 8086/186/286, 8088/188, 8096, Z8, Z80, Z8000, Super8, NSC-800, HD64180	1	2	1	256	640	2	5-1/4	360 K	20 MB	x	x	Opt.
1800 Family, HD64180, 6500 Family, 6800 Family, 68000 Family, 78300, 8048, 8051, 8080, 8085, 8086, 8088, NSC-800, Z8 Family, Z80 Family, Z8000				32	128					x	x	
32032	1	2	1	256	4 MB							
TMS32020	1	0	0	32	1 MB							
TMS320C25	1	1	0	32	256							
TMS32020	1	1	0	32	256							
68000, 68010, 68020, 68030	16	3/16	1	512/8 MB	32 MB	3	3 1/2, 5 1/4	1 MB	170 MB			
68000, 68010, 68020, 68030	16	3/16	1	512/8 MB	24 MB	2	3 1/2	1 MB	85 MB			
68000	3	3	1	512		1	5 1/4	1MB	40MB			
68020	1	2		512	4 MB	2	3 1/2	1 MB	85 MB			
Z80A, B, C, L; NSC800, 80C85, Z80C and 808T In-Circuit Emulators	1	4	2		256						Opt.	Opt.



Software Support		Comments	Model	Source	Line
Standard	Optional				
Assembler, High-Level Language Support, IC Pinout Library		Includes 48 Channel Bus-State Analyzer, In-Place Emulator, Built-In Stimulus Generator, 170 Bus-cycle trace buffer. Used with IBM PC, XT, AT, PS/2 host systems.	UniLab 8420	Orion (4760)	5
Assembler, High-Level Language Support, IC Pinout Library		Includes 48 Channel Bus-State Analyzer, In-Place Emulator, Built-In Stimulus Generator, 2730 Bus-cycle trace buffer. Used with IBM PC, XT, AT, PS/2 host systems.	UniLab 8620	Orion (4760)	
Integrated software controls Analyzer, Emulator, Stimulus Generator, and PROM Programmer, from a single context, has access to MS-DOS programs.	Histogram/Performance Measurement, MS-DOS high-level languages and cross assemblers.	Universal 8/16 Bit Emulator supports 46 processors. Integrated 48-channel bus-state analyzer.	UDL	Orion	
In-circuit emulation, bus-state analyzer, PROM programmer, stimulus generator	Software Performance Analyzer	Requires IBM-compatible PC. Supports more than 120 CPUs	UDL32	Orion	
Series 32000 Cross-Assembler, Linker, Librarian, Loader	C Cross Compiler, Pascal	Uses IBM PC or Compatible as the Host Computer	32032SDS	OwlComp	10
Sample Programs, High Level Language Interface Drivers, Full Debug Monitor, Macro Assembler	TMS32020 Macro Assembler/Linker	PC/XT/AT Plug-in Board, Dual 16-bit A/D, D/A at 50 kHz Throughput.	DSP16	Pacific	
TMS320C25 Sample and Utility Programs, Full Debug Monitor	TMS320C25 Macro Assembler/Linker, Data Acquisition	PC/XT/AT Plug-in Board, Single 16-bit A/D, D/A at 50 kHz Throughput.	TMS320C25	Pacific	
TMS 32020 Sample and Utility Programs, Full Debug Monitor	TMS32020 Macro Assembler/Linker, Data Acquisition	PC/XT/AT Plug-in Board, Single 16-bit D/A, A/D at 50kHz Throughput	TMS32020	Pacific	
PDOS, OS-9, UNIX, VERSAdos	High Level Languages	High-Performance 10-slot chassis assembly.	CS/10	PlesseyMicro	10
PDOS, OS-9, VERSAbus	High Level Languages	Low Cost 5-slot chassis assembly	CS/5	PlesseyMicro	
Monitor	IDEAL, BASIC, FORTH, PSOS, VDOS, COHERENT, PDOS, C, FORTRAN, PASCAL	SASI host adaptor to integral SASI controller, PME WFC-1 disk controller via ST-506 interface for hard disk drives and SA-450 interface for floppy disk drives	PME DS/68-1	PlesseyMicro	
PLUM		For use with Plessey Microsystems' Military/ Ruggedized CPU.	PMV-CS/5	PlesseyMicro	
ROS operating system, self-test, file management, utilities, editor, assembler, linker, locator and communications link.	Relocatable assemblers	Universal development station, hardware/software, emulator/development system. Ports: (4) RS232C, GPIB, Centronics; Portable	IceboxA	RELMS	

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
Z80A, B, C, L; NSC800, 80C85, Z80C, 8085	1	2			256						Opt.	Opt.
Add-on In-Circuit Emulator for Intel development systems.	x				x			x	x			
6500 family.	1	2		16		2					Opt.	x
68000	1	2		256		1	5 1/4					
68000, 68010		2	1	128	1024	1	5 1/4	320	280MB			
68000, 68010		2	1	128	1024	1	5 1/4	320	140MB			
68000, 68010		2	0	512	8192	1	5 1/4	320	280MB			
68000, 68010		2	0	512	8192	1	5 1/4	320	140MB			
68020		2	1	1 MB	4 MB	1	5 1/4	320K	280 MB			
68020		2	1	1 MB	4 MB	1	5 1/4	320K	280 MB			
68020		2	1	2 MB	4 MB	1	5 1/4	1.2 MB	280 MB			
68020		2	1	2 MB	4 MB	1	5 1/4	1.2 MB	280 MB			
6802	1	2	1	61.5		2	8				Opt.	
6809	1	2	1			2	8					
Z8001, Z8002	1	2	1	512	8 MB	1	5 1/4	360K	20 MB			
Z80A/B/C/11, Z8, Super 8; 8085, 80C85, 8048/35/39/40/49/50, 80C48/35/39/40/49/50, 8051/31, 80C51/31; 6801/03, 6809, 6809E, 68HC11; 6301V/X/Y; 6305U/V/X/Y/Z; 7810/11; 78C10/11; 78312, 6502, 65C02	1	1	1	64	64	2	5 1/4	1M		x	x	
Z80A/B	1	1	1	64	64	1	8	1M		x	x	
68000	1	2	1	576	576	1	8	1M		x	x	
8085	1	1	1	64	64	1	8	1M		x	x	
8086, 8087, 8088, 80C86, 80C88, 80186, 80188; $\mu$ PD70108 (V20), $\mu$ PD70116 (V30), $\mu$ PD70208 (V40), $\mu$ PD70216 (V50).	1	2	1	320	320	1	8	1M		x	x	
Z80A/B/H, Z80C, Super-8, Z8, 8085/80C85; 8048/80C48/49/50, 8051/80C51/31, 6801; 6809, 6809E, 68HC11, 6301V/X/Y, 6305U/V/X/Y/Z; 61810, 64180, Z180, 7807/09, 7810/11, 78C10/11, 78310/12, 6502/65C02	1		2	64	64						Opt.	
8086/88, 80C86/88, 80186/188; V20/V30, V40/V50	1		2	320	320						Opt.	
80286, 68000/10/12, 68020	1		2	256	256						Opt.	
68000, 68008, 68010, 6809, 6809E, 6801; 8086/87, 8088/87, 80186, 80188, 8085A; Z80, Z80CMOS, Z8001/2; 1750A, F9450, NSC800	1	2		64-128	768					opt.	opt.	opt.
8086, 8085A, 8080A, 8048, 8049, 8035, 8039, 8021, 8041A, 8022, 6800, 68000, 6802, 6808, Z8000, Z80A	1	2		128						Opt.	Opt.	Opt.



Software Support		Comments	Model	Source	Line
Standard	Optional				
ROS operating system, self-test, file management, utilities	Relocatable assemblers, editor, linker, locator	Ports: (2) RS232C, Centronics. Communications links available for VAX, Intel and CP/M systems. Portable, universal.	IceboxT	RELMS	5
Relocatable Macro cross-assembler, operating system diskette.	Relocatable Macro cross-assemblers: Z80, Z8, Z8000, 6800/01/02, 6500/01/02, 1802/05, NSC800, 9900/95 F8/3870/72, 8051, 8080/85, 6805/146805, 6809, 68000	Doubles assembly speed of Intellec	SPICE	RELMS	
Text editor, two-pass assembler, debugger/monitor in ROM.	PL/65 compiler.	Single step, real-time TRACE; software breakpoints; operational in-circuit emulator.	6500	Rockwell	
Probug, bootstrap monitor	CPM68K Regulus (UNIV Compatible).	5 spare Multibus Slots.	PDS100	SBE	
REGULUS	VRTX, polyFORTH, CP/M-68K	Multiple storage media.	SBE200	SBE	
REGULUS	VRTX, polyFORTH, CP/M-68K	Multiple storage media.	SBE250	SBE	10
REGULUS or UNIX V.2		High-performance, no-wait state MMU.	SBE300	SBE	
REGULUS or UNIX V.2		High-performance, no-wait state MMU.	SBE350	SBE	
Regulus, C	Sys III, Fortran 77	Multiple storage media, no-wait state RAM.	SBE400	SBE	
Regulus, C	Sys III, Fortran 77	Multiple storage media, no-wait state RAM.	SBE450	SBE	
UNIX V.2, C, Fortran 77	Regulus, C	Multiple storage media, no-wait state RAM.	SBE500	SBE	15
UNIX V.2, C, Fortran 77	Regulus, C	Multiple storage media, no-wait state RAM.	SBE550	SBE	
Flex disk operating system. Programming is done in assembly language.	Basic, Pascal, Forth.	Provides 7 additional slots for expansion with Modulas One modules. Select from 25 modules.	802	SBE	
		AS04, Flex.	809	SBE	
CP/M-8000, C, Assembler, DDT Debugger	Pascal, Fortran 77, Basic	Economical Z8000 software development system, Multibus optional.	SBS8000	SingleBoard	
Screen Editor, Line Assembler/Disassembler, Relocatable Assembler Linker, Symbolic Debugger	C, Pascal, Cross Compiler, CP/M Operating System	Universal 8-bit system, built-in 9-inch CRT and ASCII keyboard	SA2000	Sophia	20
Screen Editor, Line Assembler/Disassembler, Relocatable Assembler Linker, Symbolic Debugger	C, Pascal, Cross Compiler, CP/M Operating System	Built-in 5-1/2 inch CRT and ASCII keyboard	SA700-Z80	Sophia	
Screen Editor, Line Assembler/Disassembler, Symbolic Debugger	C, Pascal, Cross Compiler, CP/M Operating System	Built-in 5-1/2 inch CRT and ASCII keyboard	SA700-68K	Sophia	
Screen Editor, Line Assembler/Disassembler, Relocatable Assembler Linker, Symbolic Debugger	C, Pascal, Cross Compiler, CP/M Operating System	Built-in 5-1/2 inch CRT and ASCII keyboard	SA700-8085	Sophia	
Screen Editor, Line Assembler/Disassembler, Symbolic Debugger	C, Pascal, PL/M Cross Compiler, CP/M Operating System	Universal 16-bit system, built-in 5-1/2 inch CRT and ASCII keyboard	SA710	Sophia	
Symbolic Debugger	Assembler	Universal 8-bit to 32-bit in-circuit emulator.	SA98	Sophia	25
Symbolic Debugger	Assembler	Universal 8-bit to 32-bit in-circuit emulator.	SA98	Sophia	
Symbolic Debugger	Assembler	Universal 8-bit to 32-bit in-circuit emulator.	SA98	Sophia	
OS/40 ROM based operating system. Simulated I/O support.	Assemblers, C compilers, Pascal compilers, structured analysis tools, language directed editors (C, Pascal), C/Pascal HLL debug, integration control system.	Complete host based development system. VAX/ULTRIX & VAX/VMS support.	V-Systems	Tektronix	
OS/40 ROM-based operating system; communications firmware; simulated I/O support.	Assemblies/compiles performed on host.	Optional emulator processors and prototype control probes; system designed as a peripheral for a host system.	8540	Tektronix	

Bold face indicates additional data is provided on the page noted.

## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
8086, 8085A, 8080A, 8048, 8049, 8035, 8039, 8021, 8041A, 8022, 6800, 68000, 6802, 6808, F8, 3870, 3872, 3874, 3876, Z8001, Z8002, Z80A, TMS9900, SBP9900, 1802, 6500/1	1	2		128		2				Opt.	Opt.	Opt.
68000, 68008, 68010, 6809, 6809E, 6801; 8086/87, 8088/87, 80186, 80188, 8085A, 8051, 8048, 8021, 8041A, 8022; Z80, Z80CMOS, Z8001/2; 1750A, F9450, 9900/ 9989, 70108/V20, 70116/V30, 7809/ 08/07, 7810/11/16, 78C05/06	8	8		64-128	768	1	8	8	80MB	opt.	opt.	opt.
TMS7xxx, TMS7xCxx		2									y	
SN74AS888, SN74AS890	1	1		40 K	40K		PC	PC	PC	Opt.		
TMS32010, TMS32010-14, TMS32010-25, TMS32011, TMS320C10, TMS320C10-25, TMS320C15, TMS320E15, TMS320C17, TMS320E17	1	3		8	8					x		
TMS32020, TMS320C25	1	3		136	144					x		
TMS34010	1	3		256	256					x		x
TMS370	1	2			640	2	5 1/4	360K	20M		x	x
TMS320, TMS7000					64K							
TMS320, TMS7000					64K							
TLCS-42	1	2	1	384		1	5-1/4		10MB		x	x
TLCS-42	1	2	1	8	8	2	8	1M			x	x
TLCS-47	1	2	1	8	8	2	8	1M			x	x
TLCS-47	1	2	1	384		1	5-1/4		10MB		x	x
TMP8048/35/49/39, TMP80C48/35/49/39/ 50/40	1	2	1	8	8	2	8	1M			x	x
TLCS-48	1	2	1	384		1	5-1/4		10MB		x	x
TLCS-Z80	1	2	1	384		1	5-1/4		10MB		x	x
TMPZ84C00, Z80	1	2	1	64	64	2	8	1M			x	x
TLCS-85	1	2	1	384		1	5-1/4		10MB		x	x
W65C816	1	1	x	16	256	2	3 1/2	800	Opt.		Opt.	Opt.
W65C02, W65C802	1	1	x	16	64	2	3 1/2	800	Opt.		Opt.	Opt.
W65C124	1	1	x	18	18	2	3 1/2	800	Opt.		Opt.	Opt.
W65C134	1	1	x	0	0	2	3 1/2	800	Opt.		Opt.	Opt.
W65C816	1	1	x	256	256	2	3 1/2	800K	40 MB	x	x	x
80186, 80187, 80188, 80286, 80287, V40, V50, 7209, 68HC11, 68000, 68010, 68020, 68881, Z80, Z80B, Z80H, 6301X/Y/V, 6303X/Y/V, 64180	1	1		64/256	1 MB							Opt.



Software Support		Comments	Model	Source	Line
Standard	Optional				
DOS/50 disc based operating system; line-oriented editor; macro assembler with English language diagnostics; linker supervision; communications S/W; simulated I/O support.	Optional emulator processors and prototype control probes; ROM-based powerup systems test; real-time trace.		8550	Tektronix	5
TNIX (UNIX based) operating system, communication F/W, simulated I/O support.	Assemblers, C compilers, Pascal compilers, structured analysis tools, language directed editors (C, Pascal), C/Pascal HLL debug, integration control system.	Complete stand-alone 11/23 or 11/73 UNIX-gated development system	856140 Systems	Tektronix	
Stand-alone device			EVM7000	TI	
TI-Meta-1, Meta Assembler	Cross-Talk	Utilizes either a host PC, or Noncomputing Terminal	SN74AS-EVM-8	TI	
On-board assembler/RASSM	X-ASSM/Linker	Hardware breakpoint and trace, real-time in-circuit emulation. TMS320 first-generation XDS.	TMDS326221TI		
On-board assembler/RASSM	X-ASSM/Linker	Hardware breakpoint and trace, real-time in-circuit emulation. TMS32 second-generation XDS.	TMDS326222TI		10
User Interface (debugger)	Assembler, C Compiler	Use with TI, IBM or IBM-compatible PCs. May also be used stand-alone with a dumb terminal.	TMDS34699-10000	TI	
Assembler/Linker		IBM-PC Based	TMDS3762210TI		
Assembler, simulator, debug monitor, logic tracing with extended data/address probes.		Host independent. Utilizes host computer, requires external 5V supply.	XDS11	TI	
Assembler, simulator, debug monitor, logic tracing with extended data/address probes.		Host independent. Utilizes host computer.	XDS22	TI	
CP/M or MS-DOS	Debugger, Assembler	RTE 42 system evaluates TLCS42 MCU	BM4212A	Toshiba	15
CP/M compatible operating system	Assembler, RTE software	RTE42 evaluator	BM4220	Toshiba	
CP/M compatible operating system	Assembler, PL47 compiler, RTE software	RTE47 evaluator	BM4720	Toshiba	
CP/M or MS-DOS	Debugger, Assembler, or Compiler	RTE 47 system evaluates TLCS-47 MCU	BM4721	Toshiba	
CP/M compatible operating system	Assembler, RTE software	RTE48 evaluator (1 box type)	BM4820	Toshiba	
CP/M or MS-DOS	Debugger, Macro-Assembler	RTE 48 system evaluates TLCS-48 MCU	BM4821	Toshiba	20
CP/M or MS-DOS	Debugger, Macro-Assembler	RTE 80 system evaluates TLCS-Z80 MPU	BM8021	Toshiba	
CP/M compatible operating system	Macroassembler, RTE software	RTE80 real-time emulator. BM1020 is real-time controller	BM8022	Toshiba	
CP/M or MS-DOS	Debugger, Macro-Assembler	RTE 85 system evaluates TLCS-85 MCU	BM8521	Toshiba	
Toolbox In-Circuit Emulation Software	Assemblers, C Compilers	W65C816 In-Circuit Emulator.	ICE-MPUS	WDC	
Toolbox In-Circuit Emulation Software	Assemblers, C Compilers	W65C02, W65C802 In-Circuit Emulators.	ICE MPUS	WDC	25
Toolbox In-Circuit Emulation Software	Assemblers, C Compilers	W65C124 In-Circuit Emulators	ICE 124	WDC	
Toolbox In-Circuit Emulation Software	Assemblers, C Compilers	W54C134 In-Circuit Emulator	ICE 134	WDC	
Toolbox In-Circuit Emulation Software	Macro-Assembler, C Compiler, Pascal Compiler, BASIC, FORTH, FORTRAN	Apple IIgs Host with RS-232 interface for any application software development host.	Toolbox	WDC	
MS-DOS Standard Operating System Interface	C and Pascal Compilers, Source-level Debuggers, Assemblers, Linkers, Symbolic Debug Optional Software	Computer (AT-class) controlled emulator with 256,000 breakpoints and performance analysis	ERX-SERIES	ZAX	

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## MPU DEVELOPMENT SYSTEMS (Cont'd)

Supported CPUs	Maximum No. of Users Stations	Communication Ports		User RAM		Floppy Disk			Hard Disk	Logic Analyzer	PROM Programmer	Printer
		Serial	Parallel	Supplied (Kbytes)	Maximum Capacity (Kbytes)	No.	Size (in.)	Capacity (Kbytes)	Capacity (Kbytes)			
8048, 8031, 8032, 8051, 8052, 8085, 8086, 8087, 8088, 80186, 80188, V20, V30, 7209, V40, V50, 6809, 6809E, 68000, 68010, Z80, Z80B, Z80H	1	2		64/128	16 MB						x	Opt.
8048, 8086/8088/8087, 68000/68010, 68008, 6809/6809E, Z80/Z80B/Z80H, 8085, 80186/80188, V20/V30	8	2		64/128	16MB						8048	opt.
80186	4	4	1	512	1 MB	1	5.25	360	20 MB		Opt.	
80186	2	2	1	512	1 MB	1	5.25	360	10 MB		Opt.	
80186, 80286	4	4	1	1 MB	1 MB	1	5.25	360	40 MB		Opt.	
8088 (5 or 8 MHz)	3	5	2	128	1000	2	3 1/2	2100		avail	avail	
8088	1	1	2	256	1000	3	5 1/4	2100	20000	Opt.	Opt.	
8088 (5 or 8 MHz)	1	1	2	256	1 MB	3	5 1/4	2.1 MB	20 MB		Opt.	
8088/80188	1	Varies	Varies	128	1000	PC	PC	PC	PC	Opt.	Opt.	
8088 (5 or 8 MHz)	1	1	2	128	1000	3	5 1/4	2100	20000		opt.	
Z8000, Z80, Z8	8 to 24	eight RS232C	one	256	1Mb				36M	Opt.		Opt.
Z8000, Z80, Z8	8 to 24	eight RS232C	one	1Mb	4Mb				128M	Opt.		Opt.
Z8000, Z80, Z8	8 to 24	eight RS232C	one	1Mb	4Mb				320M	Opt.		Opt.



Software Support		Comments	Model	Source	Line
Standard	Optional				
CP/M, MS-DOS, VMS, ULTRIX, Standard Operating System Interface	C and Pascal Compilers, Source-level Debuggers, Assemblers, Linkers, Symbolic Debug Optional Software	CRT or Host Computer controlled emulator with four hardware and eight software breakpoints, 8048 Built-in standard PROM programmer.	ICD-SERIES	ZAX	5
CP/M, MS-DOS, VMS	C and Pascal Compilers, Assemblers, Linkers, Symbolic Debug	CRT or Host Computer (PC, MicroVax I, etc) controlled emulator with 4 hardware and 8 software breakpoints	ICD178/278	ZAX	
Concurrent DOS	Drivers available	Sockets for up to 256 KB EPROM, SCSI, clock/calendar, OMTI controller six open Multibus slots, removable front panel, and 300 W switching power supply. Monitor and keyboard included.	ZX96/C-DOS	Zendex	
CP/M	Drivers Available	Sockets for up to 256 KB EPROM, SCSI, clock/calendar, OMTI controller, six open Multibus slots, removable front panel, 300 W switching power supply. Monitor and keyboard included.	ZX96/CPM	Zendex	
RMX, System Debug Monitor	PLM, C, Drivers available	Sockets for up to 96 KB EPROM, SCSI, OMTI controller, six open Multibus slots, removable front panel, and 300 W switching power supply. Monitor and keyboard included.	ZX96/RMX	Zendex	
Source software and software development tools available	Level 3 or Level 4 software	Multi-user, multitasking, real-time operating system. Includes on-line software development tools.	STD polyFORTH	Ziatech	10
PC DOC 3.1, Ziatech Bios, Host development software		STD DOS is an innovative STD Bus adaptation of IBM PC DOS 3.1 which functions both in development and target environments.	STD DOS	Ziatech	
PC-Dos, Ziatech Multi-Dos BIOS, VRTX, Tracer, Board Support Package (BSP)		Combines the strengths of PC-DOS and VRTX. Provides effective operating support services such as file management and peripheral equipment control.	STD Multi-Dos	Ziatech	
PC Std, LOCATE, DBUG 88		STD PDS provides multi-level on-line help screens and user-definable soft keys for development convenience.	STD PDS	Ziatech	
PC STD, LOCATE, DBUG 88, VRTX, ZT 8806 Board Support Pack. (BSP)		Popular, multitasking real-time operating system. Task scheduling via priorities, time slicing, intertask communication, and semaphores.	STD VRTX	Ziatech	
ZEUS description incl., C, Assembler	Fortran, Cobol, Basic	Expandable system; optional in-circuit emulators; ZSCAN family, EMS8000	Model 11	Zilog	
ZEUS description incl., C, Assembler	Fortran, Cobol, Basic	Expandable system; optional in-circuit emulators; ZSCAN family, EMS8000	Model 21	Zilog	
ZEUS description incl., C, Assembler	Fortran, Cobol, Basic	Expandable system; optional in-circuit emulators; ZSCAN family, EMS8000	Model 31	Zilog	

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# Experience Counts.



## EZ-PRO Emulators

Experience quick delivery, easy operation, fast development schedules. EZ-PRO® users reap the benefits of the C language fully integrated with advanced emulation tools, including precedence triggering, Deep Trace™, on-line code revisions, and performance analysis tools.

In addition to IBM® PC-XT/AT, hosts include IBM Personal

System/2™, Macintosh II™, VAX™, MicroVAX™, and Sun Workstation®.

EZ-PRO users also have the advantage of the best post-sales support in the industry.

They know that their emulators are covered by

American Automation's 5-year limited warranty.

Experience counts. Now with over 10 years experience, American Automation has designed more emulators than anyone. Count on EZ-PRO to provide the most cost/effective development support.

<b>Intel:</b> 8031 8032 8086 8035 8088 8039 80186 8344 80188 8048 80286 8049 8050 8051 8085A 8085A2 8096/97	<b>Motorola:</b> 6800 68B00 68HC11A2 6801 68HC11A8 6802 68B02 68000 146805E2 68008 6803 68010 6808 68B08 6809 6809E 68B09 68B09E	<b>Hitachi:</b> 6301R 6301V1 6301X 6301Y 6303R 6305V 63705 6309 6309E 64180R0 64180R1	<b>Rockwell:</b> 6502 6503 6504 6505 6506 6507 6512 6513 6514 6515	<b>RCA:</b> 1802 1805 1806 CDP6805C4 CDP6805C8 CDP6805D2 CDP6805E3	<b>Zilog:</b> Z80A Z80B Z80H Z180 Z8001 Z8002
				<b>Harris:</b> 80C86 80C88	<b>NEC:</b> V20 V40 V30 V50
				<b>National:</b> NSC800	<b>Signetics:</b> 8X300 8X305

...AND MORE

\*Assumes EZ-PRO Development Station connected to MSDOS host.

**american automation** 

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## HILEVEL UPDATE

# MICROCODE?... HILEVEL SYSTEMS!

## Development Systems Reduce Design Time

### Stand-Alone Systems Cut Design Time

If you are developing microcode programs, calling the toll-free number below could be the most important action you will take to assure your project is completed on time. Use the number to arrange a demonstration of the DS/CS Series of microcode development systems and see how they can reduce your development time.

According to Gary Pollard, Product Marketing Manager, the DS/CS Series development workstations "feature multiple processors that operate over twice as fast as older, single processor, CP/M\* based development systems."

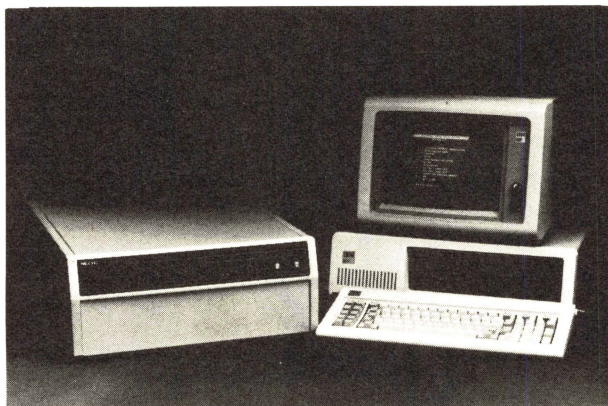
Don't be fooled by misleading access time claims. Call HILEVEL Applications and request the new Application Note, "When 25 nsec is faster than 10 nsec."

All models in the DS/CS Series provide both an MS (or PC)/DOS\* CPU and a bit-slice processor. Tasks are divided between the processors to assure optimum system performance. The MS/DOS CPU handles microcode assembly, file management, symbolic debug, and high level test language operations. The faster bit-slice processor provides control for emulation and analysis operations, performing operator commands almost instantly. This eliminates the frustration of waiting for the system to perform...as well as the wasted time.

The multiple processors also allow multi-tasking operations. For example, use your favorite word processing program to write your progress report while the bit-slice processor is tracing down that final elusive bug.

Designed to make you efficient.

Relocatable and linking macro-meta assemblers, multi-processor architecture, high-speed WCS, high performance logic analysis, transmission line cables to your target, and menu driven operator interface combine to make the DS/CS the most efficient stand-alone development system available.



Development System features 35 MHz analyzer to support all bit-slice and application specific processors.

*"Only HILEVEL can provide a development system with the speed to support all the new bit-slice and bipolar processors that have been recently announced."*

## Integrated Software Provides a Total Development and Test Solution for your Microprogrammed Designs.

### Fast Macro-Meta Assembler Reduces Waiting Time.

The HILEVEL Macro-Meta Assembler allows you to develop definitions and source files to match your unique hardware. This program (known as HALE: HILEVEL Assembly Language Environment) provides relocation and linking features to allow software modules to be developed and assembled independently. Written in C, these programs will assemble your code at over twice the speed of competitive Meta assemblers.

For PC or VAX based systems, these assemblers are part of a full complement of utility, upload/download, and test language programs.

For previous users the assemblers are fully AMDASM\* and Microtec compatible.

### Software Programs Enhance Debug Abilities.

Over twenty HILEVEL software packages are available for use on either the DS/CS Series of development systems, your PC, your VAX, or other mini-computers. In addition to the HALE™ assembler, programs include symbolic debug, upload/download routines, VT100\* terminal emulation, PC utilities, EPL (EMULYZER Programming Language), and demonstration programs.

Use the EPL program with your development system for extended automatic testing of the completed design. This test language interpreter allows you to execute command files. These files may contain an entire test program with calls to assembled object files. A single execute instruction allows multiple test sequences to be executed, the results analyzed, and the operator prompted for the next action.

### Full Support for Bit-Slice and Bipolar Processors

Only HILEVEL Can Provide a development system with the speed to support all the new bit-slice and bipolar processors that have been recently announced.

In-circuit emulators are available for most of the new bipolar processors. These emulators may be used independently or in conjunction with your development station to support the 29116, 2910, TMS320, 1032, or NCR32. Support is also available for the new 29PL141, AS888 and 29300 families recently announced and for the 29400 to be introduced in 1986.

Designing a custom, application specific processor? Using a VHSIC implementation of MIL-Std-1750A? We can help. Call our application specialist at the number below with your unique needs.

### Microcode Development on your Computer.

Own a VAX\*? An IBM-PC\*? A TI\* Personal Computer? HILEVEL EMULYZERS are available with software programs that convert your present computer to a development system. This allows you to obtain the benefits of the EMULYZER™ with its powerful bit-slice processor and use your computer instead of the MS/DOS processor furnished in the HILEVEL stand-alone development systems.

Are you planning to buy a CP/M computer for your lab? Probably not...therefore, why purchase a microcode development system with a CP/M processor? Instead, use the power you already have in your VAX or PC to complement the high-speed performance of the DS Series EMULYZERS for HILEVEL. Your computer, an EMULYZER, and the appropriate HILEVEL software package give you all the features of our stand-alone systems...without duplicating computing power!

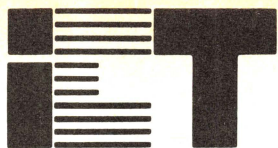
**HILEVEL**  
TECHNOLOGY, INC.

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Irvine, CA 92718  
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Call Toll Free: **1-(800)-HILEVEL**  
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## PDS-1 PEEL<sup>TM</sup> Development System Features

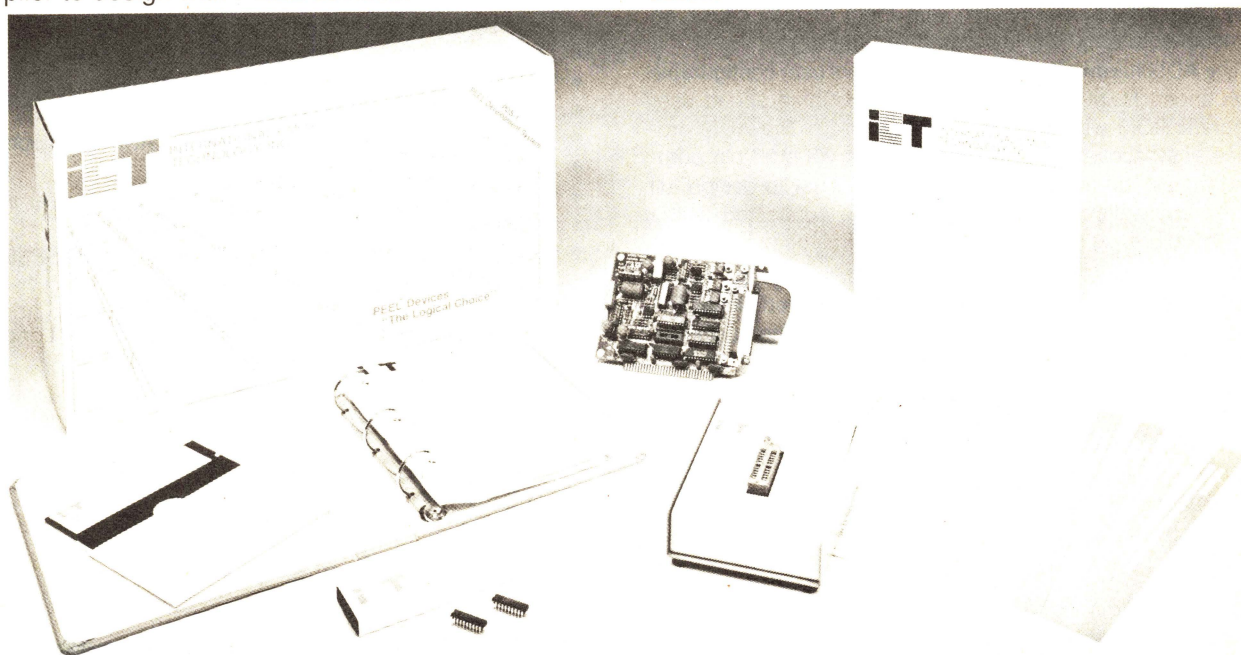
- **Development System for PEEL Devices**
  - Editor, logic assembler, translator programmer, and tester all in one system
  - Runs on PC-compatible computers
- **Conventional PLD Programmer Functions**
  - Program, Load, Verify, Secure
- **APEEL<sup>TM</sup> Boolean Logic Assembler**
  - Supports all advanced features of PEEL devices
  - "PALASM\*-like" sum-of-products equations
  - "ABEL\*-like" macro cell definitions
  - Logic simulation
- **Translates Standard PLDs to PEEL Devices**
  - Loads PLD or reads JEDEC file
  - Automatically translates to PEEL device
- **Built-in File Editor**
  - Edit source, JEDEC, or test-vector files
- **Enhanced Logic-Test Capabilities**
  - Tests device in socket to JEDEC test vectors
  - Special features: single step, loop, capture
- **Expandable and Accessible**
  - New features and devices supported with software updates
  - No copy protection

### General Description

The PEEL<sup>TM</sup> Development System is a powerful, yet inexpensive, PC-based system for designing with PEEL (Programmable Electrically Erasable Logic) devices. The PDS-1 is a personal PLD work-station providing everything needed to implement your logic designs from concept to silicon. Several options for designing with PEEL devices are available with the PDS-1. For example, an existing PLD design (i.e., a PAL\* or EPLD JEDEC file) can be automatically translated and programmed into a PEEL device. Additionally, the translation capability allows you to use your present PLD logic assembler or compiler to design with PEEL devices.

To fully support the advanced features of PEEL devices, the PDS-1 also provides the tools needed to design from start to finish, including a built-in word processor for design entry and editing, the APEEL<sup>TM</sup> boolean-logic assembler, a complete PEEL-device programmer and enhanced logic tester.

The capabilities of the software-controlled programmer will be expanded as new devices are released by ICT. Registered owners are enrolled in the ICT software update service and receive programmer/development-software updates.



PDS-1, PEEL Development System



# Digital Signal Processor Development System

## DSP56000ADS

### For DSP56000 Family Products

The DSP56001-based Application Development System (ADS) is a three-component development tool for designing, debugging, and evaluating DSP56000 and DSP56001 target system equipment. The ADS simplifies evaluation of the user's prototype hardware/software product by making all of the essential DSP56000 timing and I/O circuitry easily accessible.

An IBM PC using the MS-DOS operating system acts as the medium between the user and the DSP56000 hardware. The three ADS components are an Application Development Module (ADM) board, an IBM PC bus interface board, and a MS-DOS based user interface program that runs on the IBM PC and interacts with the user, controlling as many as eight ADMs simultaneously. Using a low cost personal computer significantly decreases the overall hardware complexity and cost of development while increasing the capabilities of the system.

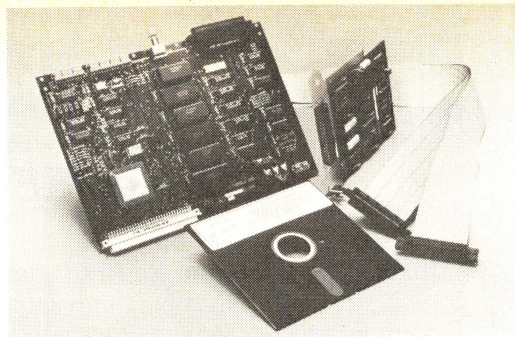
DSP algorithm development is simplified with features such as multiple MS-DOS file I/O capability to the ADM under DSP56001 program control and immediate access to a hex/fractional/decimal calculator. The ADS is fully compatible with the DSP56000SASMA design-in software package and may act as an accelerator for testing DSP56000 family algorithms.

DSP programs may be executed real-time, single instruction traced, or multiple instruction stepped with registers and/or memory block contents displayed.

As many as 99 conditional and/or unconditional breakpoints may be placed in ADM program memory. Breakpoints may have actions associated with them or may cause an immediate halt and display of enabled registers.

The ADM hardware provides 8K words of user configurable high speed RAM and 1K to 4K words of high speed user program ROM with no wait states required. The ADM provides easy access to all DSP56001 pins via a 96 pin euro-card female connector. This enables the user to design full speed application circuits which may be connected to the DSP56001 using standard euro-card prototype boards.

Two additional connectors provide easy access to the DSP56001 on-chip peripheral circuits. Dedicated Host/DMA and SSI/SCI connectors allow easy access to the host interface port as well as both serial interface ports.



Jumper options allow changing clock inputs, DSP56001 operating mode on reset, reconfiguration of RAM partitioning between Program, X or Y memory spaces, and address relocation of RAM and/or ROM.

Hardware features include:

- Full speed operation at 20.48 MHz
- Multiple ADM support with programmable ADM addressing
- 8K words of configurable RAM for DSP56000/1 code development
- 1K words of monitor ROM expandable to 4K words
- 96 pin euro-card connector for accessing all DSP56001 pins
- Separate connectors for accessing serial or host/DMA ports
- Stand-alone operation of ADM after initial development
- No external supply required when connected to IBM PC

The minimum hardware requirements for the DSP56000 ADS User Interface Program include:

- IBM PC, XT, or AT with 384K bytes of RAM
- PC-DOS/MS-DOS v2.1 or later.

Software features include:

- Single/multiple stepping through DSP56000 object programs
- Conditional or unconditional breakpoints
- Program patching using a single-line assembler/disassembler
- Session and/or command logging for later reference
- Loading and saving of files to/from ADM memory
- Macro command definition and execution
- Display enable/disable of registers and memory
- Debug commands that support multiple ADM development
- Hexadecimal/decimal/binary calculator
- MS-DOS system commands from within ADS user interface program
- Multiple MS-DOS input/output file access from DSP56000 object programs

Software packages available are listed on the last page of this section.



# Hardware/Software Development Stations

## HDS-300

### For M68000/M6800-Based Systems

#### For 8-, 16- and 32-Bit MCU and MPU Development.

The HDS-300 is the most powerful development support tool in the Motorola line. It serves as the key link between a Host system and a target system under development. It provides a quick, user-friendly way to reduce engineering costs and to minimize project risk. It represents a new generation in development support instrumentation.

The HDS-300 can operate either stand-alone or with a development Host system. With the Hosted HDS-300 System you develop your software on an RS-232-C compatible development host, then download the object code into the HDS-300 for target emulation and debug. When performing source-level debug, a hosted HDS-300 displays source and compiled code to allow easy modification or step-by-step analysis at either level. The HDS-300 one-line assembler/disassembler speeds up software development; its internal Bus State Monitor provides trace history and real-time trace analysis with disassembly. Window support allows easy examination of the trace history and, to streamline debugging and code verification, a versatile breakpoint capability allows up to 6 breakpoints to be active simultaneously.

All these features, plus user macros, emulation memory, target status analysis, thorough on-line HELP screens and user-friendly "windows" make the development process simpler and more effective.

An HDS-Development Station consists of two separate entities — a Control Station and an Emulator Module. The Control Station contains the common control, logic, and memory functions needed to control emulation. The Emulator Module contains the specific MPU/MCU which the station is to emulate, together with supporting control circuitry. Hence, there are different Emulator Modules for different target MPU/MCUs. The Emulator Modules for various Motorola MPU/MCUs are listed in the tables that start on the fourth page of this section.



HDS-300

## HDS-200

### For M6804/05-Based Systems

#### For Lower-Level Tasks

Not every development project demands the performance capabilities of the full-function HDS-300 System. For less demanding development tasks, Motorola offers the HDS-200 Hardware Development Station.

The HDS-200 Hardware Development Station is the tool of choice for low-cost, real-time emulation for the 8-bit M6804, M6805, and M146805 MCU Families.

The HDS-200 features real-time emulation, sixteen prioritized and programmable breakpoints, line-by-line assembler/disassembler, program trace display, HELP commands, and a transparent operation mode. All these features are designed to assist your hardware and software development . . . and to do it cost-effectively.

To support low-cost real-time emulation for M6804, M6805, M68HC05, and M146805 MCU designs, Motorola offers a number of emulators for the HDS-200. These modules provide a quick interconnection between the HDS-200 and the target system. By plugging directly into the MCU/MPU socket on the target system, these emulator modules provide the proper electrical connections and interfaces to duplicate the performance of the normal MCU/MPU function. The appropriate Emulator Modules for various MCUs are listed in the tables that start on the fourth page of this section.

## HDS-300 Support Products

### System Performance Analyzer

For 32-bit MC68020 designs, the System Performance Analyzer (SPA) offers advanced bus analysis capability to augment the HDS-300's Bus State Monitor (BSM). The SPA supports the MC68020 MPU design at clock rates of up to 20 MHz, and comes with a trace history memory and a state controller. The SPA has the flexibility to program up to 16 independent trace blocks, set seven different breakpoints, trigger on up to four complex 8-bit count events, and capture 4000 qualified bus cycles.

### Source Level Debugger

This debugging tool is available with the hosted HDS-300. Source Level Debug (SLD) enables you to debug code written in the popular "C" high-level language. The window-based debugger allows you to view and manipulate the target system via source code. Key features of the SLD include single stepping, free running execution, restart execution from the beginning of the application, and the ability to set breakpoints at the source line, function, or physical address. With it, you can quickly see how the compiler handled your source code, instruction by instruction, then reprogram where necessary.



# Software Development Host

Motorola offers the VMEsystem 1131 Open System Development Host. In addition, a number of non-Motorola hosts can be used with the HDS-300 Station, notably the VAX Minicomputer and a variety of native microcomputers.

## VMEsystem 1131 Multi-User Development Host

(Model SYS1131DVLP)

The SYS1131DVLP is an extremely powerful MC68020-based software development host system supporting both hardware and software design efforts. The "DVLP" integrates the software development environment with the HDS-300 in a complete development system. And because the DVLP provides the industry-preferred SYSTEM V/68 UNIX operating system and software control methodologies, this system is widely applicable to the general milieu of development projects. The DVLP system includes a selection of 8- and 16-bit software cross development packages:

<b>M68NNXBPASMLK</b>	M68000/008/010 Macro Structured Assembler, Linkage Editor, Pascal Compiler and Run-Time Libraries
<b>M68N2XBCC</b>	MC68000/008/010 Cross C Compiler
<b>M68NEXBCC11A</b>	MC68HC11 Cross C Compiler
<b>M68NCXBLINKER</b>	Portable Cross Linkage Editor
<b>M68NCXBRASM</b>	M6800 Family Portable Cross Assembler
<b>M68NNXBTLKT</b>	VERSA Dos Tool Kit (Supports code migration between System V/68 and VERSA Dos operating systems)
<b>M68NNXBSV131B</b>	System V/68 Unix operating system, 1-8 users

Additional software is available separately:

<b>M68N2XBASM</b>	MC68020 Macro Assembler
<b>M68NNXBCC20B</b>	MC68020 Cross C Compiler, 1-8 users
<b>M68NNXBSDL20</b>	MC68020 Source Level Debug
<b>M68NNXBSDL00</b>	MC68000/008/010 Source Level Debug
<b>M68NEXBSLD11</b>	MC68HC11 Source Level Debug Object for C Compiler

The DVLP system utilizes the 32-bit MC68000 microprocessor and the MC68881 floating point coprocessor, both running at 16 MHz. The system not only supports multiple users simultaneously, but it will support simultaneous debug sessions utilizing multiple HDS-300 control stations using any mix of HDS-300 emulators. The DVLP system is based on Motorola's VMEmodules and includes the following components:

<b>MVME131XT</b>	MC68020 and MC68881, 16K bytes of cache, and paged memory management
<b>MVME204-2</b>	2M bytes memory board with byte parity checking, using the high-speed private memory bus with the MVME1131
<b>MVME320-1</b>	Winchester/Floppy controller
<b>MVME350</b>	Streaming tape controller
<b>MVME834</b>	70M byte Winchester/1M byte 5-1/4" Floppy/Streaming Tape mass storage module

# Evaluation Modules

Need to evaluate the performance of a particular Motorola MPU or MCU? The line of Evaluation Modules lets you do this quickly, easily and inexpensively.

Requiring only an external power supply and an RS-232C terminal, Motorola EVMs support the 16-bit MC68000 microprocessor, and a number of the most popular 8-bit MPUs and MCUs.

All Motorola EVMs feature an on-board programmer for EPROMs and EEPROMs (when applicable), a monitor/debugger using SYMbug-type syntax, a one-line assembler/disassembler, dual memory maps, target MPU I/O, power-on reset, user reset/abort and an external clock input.

Evaluation Modules/Boards								
M68701EVM	M68705EVM	M68HC04EVM	M68HC05EVM	M68HC11EVM	M68HC99EVM	M1468705EVM	M68HC11EVB	MEX68KECB

### Device Supported

MC6801	•							
MC6801U4	•							
MC68701	•							
MC68701U4	•							
MC6803	•							
MC6803U4	•							
MC6804J1/J2			•					
MC6804P2			•					
MC68704P2			•					
MC68HC04J2/P3			•					
MC6805P2/P4/P6		•						
MC6805R2/R3	•							
MC6805U2/U3	•							
MC68705P3/P5	•							
MC68705R3	•							
MC68705U3/U5	•							
MC146805F2						•		
MC146805G2						•		
MC1468705F2						•		
MC1468705G2						•		
MC68HC05C2/C3/C4/C8			•					
MC68HC05L6			•					
MC68HC805C4			•					
MC68HC11A0/A1/A8				•			•	
MC68HC811A2				•			•	
MC68HC99					•			
MC68000								•



# Development System Selection Guide

MPU or MCU	Emulator (Standard Memory)	Control Station	Software Options		Other Options	
			Cross Software	Source Level Debugger	Emulator Memory	System Performance Analyzer
MC68020    20 MHz     25 MHz	M68020HM3C-1 (64KB)	M68HDS300	M68NNXBCC20A,B,C	M68NNXBSDL20	M68020MEM2,3	M68HDS300SPA
	M68020HM3C-2 (256KB)	M68HDS300	M68NNXBCC20A,B,C	M68NNXBSDL20	M68020MEM3	M68HDS300SPA
	M68020HM3C-3 (1MB)	M68HDS300	M68NNXBCC20A,B,C	M68NNXBSDL20	—	M68HDS300SPA
	M68020HM3C-4 (64KB)	M68HDS300	M68N2XBASM	M68NNXBSDL20	M68020MEM2,3	M68HDS300SPA
	M68020HM3C-5 (256KB)	M68HDS300	M68N2XBASM	M68NNXBSDL20	M68020MEM3	M68HDS300SPA
	M68020HM3C-6 (1MB)	M68HDS300	M68N2XBASM	M68NNXBSDL20	—	M68HDS300SPA
MC68010	M68010HM3A,B,C	M68HDS300	M68N2XBCC M68N2XBASM	M68NNXBSDL00	M68DHS3EMM1,2,3	
MC68008	M68008HM3A,B	M68HDS300	M68N2XBCC M68N2XBASM	M68NNXBSDL00	M68DHS3EMM1,2,3	
MC68000	M68000HM3A,B,C	M68HDS300	M68N2XBCC M68N2XBASM	M68NNXBSDL00	M68DHS3EMM1,2,3	
MC68HC11	M68HC11ANHM3A,B	M68HDS300	M68NEXBCC11A,B,C	M68NEXBSDL11	M68DHS3EMM1	
MC6801,U4	M6801HM3A	M68HDS300	M68NCXBRASM		M68DHS3EMM1	
MC6803,U4	M6801HM3A	M68HDS300	M68NCXBRASM		M68DHS3EMM1	
MC6809,E	M6809HM3A	M68HDS300	M68NCXBRASM			
MC6804J2,P2	M6804P2HM	M68HDS201A	M68NCXBRASM			
MC68HC05C4,8	M68HC05CHM3A,B M68HC05CHMA,B	M68HDS300 M68HDS201A	M68NCXBRASM			
MC6805P2	M6805P234HM	M68HDS201A	M68NCXBRASM			
MC6805R2,3	M6805RU23HM	M68HDS201A	M68NCXBRASM			
MC6805S2	M6805S2HM	M68HDS201A	M68NCXBRASM			
MC6805U2	M6805RU23HM	M68HDS201A	M68NCXBRASM			
MC146805E2	M146805E2HM	M68HDS201A	M68NCXBRASM			
MC146805F2	M146805F2HM	M68HDS201A	M68NCXBRASM			
MC146805G2	M146805G2HM	M68HDS201A	M68NCXBRASM			

# Development Systems Part Number Descriptions

## Software Development Host

SYS1131DVLP                      SYS1131 Including 8-, 16-Bit Languages and Tools

## Hardware/Software Development Station

M68HDS201A                      HDS-200 Control Station  
M68HDS202A                      220 V Version of HDS-200 Control Station  
M68HDS300                        HDS-300 Control Station  
M68HDS302                      220 V Version of HDS-300 Control Station

## Source Level Debugger

M68NEXBSLD                    M68HC11 Source Level Debug Object for C Compiler on SYS1131DVLP  
M68NNQSSLD11                  M68HC11 Source Level Debug Source Code  
M68NNXBSDL00                  M68000,008,010 Source Level Debug for HDS-300 and SYS1131DVLP  
M68NNXBSDL20                  M68020 Source Level Debug for HDS-300 and SYS1131DVLP

## Emulator Module (POD)

M146805E2HM                   MC146805E2 Emulator Module and Software for HDS-200  
M146805F2HM                   MC146805F2 Emulator Module and Software for HDS-200  
M146805G2HM                   MC146805G2 Emulator Module and Software for HDS-200  
M68HC05CHMA                   MC68HC05C4,8 Emulator Module with DIP Cable for HDS-200  
M68HC05CHMB                   MC68HC05C4,8 Emulator Module with PLCC Cable for HDS-200  
M68HC05CHM3A                   MC68HC05C4,8 Emulator Module with DIP Cable for HDS-300  
M68HC05CHM3B                   MC68HC05C4,8 Emulator Module with PLCC Cable for HDS-300  
M68HC11ANHM3A                   MC68HC11A Emulator Module with DIP Cable for HDS-300  
M68HC11ANHM3B                   MC68HC11A Emulator Module with PLCC Cable for HDS-300  
M68000HM3A                    MC68000 Emulator/Bus State Monitor Module with DIP Cable for HDS-300  
M68000HM3B                    MC68000 Emulator/Bus State Monitor Module with PLCC Cable for HDS-300  
M68000HM3C                    MC68000 Emulator/Bus State Monitor Module with PGA Cable for HDS-300  
M68008HM3A                    MC68008 Emulator/Bus State Monitor Module with DIP Cable for HDS-300  
M68008HM3B                    MC68008 Emulator/Bus State Monitor Module with PLCC Cable for HDS-300  
M6801HM3A                      MC6801,701,01U4,701U4,03,03U4 Emulator Module for HDS-300  
M68010HM3A                    MC68010 Emulator/Bus State Monitor Module with DIP Cable for HDS-300  
M68010HM3C                    MC68010 Emulator/Bus State Monitor Module with PGA Cable for HDS-300  
M68020HM3C-1                   20 MHz MC68020 Emulator Module with 64K RAM and PGA Cable for HDS-300  
M68020HM3C-2                   20 MHz MC68020 Emulator Module with 256K RAM and PGA Cable for HDS-300  
M68020HM3C-3                   20 MHz MC68020 Emulator Module with 1M RAM and PGA Cable for HDS-300  
M68020HM3C-4                   25 MHz MC68020 Emulator Module with 64K RAM and PGA Cable for HDS-300  
M68020HM3C-5                   25 MHz MC68020 Emulator Module with 256K RAM and PGA Cable for HDS-300  
M68020HM3C-6                   25 MHz MC68020 Emulator Module with 1M RAM and PGA Cable for HDS-300  
M6804P2HM                      MC6804 Emulator Module and Software for HDS-200  
M6805P234HM                   M6805P2 and M68705P3 Emulator Module and Software for HDS-200  
M6805RU23HM                   MC6805R2,R3,U2,U3 Emulator Module and Software for HDS-200  
M6805S2HM                      MC6805S2 Emulator Firmware Cartridge and Diskettes for HDS-200  
M6809HM3A                      MC6809 Emulator Module and Software for HDS-300

## System Performance Analyzer

M68HDS300SPA                   System Performance Analyzer Module for 32-Bit Emulation

## Memory Expansion

M68HDS3EMM1                   64K Byte Emulator Memory Expansion for HDS-300; M68000,008,010,HC11, 6801,03  
M68HDS3EMM2                   128K Byte Emulator Memory Expansion for HDS-300; M68000,008,010  
M68HDS3EMM3                   256K Byte Emulator Memory Expansion for HDS-300; M68000,008,010  
M68HDS3FDKT                   HDS-300 Second Floppy Drive Kit  
M68020MEM2                    MC68020 Emulator Expansion to 256K Bytes for HDS-300  
M68020MEM3                    MC68020 Emulator Expansion to 1M Bytes for HDS-300



# Development Systems Part Number Descriptions (Continued)

## Cables/Hardware

M68HC05CDIPT	MC68HC05C4,8 DIP Cable Probe for HDS-300
M68HC05CPCCT	MC68HC05C4,8 PLCC Cable Probe for HDS-300
M68HC11ADIPT	MC68HC11A DIP Cable Probe for HDS-300
M68HC11APCCT	MC68HC11A PLCC Cable Probe for HDS-300
M68HDS3ADPTR	HDS-200 M68HC05C4 Module to HDS-300 Adapter Board with Software
M68000/10DIPT	MC68000,010 DIP Cable Probe for HDS-300
M68000/10PCCT	MC68000,010 PLCC Cable Probe for HDS-300
M68000/10PGAT	MC68000,010 PGA Cable Probe for HDS-300
M68008DIPT	MC68008 DIP Cable Probe for HDS-300
M68008PCCT	MC68008 PLCC Cable Probe for HDS-300

## Cross Software

M68BEQSCC11	M68HC11 Source for C Compiler
M68BNQBCC20C	MC68020 Cross C Compiler on Mag Tape Media, 1-16 Users Licensed
M68BNQBCC20D	MC68020 Cross C Compiler on Mag Tape Media, 1-32 Users Licensed
M68BNQBCC20E	MC68020 Cross C Compiler on Mag Tape Media, 1-64 Users Licensed
M68BNQBCC20F	MC68020 Cross C Compiler on Mag Tape Media, >64 Users Licensed
M68BNQSCC20-2	MC68020 Cross C Compiler Source on Mag Tape Media
M68BNQSOPT	Hi-Level C Optimizer Source on 9-Track Tape
M68KTUTOR-D4	Tutor Source Listing, Rev 1.3
M68KTUTORS	Tutor Source Code for MEX68KECB on VERSAdos 8" Diskette
M68N2QSASM	MC68020 Assembler for System V/68 Source Code on Mag Tape Media
M68N2XBASM	MC68020 Assembler for System V/68 Object Code on 5.25 Floppy Media
M68N2XBCC	M68000,008,010 C Compiler Assembler Object for SYS1131DVLP System V/68, 1-8 Users
M68N2XSASM	MC68020 Assembler for System V/68 Source Code on 5.25 Floppy Media
M68NCXBRASM	M6800,01,04,05,09 Cross Assembler/Linker for V/68 on SYS1131DVLP
M68NEXBCC11A	M68HC11 C Compiler/Assembler/Linker for SYS1131DVLP for 1-2 Users
M68NEXBCC11B	M68HC11 C Compiler/Assembler/Linker for SYS1131DVLP for 1-8 Users
M68NEXBCC11C	M68HC11 C Compiler/Assembler/Linker for SYS1131DVLP for 1-16 Users
M68NNXBCC20A	MC68020 Cross C Compiler Object on 5.25 Floppy Media, 1-2 Users
M68NNXBCC20B	MC68020 Cross C Compiler Object on 5.25 Floppy Media, 1-8 Users
M68NNXBCC20C	MC68020 Cross C Compiler Object on 5.25 Floppy Media, 1-16 Users
M68NNXBPAFMLK	PAL Port Assembler/Linker Object on 5.25 Floppy Media
M68NNXBTLKT	VERSA dos Tool Kit, System V/68, Object Code, 5.25 Floppy Media
M68NNXSICC20-2	MC68020 Cross C Compiler Source on 5.25 Floppy Media
M68NNXSPASMLK	PAL Port Assembler/Linker Source on 5.25 Floppy Media
M68NNXSTLKT	VERSA dos Tool Kit, System V/68, Source Code, 5.25 Floppy Media
M68W2XBH300D	MC68020 Release 1.1 Update and System Performance Analyzer Update for HDS-300
M68WEXBH300	M68HC11 Release 2.0 Update for HDS-300

## MPU Software Support

MC68KTBA	Token Bus Frame Analyzer (EPROMs for MVME372 Board)
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## Evaluation Modules

MEX68KECB	MC68000 Educational Computer Board
M1468705EVM	M146805E2,F2,G2 Evaluation Module
M68HC04EVM	M6804J1,J2,P2, and M68HC04P3 Family Evaluation Module
M68HC05EVM	M68HC05 Family Evaluation Module
M68HC11EVB	MC68HC11 Family Evaluation Board
M68HC11EVM	MC68HC11 Family Evaluation Module
M68701EVM	MC68701,6801,6801U4,6803,6803U4 Family Evaluation Module
M68705EVM	MC68705,6805P,R,U Family Evaluation Module
M68HC99EVM	MC68HC99,98 Hard Disk Controller Family Evaluation Module

## Digital Signal Processor Development Software

DSP320to56001	32010 to DSP56000,1 Translator Software
DSP56000CLASA	DSP56000 Assembler/Simulator Software for IBM PC (PC and MS-DOS)
DSP56000CLASC	DSP56000 Assembler/Simulator Software for SUN III (UNIX, BSD 4.2)
DSP56000CLASD	DSP56000 Assembler/Simulator Software for VAX (VMS, VER. 4.2)
DSP56000CLASE	DSP56000 Assembler/Simulator Software for VAX (UNIX, BSD 4.2)



**UniLab™ 8000 Series analyzer-emulators share common features. All include Orion's 48 Channel Bus-State Analyzer, In-Place Emulator, built-in Stimulus Generator and EPROM Programmer and provide for the optional Program Performance Analyzer™. There are also notable differences. The newer 8620 utilizes a proprietary high-speed parallel bus and 2730 bus-cycle trace buffer to provide InSight™ — continuous monitoring of register contents, I/O lines, ports and user-defined memory windows. The 8620 includes a crystal-controlled, one microsecond timer for more precise event measurements. The UniLab 8420 makes use of a standard RS232C serial interface.**

## SOFTWARE FEATURES

- Menu or command driven with single context for all instruments.
- Line-by-line assembler.
- High level language support.
- Supports common cross-assembler symbols loader for Intel OMF files, Motorola S records and Tektronix HEX.
- Extensible macro capability.
- Cursor key or command control.
- Pop-up mode switch panel.
- Split screen displays, user definable.
- On-line glossary.
- Menu-driven shell displays equivalent commands.
- Log session to DOS text file.
- View text files in separate window.
- Save screen display to DOS text file.
- 40 user-definable soft function keys.
- Bonus features: Calculator, ASCII table, IC pinout library, memo message feature, direct DOS access, EGA/ECD support (or use monochrome display).

## BUS-STATE ANALYZER

- 48-bit wide Trace Display and Memory.
- Extensive filtering capabilities in both 8620 and 8420.  
For 8420: 170 bus-cycle trace buffer.  
For 8620: 2730 bus-cycle trace buffer.
- 48 data inputs. Two groups of 8 can be separately clocked.
- 4 clock signal inputs. Gated to form one bus clock: 297 ns minimum bus cycle.  
Clock edge filter prevents re-trigger before 100 ns.
- 1 microsecond crystal-controlled timer.
- Address demultiplexing latches included — also used by emulator.

## ANALYZER TRIGGER

- 4 step sequential trigger.
- RAM truth tables allow search for any function of 8-bits at each 8-bit group, for each step.
- 8 truth tables per step x 4 steps = 32 @ 256-bit tables.
- 16-bit inside/outside range detection on address lines.
- 4-bit segment enable gives 20-bit address capability.
- Pass counter: wait up to 65,382 events or cycles before 4th step.
- Before/After Pass Count trigger enable.
- Delay counter: wait up to 65,382 events or cycles to stop trace.
- Filter feature: records only cycles which satisfy trigger.
- Oscilloscope sync output. (Sync on trigger.)
- Interrupt output: interrupt target on trigger (if enabled).
- LED indicates searching for trigger. Stand-alone operation while waiting.

## IN-PLACE EMULATOR

- Download time for UniLab 8420: 57 seconds for 64K binary file from AT hard disk.  
For 8620: 5 seconds for 64K binary files from AT hard disk at 19200 baud.
- 150 ns maximum access time ROM emulation memory.
- 32K x 8-bit or 16K x 16-bit standard, 128K bytes optional.
- Individual 2K segments can be selected in any combination within 128K range.
- 20-bit enable address decoding.
- Stand-alone operation possible as a ROM emulator.
- 16-bit idle register loops target CPU allowing loading of emulation RAM and resumption of program execution.
- Optional, target processor-specific software gives full debug capability including register and target memory display and change, breakpoints, and single step, next step, and for the 8620 only a real time display.
- Program loading software: from hex or binary disk files, hex serial download, memory image, ROM read.

## EPROM/EEPROM PROGRAMMER

- Smart programming algorithm for high speed.
- 28-pin zero insertion force socket handles 24 and 28 pin devices.
- Programs most popular industry standard devices including 2716, TMS2516, 2532, 2732A, 2764/128, 27256/64A/128A. (Also CMOS versions.)
- Optional programming module available for 27512, 2716B, 2732B.

## SIGNAL OUTPUTS

- TTL logic levels (74LS244 outputs).
- 100 ohms forward terminating resistors on Emulator data lines.
- Reset output: open collector, 7406 thru 47 ohms.
- Interrupt output: open collector, 7406 low true.
- 9 Stimulus outputs (8255 NMOS outputs).

## SIGNAL INPUTS

- TTL logic levels. (74ALS inputs.)
- 0.1 ma maximum loading includes emulator and analyzer.

## COMPUTER REQUIREMENTS

- IBM-compatible PC, XT, AT, PS/2, MS-DOS 2.0 or above, 320K RAM, RS232C port for the 8420, dual floppy drives, or Winchester drive. For the 8620, one short slot is needed for Orion parallel bus adaptor card.
- Monochrome and EGA compatible.

## PHYSICAL DATA

- Size: 2.1 in. high x 13 in. wide x 7.8 in. deep. (53 x 330 x 198 mm. H x W x D.)
- Weight: 4 lbs. (1.8 Kg.)

## POWER

- 100 KHz switching supply built in. 110v  $\pm$  10% 50/60 Hz input. 15 Watts (standard), or 220v  $\pm$  10% 50/60 Hz input: 15 Watts (optional).

## ACCESSORY OPTIONS

- Personality Paks for more than 150 microprocessors.

## PROGRAM PERFORMANCE ANALYZER (OPTIONAL)

- Analysis range from a single byte to entire program.
- Data gathered as target processor runs at full speed.
- Address Domain mode determines activity level in any specified address ranges.
- Time Domain mode determines run time range(s) of any range of code with  $\pm$  20 microsecond accuracy. Automatic mean run time display.
- Multi Pass mode allows up to 15 code ranges.
- Graphical and tabular results displays.
- Symbolic labels with automatic conversion to address ranges.
- Manual or automatic range definition.
- Symbol table save and recall.
- Template save and recall feature. Data save and recall.
- Full 80 character title/date line.
- Seamless integration with other UniLab functions to trace code, examine registers and memory, alter code with the line-by-line assembler. Extensible filters trigger only on qualifying data.

Call Toll Free: 800/245-8500 In California: 415/361-8883

**ORION**  
INSTRUMENTS

**Orion Instruments, Inc.**

702 Marshall Street, Redwood City, CA 94063 U.S.A.

TELEX: 530942 FAX: 415/361-8970

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# **INTRODUCTION TO MICROCOMPUTER BOARDS**

In this section single- and multiple-board microcomputers are arranged in alphanumeric sequence by data word size, bus type, and within that grouping, according to the microprocessor on which they are based.

Microcomputer support boards are listed after the CPU boards. Support boards are grouped according to the supported system or bus, primary function, and then alphabetically by manufacturer.

MICROCOMPUTER BOARDS

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
	8-32	Z80A	4	S-100	8	2		38.4	64	96		x
8	8-24	R6511Q	2		5	1	32	19.2	64	0.1/32	0/32	
8	8	Z-80A	4		5, ± 12	2	2	38.4	64	64	2/4	x
8	8	Z-80A	4		5, ± 12	4	2	38.4	64	64	2/4	x
8	8	Z-80B	6		5, ± 12	2	2	38.4	64	64	2/4	x
8	8	Z-80B	6		5, ± 12	4	2	38.4	64	64	2/4	x
8	8	Z-80B	6		5, ± 12	2	1	38.4	64	64	2/64	x
8	8	Z-80B	6		5, ± 12	2	1	38.4	64	128	2/64	x
8	8	Z-80B	6		5, ± 12	2	1	38.4	64	256	2/64	x
8	8	Z8	7.37		5	1	39	19.2	120	2/8	0/8	
8	8-32	Z80	4		5		40		64	1/2	0/8	
8	8	Z80	4/6		100, 120, 220 VAC	4	16	38.4	64	56	8	
8	8	Z80	4/8		5, ± 12	1	40	64	64	32	0/32	
8	8	80C31	12		5	2	32	38.4	64	8/32	0/32	
8	8	6303	1.23		7-15	1	16	9.6	64	32/512	32	
8	16	8088	4		5	1	23	4.8	32	4/8	8/16	
8	8	6303	1	—	6-10	1	14	9.6	64	256	32	
8	8	6303	1.23		6-10	1	14	9.6	64K	96	32	
8	8	64180	6		5, ± 12	6	2	38.4	512	256/512	8/64	x
8	8/24	65C02	2/4		5	1	6	19.2	64	8/48	8/20	
8	8-24	6511	2		± 12	1	30	19.2	64	2/32	0/32	
8	8-24	6511	2		5	1	24-29	19.2	64	2/32	0/32	
8	8	6809	1.7		5, ± 12	1	76	19.2	100	28	72	
8	8	8052	11.06		5	2	37	19.2	128	8/16	0/8	
8	8-24	8085A	2		5	1	22		64	0.256/0	0/4	
8	8-24	8085A-2	4.84		5, ± 12	1	48	38.4	64	4/32	0/60	
8	16	8088	4	—	5	1	23	4.8	32	4/8	8/16	
8	16	8088	4	—	5	1	23	4.8	32	8/32	8/16	
8	16	8088	5	-1	cons. fac.	4	48	38.4	1024			x
8	16	6502	1	AIM-65	5	0	72		64	1/4	0/20	
8	8	8044	12	BITBUS	5, ± 12	1		2.4	64	2	0/64	
8	8	8044	12	BitBus	5	1	24		128	2/32	16/64	
8	8	8044	12	BITBUS	5	1	24	2400	64	2		
8	8	8044	12	BITBUS/PC	5	1		2.4	64	2/64	0/64	
8	8	8044	12	BITBUS/SBX	5	1		2400	64	2		
8	8-24	6800	1	Bus-44	5, ± 12	1	32	9.6	64	0.5	0/4	

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.

μC BOARDS



Software Support						Hardware Support	Comments	Model	Source	Line
Assembler	Debug/Monitor	Editor	High Level Language	Operating System						
				x	x		Uses M-60 Multiprocessing expansion bus.	DPC183	ACE	5
x	x	x		x	x		Expandable, IEEE-488 capability, timer, memory-mapped I/O, with most microcomputers, can be used as a development system with in-circuit emulation.	SBC6511	ConnMicro	
x	x	x	x	x	x		8", 5 1/2" and 3 1/2" floppy controller	DSB4042	Davidge	
x	x	x	x	x	x		8", 5 1/2" and 3 1/2" floppy controller	DSB4044	Davidge	
x	x	x	x	x	x		8", 5 1/2" and 3 1/2" floppy controller	DSB4062	Davidge	
x	x	x	x	x	x		8", 5 1/2" and 3 1/2" floppy controller	DSB4064	Davidge	
x	x	x	x	x	x		50 pin expansion, 8", 5 1/2" and 3 1/2" floppy controller	DSB6064	Davidge	
x	x	x	x	x	x		50 pin expansion, 8", 5 1/2" and 3 1/2" floppy controller	DSB6128	Davidge	
x	x	x	x	x	x		50 pin expansion, 8", 5 1/2" and 3 1/2" floppy controller	DSB6256	Davidge	
	x	x	x		x		Similar to MC-1N, extra RAM, EPROM, and I/O, control basic (2K).	MC-1Z	Basicon	10
x	x	x	x	x	x		Three 8-bit output ports, two 8-bit input ports.	MD-SBC1	Thomson	
			x				On-board power supply, accepts any combination of RAM, EPROM or EEPROM	DSB3200	Davidge	
					x		Cassette interface, battery-packed clock-calendar chip, dip switches, low-cost controller board.	SBS80	SingleBoard	15
x	x	x	x		x			MC21	Basicon	
x			x				Data logger, 10-bit A/D, 50 $\mu$ A dormant mode	Tattletale IV	Onset	
	x	x	x	x	x		Industrial development and control system with on board EPROM programmer, BASIC and FORTH in firmware.	ipc-SBC88	Vesta	
							Complete datalogger with A to D and Basic operating system	TATTLETALE II	Onset	
x			x				Complete data logger. 8 channel 8-bit A/D converter, 200 $\mu$ A dormant mode, BASIC	Tattletale III	Onset	20
x	x	x	x	x	x		Eight-inch and 5 1/4-inch floppy disk controller, SCSI	DSB8016	Davidge	
x	x	x	x	x	x		Includes 12 bit A/D, instrumentation, amp and 16-channel multiplexer.	IDAM	Golden	
x	x	x		x	x		RS-232 with CmCnet. Expandable, with most microcomputers, can be used as a development system with in-circuit emulation.	SBC6511-KA	ConnMicro	
x	x	x		x	x		IEEE-488 interface. Exandable. Can be used as a controller. With most microcomputers, can be used as a development system with in-circuit emulation.	SBC6511-KB	ConnMicro	
x			x	x			A single board system with 86x25 display, keyboard, floppy printer.	DT6000	AppBusComp	25
	x	x	x		x		Similar to MC-1Z except with a full 8K basic.	MC-11	Basicon	
							Four-level vectored interrupt, Multimaster control, programmable 14-bit binary timer, optional RS232C port.	mSBC80/04	MicroInds	
	x				x		Stand-alone single-board computer with prototyping area, SBC 80/24 compatible, 2iSBX connectors, CMOS RAM with battery backup.	Multiboard-85	MicroDesigns	
	x	x	x	x	x		Industrial development and control system with on board EPROM programmer, BASIC and FORTH in firmware.	ipc-SBC88-1	Vesta	
	x	x	x	x	x		Industrial development and control system with on board EPROM programmer, BASIC and FORTH in firmware.	ipc-SBC88-2	Vesta	30
	x						Four 8-bit wide SBX connectors, on-board 8087 socket	DP8800	Comark	
x	x	x	x	x	x		Software compatible with AIM-65.	6500	Cubit	
x	x	x	x	x	x		16 channel 12 bit A/D converter, 2 12-bit D/A outputs, software programmable gain set; built-in real-time, multitasking executive.	iRCB44/20A	Intel	
x	x		x	x			BitBus I/O remote controller board	iRCB 44/20	Intel	
x	x		x	x	x		Digital remote controller board, BITBUS interface plus 24 lines digital I/O, SBX connector for expansion, distributed control applications.	iRCB44/10A	Intel	35
x	x	x	x	x	x		Interfaces PC Bus to BITBUS.	iPCX344A	Intel	
x	x		x	x	x		Intelligent multimodule board, interface from SBX-bus to BITBUS with room for user programs to offload the host CPU.	iSBX344A	Intel	
x	x	x	x	x	x		Serial port is programmable to 9600 baud.	MCL45	Wintek (4913)	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8-24	6800	1	Bus-44	5	1	32	9.6	64	0.5	0/4	x
8	8-40	6809	1	Bus-44	5, $\pm 12$	2	32	9.6	64	2/32	0/64	
8	8-40	6809	1	Bus-44	5, $\pm 12$	2	32	9.6	64	6	0/32	
8	8-40	6809	1	Bus-44	5, $\pm 12$	2	32	9.6	64	24	0/32	
8	8-24	6800	1	Bux-44	5, $\pm 12$				64	128		
8	8-32	NSC800	3	C-44	6.5-18		22	9.6	64	0.178	6	
8	8	6805E2	1	C-44	6.5-18		8	9.6	8	1.19	2/6	
8	8	80C85	3	C-44	6.5-18		24		64	8/24	8/24	
8	8	80C88	1	C-44	6.5-18	1	22	38.4	512	25	8	
8	8-24	6801		DIN	5/12	1	12	9.6	640	12	8	
8	16	MC68008	8/10	EXORbus	5, $\pm 12$	6		38.4	1000	8/56	16/112	—
8	8	Z80	4/6	EXORbus	5, $\pm 12$	1	8	19.2	64	4	8/32	
8	8-24	6809	1.5/2	EXORbus	5, $\pm 12$	2	20		64	0/10	0/20	
8	8	6502	1/2	EXORbus	5, $\pm 12$	2	76	19.2	64	0/56	0/64	x
8	8	6502	1/2	EXORbus	5, $\pm 12$	1	76	19.2	32	8	24	x
8	8	6502	1/2	EXORbus	5, $\pm 12$	1	8	19.2	64	4	8/32	
8	8-24	6800	1	EXORbus	5, $\pm 12$	1	60		64	1	0/4	x
8	8-24	6800	1	EXORbus	5, $\pm 12$	1	32	9.6	64	1	0/8	x
8	8-24	6800	1	EXORbus	5, $\pm 12$	1	8		64	0/10	0/10	x
8	16	68008	8/12	EXORbus	5, $\pm 12$	2	40	19.2	1MB	64	64	x
8	8-24	6802	1	EXORbus	5, $\pm 12$	0	26		64	128	0/4	
8	8-24	6802	1	EXORbus	5, $\pm 12$	1	26	9.6	64	128	0/4	x
8	8	6802	1/2	EXORbus	5, $\pm 12$	1	8	19.2	64	4	8/32	
8	8-24	6809	1	EXORbus		2	20		64	0/10	0/20	
8	8-24	6809	1	EXORbus		1	20		64	2	2/14	
8	16	6809	1/2	EXORbus	5, $\pm 12$	2	40	38.4	1048	2/8	2/32	
8	8-32	6809	2	EXORbus	5	2			1000		8	x
8	8-24	6809	2	EXORbus	5, $\pm 12$	1	20	28.8	64	2	2/14	x
8	8	6809	4/8	EXORbus	5, $\pm 12$	1	8	19.2	64	4	8/32	
8	16	6802	0.5/1	EXORciser	5, $\pm 12$	2	40	38.4	56	1.2	6	x
8	16	6809	1	EXORciser	5, $\pm 12$	2	40	38.4	64	1	6	
8	8	64180	6.288	G-96	5, $\pm 12$	1	16	1.0	512	0/459	0/64	x
8	16	CP80C88	4.77	IBM PC	5	4	2			640	64	x
8	8	HD64180	6	IBM PC		2		38.4	128	128		x
8	N/A	N/A		IBM PC	5	0			256	256		
8	16	V40	7.16	IBM PC	5	2		115.2	1MB	768	32/128	x
8	8-12	6301	24	IBM PC	5	0	0					x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support					Hardware Support	Comments	Model	Source	Line
Assembler	Debug/Monitor	Editor	High Level Language	Operating System					
x	x	x	x	x	x	Serial port is programmable to 9600 baud. Single 5V supply.	MCV45	Wintek	5
x	x		x		x	On-board real-time clock interrupt, power-on reset and watchdog timer circuit.	<b>MCH18</b>	<b>Wintek (4913)</b>	
x	x		x		x	Watchdog timer, real-time clock	MCH38	Wintek	
x	x		x		x	Watchdog timer, real-time clock	<b>MCH68</b>	<b>Wintek (4913)</b>	
x	x	x	x		x	Socket for EPROM, 1 K to 4 Kbytes	<b>MCL10</b>	<b>Wintek (4913)</b>	
						Two 16-bit timers, real-time clock, switching voltage regulator, 5 interrupts.	CPU801	Onset	10
	x				x	Eight analog input lines, real-time clock, voltage regulator, 27C16 EPROM, 256-bit EEPROM	CPU6805A	Onset	
	x						CPU8085A	Onset	
	x					100NA low power mode	CPU8088	Onset	
			x	x		Single-board FORTH microcomputer.	TDS900	Stynetic	
x	x	x	x	x	x	PAL, Generated memory map using 8K and 16K static RAMS and 8K through 64K EPROMS.	9641	CreMicro	15
x	x	x	x	x	x	Interchangeable 6502/6802/6809/Z80 CPUs. GPIB, ACIA, printer ports, VUA, VXA, VMA and bootstrapping.	GMS6527	GenMicro	
						Motorola Micromodule MM17 Compatible CPU card	MIKUL 6809-6	TLIndustries	
x	x	x	x	x	x	Basic, assembler, forth, PL65, real clock, CMOS battery for all RAM.	ASBC-65-64	AppBusComp	
x	x	x	x	x	x	Basic, assembler, forth, PL65, CMOS battery for RAM.	ASBC-65-8	AppBusComp	
x	x	x	x	x	x	Interchangeable 6502/6802/6809/Z80 CPUs. GPIB, ACIA, printer ports, VUA, VXA, VMA and bootstrapping.	GMS6506	GenMicro	20
x	x	x	x	x	x	Crystal-controlled clock, interrupt, DMA, power-on reset, buffered bus, 3 PIAs.	M68MM01	Motorola	
x	x	x	x	x	x	Crystal-controlled clock, interrupt, DMA, power-on reset, buffered bus, 2 PIAs.	M68MM01A2	Motorola	
x	x	x	x	x	x	Three 16-bit timers, parallel printer I/O interface, buffered bus, 5 sockets for 2K EPROM, ROM or RAM.	M68MM01D	Motorola	
x	x	x	x	x	x	Forty I/O lines, 20 buffered. Can also use 8-bit 6502, 6802, 6809, and Z80 CPUs. GPIB Talker/Listener/Controller port.	GMS6507	GenMicro	
x	x	x	x	x	x	Three 16-bit timers, programmable baud rate.	M68MM01B	Motorola	25
x	x	x	x	x	x	Audio cassette interface, dynamic RAM refresh, buffered bus, 3 16-bit timers.	M68MM01B1A	Motorola	
x	x	x	x	x	x	Interchangeable 6502/6802/6809/Z80 CPUs. GPIB, ACIA, printer ports, VUA, VXA, VMA and bootstrapping.	GMS6525	GenMicro	
x	x	x	x	x	x	Can use RAM in ROM sockets.	M68MM17	Motorola	
x	x	x	x	x	x	Three 16-bit timers, DMA buffered bus.	M68MM19	Motorola	
	x			x	x	Resident monitor. Has 2 kbytes of nonvolatile RAM with space for RAM or ROM expansion.	9619A	CreMicro	30
x	x	x	x	x	x	Designed for use with OS-9 operating system. Real time interrupt PTM on-board.	9639	CreMicro	
x	x	x	x	x	x	Three 16-bit timers, DMA buffered bus.	M68MM19A	Motorola	
x	x	x	x	x	x	Interchangeable 6502/6802/6809/Z80 CPUs. GPIB, ACIA, printer ports, VUA, VXA, VMA and bootstrapping.	GMS6526	GenMicro	
	x				x	ACIA, PIA, bit-rate generator, interrupt vector generator, power-failure protect restart triple programmable timers.	9600A	CreMicro	
	x				x	ACIA, PIA, bit-rate generator, interrupt vector generator, power failure protect restart, hardware compatible with CMS 9600A.	9609	CreMicro	35
x	x	x	x	x	x	Low power, sockets for 16-channel 12-bit A/D converter	7510	Sensoray	
x	x	x	x	x	x	An IBM PC/XT Syatem for Integrating Functionality into Larger Systems.	QPC5101	Qualogy	
x	x			x	x		CPS-QPC	InterconMicro	
						Used for evaluation of TMS34061, TMS34070, and TMS4161	TMDS3471804000 TI		
x	x	x	x	x	x	On-board floppy controller and video option.	LittleBoard/PC Ampro		
x	x		x	x		Digital imaging system for the IBM PC, XT, AT and compatibles.	IDETIX	MicronTech	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

Data Word Size (bits)	Instruction Word Size (bits)	General				I/O			Memory			
		CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8	8044	12	IBM PC/BITBUS	5	1		2.4	64	2	0/64	
8	8-48	8088	5	IBMPc	5, $\pm 12$	2				256	64	x
8	8-48	8088	5	IBMPc	5, $\pm 12$	1				128	32	x
8	24	Z80A	4	IIOC	5, $\pm 12$	1	24	9.6	64	2	8	
8	24	Z80A	4	IIOC	5	1	8	19.2	64	4		
8	24	6802	4	IIOC	5, $\pm 12$	2	16	38.4	1MB	32	48	x
8	48	6809	1/2	IIOC	5				64	4	16	x
8	48	6809	1/2	IIOC	5	2	16	76.8	1MB	16	64	x
8	24	8085A	6.144	IIOC	5	1	46	1.2	64	2	10	x
8	8	8052	11.0592	iSBX	5, $\pm 12$	2	40	19.2K	128	8/64	8/64	x
8	8	NSC800	2	Multibus	5	2	22	9.6	64	1/10	4/16	
8	8-24	NSC800	2.5	Multibus	5, $\pm 12$	1	48	19.6	64	8/56	56	
8	8	Z80	2/4	Multibus	5, $\pm 12$	2	56	9.6	64	4	8/16	x
8	8-32	Z80	2/4	Multibus	5, $\pm 12$	2	32	19.2	64	64	64	x
8	8-32	Z80	2/4	Multibus					64			
8	8-24	Z80	4	Multibus	5	2	16	19,200	16	32	16	x
8	8-32	Z80A	2/4	Multibus	5, $\pm 12$	2	8	19.2	64	64/1MB	0/32	x
8	8-32	Z80A	2/4	Multibus	5, $\pm 12$	4	8	19.2	64	64/1MB	0/32	x
8	8-32	Z80A	2/4	Multibus	5, $\pm 12$	2	0	19.2	64	128/16MB	0/64	x
8	8-32	Z80A	2/4	Multibus	5, $\pm 12$	1	48	19.2	64	16/64	0/40	
8	8-32	Z80A	4	Multibus	5, $\pm 12$	4	2	19.2	64	256	0/32	
8	8-32	Z80A	4	Multibus	5, $\pm 12$	2	16	9.6	64	64/128	2/32	x
8	8-32	Z80A	4	Multibus	5, $\pm 12$	2	24	19.2	64	64	0/128	
8	16	Z80A	4	Multibus	5	1	48	9.6	64	8/8	0/16	x
8		Z80A	4	Multibus	5	1	48	9.6	64	32/32	0/32	x
8	8	Z80A	4	Multibus	5	1	48	9.6	64	64/64	0/32	
8		Z80A	4	Multibus	5	3	24	9.6	64	64/64	0/32	x
8	8	Z80A	6	Multibus		2	16		16K	32	16	
8	8-24	Z80B	6	Multibus	5	1	48	19.2	64	128/128	0/32	
8	8-24	Z80B	6	Multibus	5	3	24	19.2	64	128/128	0/32	
8	8-24	8080A	2.2	MULTIBUS	5	1	48	38.4	1 MB	4/4	0/8	
8	8-24	6809	1/2	Multibus	5	2	48	19.2	64	9	8	x
8	8-32	80C88	5/8	Multibus	5	1	24	19.6	1 Mb	16/64	256	
8	8-48	80188	6	Multibus	5	8			1MB	64		x
8	8-24	8080A	2	Multibus	5	1	48	38.4	64	1/4	0/16	x
8	16	8080A	2.05	Multibus	5, $\pm 12$	2	48	38.4	64	1/4	0/16	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support					Hardware Support	Comments	Model	Source	Line
Assembler	Debug/Monitor	Editor	High Level Language	Operating System					
x	x	x	x	x	x	Enables an IBM PC to host a BITBUS network.	PCX344A	Intel	5
			x	x	x	Three timer channels, 8 levels of interrupts, supports MS-DOS, CP/M86 and concurrent CP/M.	FE6400	Faraday	
			x	x	x	On-board floppy disk controller and monochrome display controller, supports MS-DOS, CP/M86 and CP/M.	FE6410	Faraday	
						Automatic and manual restart logic	MPMZ80A	PEP-Modular	
						Z80A CPU Module with DMA Controller	MPMZ80D	PEP-Modular	
x	x			x		Automatic and manual restart logic, battery backup available.	MPM6	PEP-Modular	10
				x		CPU module with DMA controller.	MPM10	PEP-Modular	
x	x			x		Data retention with external battery backup module.	MPM11	PEP-Modular	
x	x			x		2000 hour standby operation, automatic and manual restart logic	MPM8085A	PEP-Modular	
x	x	x	x			On-board BASIC, PROM Programmer, Prototyping area, expansion bus.	SIBEC-II	BinaryTech	
					x	Micro power operation, Z80 instruction set, Breadboard area.	DR800	Dexter	15
					x	CMOS, Z80 compatible, battery backed-up RAM	CBC80C/24	DiversTech	
x	x		x		x	Eight vectored interrupts, four programmable timers, resident diagnostics, memory and I/O modules available.	S80CPU	Babcock	
x	x	x	x	x	x	Floppy controller, streaming tape interface, hard-disk interface, DMA, IEEE-488 controller.	MLZ90	Heurikon	
x	x	x	x	x	x	Replaces 8080 CPU board in Intellec 800, 888. Supports all Z80 software and architectural features. ISIS-11 compatible.	Z80SAM	RELMS	
x	x		x	x	x	Intended as supervisor for Multibus system.	RSBC-Z80/32	RELMS	20
x	x	x		x	x	Floppy controller, streaming-tape interface, hard-disk interface.	MLZ91A	Heurikon	
x	x	x		x	x	Floppy controller, streaming-tape interface, hard-disk interface, DMA, Multimaster capability.	MLZ92A	Heurikon	
x	x	x	x	x	x	DMA, modem and SDLC/HDLC signals.	MLZ93	Heurikon	
x	x	x	x	x	x	High-speed math processor, 16-level interrupt controller, 6 counter/timers, Multimaster bus arbitration logic, accepts floating-point processors.	ZBC80	Matrox	
			x	x	x	On-card video graphics controller	MLZVDC	Heurikon	25
x	x	x	x	x	x	Floppy disk controller hard disk interface Multimaster capability, math processor interrupt controller, 3 counter/timers.	SBC90A	InnovRes	
	x					Programmable baud rate generator, two on-board iSBX expansion sockets, on-board memory and I/O management.	PBC80	Matrox	
x						High-memory industrial controller or low-end computer board.	MSC8001	MonSys	
x						Multimaster logic, PROM memory maps, math chip for floating-point processing.	MSC8004	MonSys	
						Optional on-board arithmetic processing unit	MSC8004A	MonSys	30
x						Multimaster logic and optional APU, single/dual address maps available with custom RAM/ROM and I/O mapping.	MSC8007/A	MonSys	
x	x		x	x	x	Intended as supervisor for multiprocessor system. Communications options.	RSBC-Z80SP	RELMS	
						Optional on-board APU, individual board reset	MSC8014	MonSys	
						Optional on-board APU, individual board reset	MSC8017	MonSys	
x	x	x	x	x	x	8-level interrupt controller, 3 programmable timers.	iSBC80/20-4	Intel	35
x	x	x	x			Programs 2716, 38E70. Emulates 3870 family, cross-assembler for 8080- and 6800-based systems. On-board keyboard and display.	F68PEP	Fairchild	
						CMOS replacement for iSBX 88/25, 0-70°C and -40 to 70°C versions available, on-board battery-backed RAM	CBC88C/25	DiversTech	
x	x	x	x	x	x	Nine DMA channels, 64 Kbytes DRAM expandable to 192 Kbytes, 2 iSBX expansion connectors, RS232C on 6 channels.	iSBC188/48	Intel	
x	x	x	x	x	x	Sockets for interchangeable line drivers and terminators, programmable communications interface, single-level interrupt.	iSBC80/10B	Intel	
x	x	x	x	x	x	48 individually programmable parallel I/O lines. Available built to MIL883 Standard.	DCS8010A	DistComp	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

Data Word Size (bits)	Instruction Word Size (bits)	General				I/O			Memory			
		CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8-24	8080A	2.05	Multibus	5, $\pm 12$	1	48		64	1	0/8	
8	8-24	8080A-2	2.4/4.8	Multibus	$\pm 5, \pm 12$	1	48	38.4	64	8/8	0/32	
8	8-24	8085	2	Multibus	5	1	22		64	0.512/0	2/4	x
8	8-24	8085	2	Multibus	5	1	22		64	0.512/0	2/4	x
8	8-24	8085	2	Multibus	5	1	22		64	0.256/0	4	x
8	8-24	8085	5	Multibus	5, $\pm 12$	2	42	9.6	64	16/64	0/8	
8	16	8085	5	Multibus	5, $\pm 12$	1	48	38.4	64	6/6	0/16	
8	8-24	8085A	2.45	Multibus		1	—		64	16	0/16	
8	16	8085A	2.5/5	Multibus	5, $\pm 12$	1	48		64	4	0/12	
8	8-24	8085A	2.76	Multibus	5, $\pm 12$	4	10	56	64	16	0/8	x
8	8-24	8085A	2.76	Multibus		1	42		64	16	0/8	
8	8-24	8085A	2.76	Multibus		4	10		64		0/8	
8	8-24	8085A	3.07	Multibus	5	1	48	1	64	2	0/16	x
8	16	8085A-2	2/5	Multibus	5	1	22	9.6	64	0.5/9	0/32	x
8	8-32	8086	5	Multibus	5, $\pm 12$	Varies	Varies	819				x
8	8-32	8086	5	Multibus	5, $\pm 12$	8	0	819	1Mb	17/0		x
8	8-32	8088	4.2/5	Multibus	$\pm 5, \pm 12$	1	24	38.4	1000	4/16	0/32	x
8	8-32	8088	4.8	Multibus	5, $\pm 12$		24		1Mb	4/4	0/64	
8	8-32	8088	4.8	Multibus	5, $\pm 12$	-	24		64	8	64	x
8	8-32	8088	4.8/6.67	Multibus	$\pm 5, \pm 12$	0	24	38.4	1000	4/8	0/128	x
8	8-32	8088	5	Multibus	5, $\pm 12$	1	24	9.6	64	4	0/64	
8	16	8088	5	Multibus	5, $\pm 12$	varies	varies	1000	1Mb	4x28		x
8	16	8088	5	Multibus	5, $\pm 12$	8	0	1000	1Mb	17/0		x
8	20	8088	5	Multibus	5, $\pm 12$	4	0	9.6	1000	8	0/16	x
8	8,16,24	8080A-1	2	Multibus I	5, $\pm 12$	1	48	19.2	64			
8	8,16	8085	2.76	Multibus I	5	5	10	Prog.		16/64	16	
8	8,16	8085	2.76	Multibus I	5	1		Prog.	64	16	16	x
8	8,16	8088	5/8	Multibus I	5	1	24	Prog.	1 MB			x
8	8,16	8088	5/8	Multibus I	5	1	24	Prog.	1 MB			x
8	8	Z80B	6	None	5, $\pm 12$	2	98	76.8	64	0/64	0/64	
8	16	8088	4.77	PC bus	5	0	0		1	256	32	x
8	16	8088	4.77	PC bus	5	0	0		1	256	32	x
8	8-24	F3850	2	Proprietary	5	1	64	0.11	64	1	1/10	

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support				
x	x	x	x	x	x	For severe environmental operation conditions: -55°C to 85°C, 5 G vibration — 5 Hz to 2 kHz, 15 G shock — 11 ms, 0 to 95% humidity.	SECS80/10A	Titan/SESCO	5
x	x	x	x		x	Two programmable 16-bit BCD and binary timers, eight-level programmable interrupt control, power-fail memory protection.	iSBC80/24A	Intel	
			x		x	Single board computer	mBLC80/05	MicroInds	
			x		x	Single board computer	mSBC80/05	MicroInds	
			x		x	Single board computer	mSBC80/16D	MicroInds	
	x			x	x	Includes two iSBX connections, dual-ported RAM, two 16-bit counter/timers	44-002	Anasco	10
x	x	x	x	x	x	Includes CRT display controller and ASCII keyboard input port.	MC85	Comark	
					x	Accepts low-level signal down to 10 mV.	DT3754	DataTrans	
x	x		x	x		Seven CPU boards in series. DS board has math processor and 12 interrupt inputs.	AMSSeries	Siemens	
x	x	x	x	x	x	Four-channel communications computer or intelligent slave for communications expansion. Twelve levels of programmable interrupt control.	iSBC544	Intel	
					x	For severe environmental operation conditions: -55°C to 85°C, 5 G vibration — 5 Hz to 2 kHz, 15 G shock — 11 ms, 0 to 95% humidity.	SECS80/30	Titan/SESCO	15
					x	Has both 8085 and 8088 processors, only one of which operates at a time. Optional battery-backed calendar clock, math chip.	SECS80/544	Titan/SESCO	
x	x	x	x	x	x	Three sockets for distributed digital I/O processing, 12 levels of programmable interrupts, three programmable counters.	iSBC569	Intel	
x	x	x	x	x	x	Software-transparent to Intel SBL90/05, has three SBX connectors, fast-mode selection for CPU clock, needs ± 12V for RS-232.	ZX80/15	Zendex	
x	x	x	x	x	x	Wire-wrappable kluge card in Multibus form-factor, except double height. Four 28-pin RAM/ROM sockets.	DCSIWW/88	DistComp	
	x			x	x	Intelligent communications controller. Can run an operating system for development of communications protocol.	DCSSI08	DistComp	20
x	x	x	x	x		See iSBC86/14. ROM/PROM expandable to 64K bytes with iSBC 341 Multimodule.	iSBC88/25	Intel	
						12-bit 20KHz A to D converter with programmable gain, 16-different 1/32 single-ended analog, input channels, on-board 21V power supply for E <sup>2</sup> PROM modification.	mSBC88/40	MicroInds	
			x		x	Same as 88/40 Plus RAM.	mSBC88/40A	MicroInds	
x	x	x	x	x	x	Measurement and control computer. On-board 12-Bit, 32 channel A/D converter, 3 iSBX connectors, 3 programmable timers, 4 EPROM sockets.	iSB88/40A	Intel	
				x	x	Includes two iSBX connections, two 16-bit counter/timers	44-001	Anasco	25
x	x	x	x	x	x	RAM, ROM, PROM sockets, wire-wrappable kluge card in multibus form factor, except double height.	DCS/iWW/8B	DistComp	
	x			x	x	Intelligent communications controller. Can run an operating system for development of communications protocol.	DCS/SI08	DistComp	
x	x	x	x	x	x	Intended as coprocessor for DCS 86/16 or as 8-bit processor for Multibus systems. Three timers.	DCS86/8	DistComp	
						Two SBX sites for further expansion, identical to Intel model	MSBC 80/16	MicroInds	
				x	x		SECS80/544A	Titan/SESCO	30
			x	x	x	Power-fail interrupt logic for RAM battery back-up	SECS85/10	Titan/SESCO	
			x	x	x		SECS88/10	Titan/SESCO	
			x	x	x	Includes 8087 Numeric Coprocessor	SECS88/20	Titan/SESCO	
x	x	x	x			2 RS-232, I/O Rack Module Interface 7 other parallel ports with 74 lines.	DSB3180	Davidge	
x	x	x	x	x		IBM PC/XT compatible, 500 mA.	MicroPC	Faraday	
x	x	x	x	x		IBM PC/XT compatible, CMOS version, 150 mA.	MicroPC/ CMOS	Faraday	
	x	x			x	One-megabyte address capability, memory-mapping RAM, byte-wide memory, on-card floppy disk interface, arithmetic processor and DMA.	DCM1	Fairchild	

Bold face indicates additional data is provided on the page noted.

MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8-32	NSC800	2	Proprietary	± 5	1	20	2.4	64	1.15/3	2/2	
8	8	Z80	8	Proprietary	5	2	32	9.6	128	28/92	20/36	
8	8	Z80	8	Proprietary	5	2	32	9.6	128	28/92	20/36	
8	8	Z80	8	Proprietary	5	2	32	9.6	128	28/92	20/36	
8	8	Z8	3.7	Proprietary	5	2	40		2	2/0	0/4	
8	8-32	Z80	2.457	Proprietary	5	1	16		64	16	0/4	
8	8-32	Z80	2.457	Proprietary	5	1	16		64	4	0/4	
8	8	Z80A	4	Proprietary	± 16,8		24		64	2	6	
8	8	Z80A	4	Proprietary	5, ± 12	2	16	800	64	2/16	2/64	
8	8	Z80A	4	Proprietary	5	1		9600	32	8/8	16/32	
8	8	Z80A	4	Proprietary	5	1		9600	32	8/8	16/32	
8	8-24	6808	1/2	Proprietary	5, ± 12	1	1	19.2		2	8	
8	8	8031	11.0592	Proprietary	5, ± 12	1	16	19.2K	128K	8/64	8/64	
8	8	8031	12	Proprietary	5, ± 12	2	48	1024	120	8/60		X
8	8	8031	12	Proprietary	5, ± 12	2	48	1024	120	8/60		x
8	8	8051	4/12	Proprietary	5	3	3	62.5		4/16	8/64	
8	8	8052	11	Proprietary	5, ± 12	2	16	19.2	128	8/64	4/64	x
8	8	80188	6	Proprietary	5	2	32	19.2	1 MB	256/572	8/448	x
8	16	80188	8	Proprietary	5, ± 12	3	24	1.5M	1MB	256/500	192	x
8	16	80188	8	Proprietary	5	2	24	38.4	1 MB	126	64	x
8	8	6502	1/2	Proprietary	5/ ± 12	1/3	32	19.2	64	1/3	0/8	
8	8	6502	1/2	Proprietary	5	1	16		64	1	0/64	
8	8	6502	1/4	Proprietary	5	1	16		64	2/16	0/64	
8	8	6502	4	Proprietary	5	1	32	19.2	64	1/2	0/16	x
8	8	65802	2	Proprietary	5	1	16		64	1	0/8	
8	8	65802	4	Proprietary	5	1	16		64	2/8	0/32	
8	8-24	6800	1	Proprietary	5	1	40	19.2	64	1/2	0/32	x
8	8-24	6800	1	Proprietary	5, ± 12	2	20	19.2	64	1/2	0/32	x
8	8-24	6800	1	Proprietary	5, ± 12	1	40	19.2	64	1/2	0/16	x
8	8-24	6800	2	Proprietary	5	1	40	19.2	64	1/2	0/32	x
8	16	6802	1	Proprietary		1	32		64	1.4	0/16	
8	8-24	6802	1	Proprietary		1	40		64	0/2	0/8	
8	8-24	6802	1/2	Proprietary		0	0		64	0/4	0/32	
8	8-24	6809	1	Proprietary		1	40		64	0/2	0/8	

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.

μC BOARDS



Software Support					Hardware Support	Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System					
	X	X				NSC800 evaluation board. Two 16-bit programmable counters/timers, RS232 interface, Wire Wrap area.	NSC888	National	5
X	X	X	X		X	4-channel 12-bit A/D converter, EEPROM programmer, battery backed calendar/clock, 20K turbo speed BASIC interpreter/compiler.	SBS1000	Octagon	
X	X	X	X		X	8-channel 10-bit A/D converter, EEPROM programmer, battery backed calendar/clock, 20K turbo speed BASIC interpreter/compiler.	SBS1100	Octagon	
X	X	X	X		X	Three 16-bit counter/timer channels, EEPROM programmer, battery backed clock/calendar, 20K turbo speed BASIC interpreter/compiler.	SBS1200	Octagon	
X	X	X	X	X	X	Development module for Z8 microcomputer.	Z8-SCB	Zilog (3418)	10
X	X	X	X	X	X	Baud rates are software programmable from 50 to 38.4 baud. 4 8-bit counter/timer channels, 128 vectored interrupts, complete bus buffering.	Z80MCB/16	Zilog (3418)	
X	X	X	X	X	X	See above.	Z80MCB/4	Zilog (3418)	
X	X	X	X	X	X	Will operate standalone or on ICD bus.	ZPM8	IndComp	
						Optional battery-backed RAM, clock calendar and two timer/counters	Z80ALBE	Magnum	15
X	X	X	X		X	32 digital I/O lines, 3-16 bit count/timers. EPROM programmer. Resident fast floating point language.	SYS1Z	Octagon	
X	X	X	X		X	4 Channels, 12 bit A/D, 25 TTL I/O lines. EPROM programmer. Resident fast, floating point language.	SYS2Z	Octagon	
						Expansion without backplane, 40 character LED display	BCS1	Bedford	
X	X	X	X			EEPROM Support, Expansion Bus.	SIBEC-51	BinaryTech	20
X		X					CP31/535	AllenSys	
X		X				Optional 80535 CPU	DP31/535	AllenSys	
						Eight analog I/O channels for remote RS-232 control, 40 character LED display	BCS2	Bedford	
	X		X			iSBX expansion, RPOM programmer, full floating-point BASIC, buffered expansion bus.	SIBEC-52BASIC	BinaryTech	25
X	X	X	X	X	X	Rugged industrial computer in 8.8'' x 5.8'' x 2'' metal box. I/O module rack and network options.	ECX	MicroSys	
X	X		X	X		For remote control and telemetry applications	COMTROL	CompModules	
X	X	X	X	X	X	Kernal system includes RS-232 serial port, 8K battery backable static RAM, watchdog timer and data bus driver for external bus.	Tiny188	Vesta	
							6502GP	Magnum	30
						Serial data port and 16 I/O lines, two 16-bit timer/counters	6502LB	Magnum	
						Expansion capability and optional battery-backed RAM, clock calendar, two timer/counters	6502LBE	Magnum	
X	X	X	X		X	Provision for on-board power supply, buffers/terminators on parallel lines. RS232,422 or loop serial. Optional CMOS RAM.	CMC65/04	RCIData	
					X	16-bit internal operation, expandable.	65802LB	Magnum	30
					X	16-bit internal operation, expandable.	65802LBE	Magnum	
X	X	X	X		X	DMA controller, separate on-board/off-board buffers, field programmable gate array device, decode, 8-level vectored interrupt, controller.	CMC68/15	RCIData	
X	X	X	X		X	Communications version of CMC68/15.	CMC68/15C	RCIData	
X	X	X	X		X	IEEE 488(GPIB) interface, DMA controller, separate on-board, off board buffers, field programmable gate array device decode modem leads.	CMC68/15G	RCIData	30
X	X	X	X		X	2 MHz version of CMC68/15.	CMC68/15B	RCIData	
X	X	X	X		X	Possible complete microcomputer with on-board power supply and RS-422 communications adapter.	CMC68/04A	RCIData	
X	X	X	X				560	SBE	
X	X	X			X	Crystal-controlled clock, DMA, power-on reset, mapping PROM for on-board EPROM/RAM, 2 interrupts.	1020	SBE	
X	X	X	X			Three programmable counter/timers. Crystal-controlled clock, 3 interrupts, power-on reset.	590	SBE	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

Data Word Size (bits)	Instruction Word Size (bits)	General				I/O			Memory			
		CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8-24	6809	1/2	Proprietary	5, $\pm$ 12	1	40	19.2	64	2	0/16	x
8	8-40	6809	1/2	Proprietary		0	0		64	0/4	0/16	
8	16	6809	1.5	Proprietary	5, $\pm$ 12	1	32	19.2	64	1	0/16	
8	16	8X300	8	Proprietary	5		4			0.256		
8	16	80C85A	3	Proprietary	5	1	22		64	256	8	
8	8	8031	7.3728	Proprietary	5, $\pm$ 12	1	16	19.2	128	8	8/64	
8	8	8031	7.3728	Proprietary	5, $\pm$ 12	1	16	19.2	128	8	8/64	
8	8	8031	11.0592	Proprietary	5, $\pm$ 12	1	16	19.2	128	8	8/64	
8	8	8031	12	Proprietary	5	1	4	1.2	128	2	4	
8	8	8032	7.3728	Proprietary	5, $\pm$ 12	1	16	19.2	128	8	8/64	
8	8	8032	7.3728	Proprietary	5, $\pm$ 12	1	16	19.2	128	8	8/64	
8	8	8032	11.0592	Proprietary	5, $\pm$ 12	1	16	19.2	128	8	8/64	
8	8	8052	11.05	Proprietary	5, $\pm$ 12	1	24	19.2	64	8/32	31.5	
8	16	8085	3	Proprietary	5	1	22		64	256	8	
8	16	8085A	3	Proprietary	5	1	44		64	1.28	0/4	
8	8-16	8085A	5	Proprietary	5	1	0		64	0.256	0.256	x
8	8	HD64180	6	S-100	5	2		38.4	128	128		x
8	8-32	Z80A	4	S-100	8	1			64	64	0.032	
8	8-32	Z80A	4	S-100	8	2		9.6	64	96	0.032	
8	8-32	Z80A	4	S-100	8, $\pm$ 16	2	20	19.2	64	64	2/32	x
8	8-32	Z80A	4	S-100	8, $\pm$ 16	2		19.2	64	64	2/32	x
8	8-32	Z80A/B	4/6	S-100	8, $\pm$ 16	2	20	19.2	64	64/128	2/32	x
8	8-32	Z80B/H	6/8	S-100	8, $\pm$ 16	2	20	19.2	64	64/128	2/32	x
8	Var.	Z80H	8	S-100	5	6		19.2	384		0/32	
8		Z-80	4-6	SBX	5	2	4	100	64	8/32	32/32	
8	8	Z80A	4	SCSI	5	2	8	38.4	64	64	4	x
8	8	Z80A	4	SCSI	5	2	8	125	64	64	4-32	
8	8	Z80A	4	SCSI	5, $\pm$ 12	2	33	125	64	64	4/32	
8	8	64180	6	SCSI	5, 12	6	32	76.8	512	256/512	8/64	x
8	8	64180	6	SCSI	5, $\pm$ 12	2	2	38.4	256	256	32	x
8	16	80188	6/8	Slicer	5, $\pm$ 12	2	SASI	38.4	100	256	8/16	x
8	8-32	NSC-800	2	STD	5		22		64	0/24	0/24	x
8	8	NSC800	1/2.5	STD	5	1			64			x
8	8	NSC800	2.5	STD	5, $\pm$ 12		22		64	0/8	0/32	
8	8/16	NSC800	4	STD	5, $\pm$ 12	0	0	0	64	32/32	8/32	x
8	8/16	NSC800	4	STD	5, $\pm$ 12	0	0	0	64	32/32	8/32	x
8	8	NSC800	4	STD	5, $\pm$ 12	1		9.6	64	2/32	8/32	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support					Hardware Support	Comments	Model Source		Line
Assembler	Debug/Monitor	Editor	High Level Language	Operating System					
x	x	x	x		x	Separate on-board, off-board buffers, field programmable gate array device decode, 3 channel timer, modem control leads, small wire wrap area.	CMC69/15	RCIData	5
x	x	x			x	Crystal-controlled clock, DMA, power-on reset, mapping PROM for on-board EPROM/RAM, 3 interrupts.	1010	SBE	
x	x	x	x		x	Provision for on-board power supply, RS-422.	CMC69/04	RCIData	
					x	Single step control, instruction insertion from DIP switches, and Wire-Wrap development area.	8X300KT100S	Signetics	
						Eight analog inputs, 14-bit counter/timer.	SCMT11-C	Solarcom	
	x		x			Tiny BASIC/monitor debugger, 2 counter/timers, buffered expansion bus.	SIBEC-51B	BinaryTech	10
	x		x			Tiny BASIC/monitor debugger, 2 counter/timers, buffered expansion bus, 2K EEPROM.	SIBEC-51C	BinaryTech	
	x		x			Tiny BASIC/monitor debugger, 2 counter/timers, buffered expansion bus.	SIBEC-51A	BinaryTech	
x	x	x				Based on the 8031 (ROMless 8051). Serial Port RS-232C buffered.	FX31	AllenSys	
	x		x			Tiny BASIC/monitor debugger, 2 counter/timers, buffered expansion bus.	SIBEC-52B	BinaryTech	
	x		x			Tiny BASIC/monitor debugger, 2 counter/timers, buffered expansion bus, 2K EEPROM.	SIBEC-52C	BinaryTech	15
	x		x			Tiny BASIC/monitor debugger, 2 counter/timers, buffered expansion bus.	SIBEC-52A	BinaryTech	
			x			Full BASIC interpreter, 32 analog inputs, on board EPROM burner, 24 I/O lines, optional battery-backed RAM and clock calendar	8052BASIC	Magnum	
						Eight Analog inputs, 14 bit counter/timer.	SCMT11	Solarcom	
	x					256 bytes of CMOS RAM battery backup. SMP-80 is Eurocard version.	SKC85	Siemens	
					x	Milertronics will do programming and interfacing, if desired.	PDC102	MilerTron	20
x	x			x	x		CPS-Q6A	InterconMicro	
				x	x		DPC180	ACE	
				x	x	Designed for integration into a multiprocessor multiuser microprocessor system for low-cost CP/M Plus performance.	DPC83U	ACE	
x	x	x		x	x	Able to function as the system controller in a multi-user multi-processing Turbo DOS system.	Systemaster	Teletek	
x	x	x		x	x	Two-user slave card, each user with his own CPU memory and I/O.	SBC-II	Teletek	25
x	x	x		x	x	Single-user slave board intended for use in a multi-user multi-processing environment.	SBC-I	Teletek	
x	x	x		x	x	Parallel ports may be converted to IEEE 488 or SCSI interface.	SystemasterII	Teletek	
x	x	x	x	x	x	Three separate CPU sections. Each is I/O addressed separately to serve as a user processor	MULTI-SLAVE III	AdvDigital	
x	x	x	x	x	x	Single board computers, three 16-bit CTC, two RS-232, two RS-422 channels, 44 I/O channels, four opto-isolated lines	SBC1	CAN-TRON	
x	x	x	x	x		On-board floppy controller, mounts directly on 5 1/4-inch floppy, CP/M included.	Little Board	Ampro	30
x	x	x	x	x	x	Same as Model 1A but with SCSI bus interface for multi-master I/O expansion and hard disk support.	Little Board/ PLUS	Ampro	
x	x	x	x	x	x	Same size as 5 1/4 inch floppy drive. Mounts directly on it.	LittleBoard/80	Ampro	
x	x	x	x	x	x	6 RS-232, Centronics, 8' & 5 1/4' Floppy, SCSI, Expansion ports, Z-System.	DSB8000	Davidge	
x	x	x	x	x		Two serial ports (RS-232), Centronics interface, floppy controller.	DSB8100	Davidge	
x	x	x	x	x	x	Stand-alone single board computer.	SL188	Slicer	35
x	x	x	x	x	x	Battery backed up calendar clock, watchdog timer, three 16-bit counter/timers and three 28-pin memory sockets.	LPMCPU3-2	WinSystems	
	x			x	x	STD/Z80 Compatible Timing	CMOS-CPU	Intelicom	
					x	Slave processor for STD. Bus. Z80 code compatible. Has I/O plug-in socket for specific I/O requirements.	SB8275	MicroSys	
			x	x	x	Programmed version of 7410 that performs A/D data logging, waveform capture. Includes 12-bit A/D and 8/16 channel multiplexer.	7411	Sensoray (4901)	
			x	x	x	Programmed versin of 7410 that functions as a programmable controller.	7412	Sensoray (4901)	40
			x	x	x	7410 programmed as a communications controller, RS-422, 232, link and error recovery protocols supported.	7413	Sensoray (4901)	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

Data Word Size (bits)	Instruction Word Size (bits)	General				I/O			Memory			
		CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8	NSC800	4	STD	5, $\pm$ 12	1		9.6	64	8/32	16/32	x
8	8,16	V40	5/8	STD	5	2	24	38.4	1 MB	0/512	0/512	x
8	8,16	V40	5/8	STD	5	2	24	38.4	1 MB	0/512	0/512	x
8	8-32	Z-80	2.5/4	STD	5				64	0/64	0/64	x
8	8-32	Z-80	4	STD	5, $\pm$ 12	2		9.6	64	64/0	0/8	x
8	8-32	Z-80	4	STD	5, $\pm$ 12	2	20	9.6	64	64/0	0/16	x
8	8-32	Z-80	4	STD	5, $\pm$ 12	2	20	9.6	64	0/64	0/64	x
8	8-32	Z-80A	4	STD	5	1		4.8	128	2/14	1/8	
8	8-32	Z-80A/B	2.5/6	STD	5, $\pm$ 12	2		38.2	128	0/128	0/128	x
8	8-32	Z-80A/B	2.5/6	STD	5, $\pm$ 12	1	11	38.2	128	0/128	0/128	x
8	8-32	Z-80A/B	2.5/6	STD	5, $\pm$ 12	2		500	128	0/128	0/128	x
8	8-32	Z80	4/6	STD	5, $\pm$ 12	2		307	64	0/64	0/64	
8	8-32	Z80	6.144	STD	5, $\pm$ 12	2	24	38.4	512	0/64	0/64	x
8	8-32	Z80C	4	STD	5, $\pm$ 12	2	16	307	64	0/64	0/64	
8	8-32	Z80C	4	STD	5, $\pm$ 12	2		307	64	0/64	0/64	
8	8	Z80	2.5	STD	5, $\pm$ 12	2	20	19.2	128	16	48	x
8	8	Z80	2.5	STD	5, $\pm$ 12	2	20	19.2	128	0/16	0/48	x
8	8	Z80	2.5	STD	5, $\pm$ 12	2	24	19.2	128	16	48	x
8	8, 16	Z80	2.5	STD	5, $\pm$ 12	3	6	500	32	0/32	0/32	x
8	8, 16	Z80	2.5	STD	5, $\pm$ 12	3	6	500	32	0/32	0/32	x
8	8, 16	Z80	2.5/4	STD	5				64	0/64	0/64	x
8	8, 16	Z80	2.5/4	STD	5				16	0/16	0/16	x
8	8, 16	Z80	2.5/6	STD	5, $\pm$ 12	1	16	76.8	32	0/32	0/32	x
8	8, 16	Z80	2.5/8	STD	5				64	0/64	0/64	x
8	8, 16	Z80	2.5/8	STD	5, $\pm$ 12	1	8	76.8	32	0/32	0/32	x
8	8, 16	Z80	2.5/8	STD	5, $\pm$ 12	1	4	76.8	32	0/32	0/32	x
8	8, 16	Z80	4/6	STD	5, $\pm$ 12	3	6	800	32	0/32	0/32	x
8	8, 16	Z80	4/6	STD	5, $\pm$ 12	3	6	800	32	0/32	0/32	x
8	8-32	Z80A	2.5	STD	5	0	0		64	1/4	8	x
8	8	Z80A	2.5/4	STD	5, $\pm$ 12	1		0.48	64	0/32	0/32	x
8	8-32	Z80A	2.5/4	STD	5	0	0		64	8	32	x
8	8	Z80A	4	STD	5, $\pm$ 12	2	16	19.2	64	0/8	0/32	x
8	8-32	Z80A	4	STD	5	1	24	56	64	16/64	0/32	x
8	8	Z80A	4	STD	5, $\pm$ 12	2	24	19.2	128	16	48	x
8	8	Z80A	4	STD	5, $\pm$ 12	2	20	19.2	128	16	48	x
8	8	Z80A	4	STD	5	2	0	19.2	64	0/64	0/128	

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support				
			x	x	x	7410 programmed for bar code reading, printing, data buffering.	7415	Sensoray (4901)	5
x	x	x	x	x	x	Very low power, all CMOS, extended temperature (-40°C to +85°C) operation. Two RS-232/422/485 ports. Real time clock and iSBX connector.	LPM-SBC40	WinSystems	
x	x	x	x	x	x	Real time clock and watchdog timer onboard. Two DMR channels, SBX connector and four 32 pin memory sockets.	MCM-SBC40	WinSystems	
x	x	x	x	x	x	Includes four cascable counter/timers and six memory sockets. Compatible with Mostek's MDX-CPU2A/B.	MCM-CPU2A	WinSystems	
x	x	x	x	x	x	On-board floppy-disk controller for 5 1/4" or 8" drive, four cascable counter/timers and two RS-232 serial ports with modem controls.	MCMSBC	WinSystems	
x	x	x	x	x	x	Two 20-mA opto-isolated or RS-232 serial channels with modem controls. Also four cascable counter/timers, 20 TTL compatible I/O lines.	MCMSBC2	WinSystems	10
x	x	x	x	x	x	Two 20-mA opto-isolated or RS-232 serial channels with modem controls	MCMSBC3	WinSystems	
	x		x	x	x	Supports C4 BASIC and NOVOS (Non-volatile operating system) for in-system program development.	Z80-1	VersaLogic	
	x		x	x	x	Supports C4 BASIC and NOVOS for in-system program development.	VL7806	VersaLogic	
	x		x	x	x	Supports C4 BASIC and NOVOS for in-system program development.	VL7807	VersaLogic	
	x		x	x	x	Supports C4 BASIC and NOVOS for in-system program development.	VL7842	VersaLogic	15
x	x	x	x	x	x	Full synchronous and asynchronous operation, serial I/O. Four counter timers. Replaces DSTD-102 from DY-4.	MCM102	WinSystems	
x	x	x	x	x	x	Runs all Z-80 software. Two timers, plus watchdog timer. 2 channel DMA. Hardware multiply and memory management unit.	MCM-SBC6	WinSystems	
x	x	x	x	x	x	Very low power, extended temperature operation -40°C to +85°C. Precision powerfail reset. 4 counter/timers.	LPM-SBC3	WinSystems	
x	x	x	x	x	x	Full sync and async serial I/O. Extended temperature operation -40°C to +85°C. Very low pressure required.	LPM102	WinSystems	
			x	x		Parallel port with Z80 PIO FIG-FORTH Monitor.	M/E300	Mitchell	20
x		x	x	x		CMOS version of the M/E300	M/E300C	Mitchell	
			x	x		On board IEEE 488 controller, talker, listener, FIG-FORTH monitor.	MIE200	Mitchell	
x	x	x	x	x	x	Triple DART, RS-232	05324-01	STDMicro	
x	x	x	x	x	x	Triple SIO, RS-232	05324-11A	STDMicro	
x	x	x	x	x	x		05310	STDMicro	25
x	x	x	x	x	x		05320	STDMicro	
x	x	x	x	x	x	PIO with serial SBC	05323	STDMicro	
x	x	x	x	x	x		05321	STDMicro	
x	x	x	x	x	x	Centronics port	05322	STDMicro	
x	x	x	x	x	x	DMA with RS-232	05326	STDMicro	30
x	x	x	x	x	x	Triple DART, RS-232	05324-02/3	STDMicro	
x	x	x	x	x	x	Triple SIO, RS-232	05324-12/13A	STDMicro	
	x				x	Optional external clock input. Three state bus drivers may be disabled for DMA observation. Single +5v operation. Addressable expansion to 116 kbytes.	7803A	Pro-Log	
x	x	x	x	x	x	Four JEDEC memory sockets, serial port, 4-channel counter/timer.	SB8010	MicroSys	
	x				x	Counter/timer with 6 channels, 2 frequency options single +5v operation, DMA compatibility to memory, compatible with all Z80 interrupt modes.	7804	Pro-Log	35
x	x	x	x	x	x	2 JEDEC memory sockets, 2 serial ports, 2 parallel ports, 4-channel counter/timer, battery-backed clock calendar.	SB8020	MicroSys	
	x		x		x	Memory mapping and I/O expansion line, programmable serial port.	MCPU800	Miller	
			x	x		On board IEEE 488 controller, talker, listener, FIG-FORTH monitor.	M/E200A	Mitchell	
			x	x		Parallel port with Z80 PIO FIG-FORTH Monitor.	M/E300A	Mitchell	
	x			x	x	Z80A-DART and Z80A-CTC provide two RS-232C and four counter/timer channels.	7806	Pro-Log	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8-32	Z80A	4	STD	5	0	0		64	2	8	x
8	8-32	Z80A	4	STD	5, ± 12	2		9.6	128	0/128	0/128	x
8	8-32	Z80A	4	STD	5, ± 12	2		9.6	128	0/128	0/128	x
8	8-32	Z80A	4	STD	5				128	0/32	0/32	x
8	8-32	Z80A	4	STD	5, ± 12	2		19.2	64	64/64	0/16	x
8	8-32	Z80A	4.0	STD	5,12	8	24	56	64	64	16	x
8	8	Z80A	4.0	STD	5, ± 12	2	20	19.2	128	0/16	0/48	x
8	8-32	Z80C	2.5,4	STD	5				64	0/64	0/64	x
8	8,16	80C88	5	STD	5, ± 12	2		19.2	1028		0/16	x
8	8,16	80C88	5/8	STD	5	1		38.4	1 MB	0/64	0/128	
8	8,16	80C88	5,8	STD	5	1		38.4	1 MB	0/64	0/128	
8	16	8088	5	STD	5, ± 12	2	16	19.2	1 MB	8/256	0/512	
8	16	8088	5	STD	5, ± 12							
8	8,16	8088	5/8	STD	5	1		38.4	1 MB	0/64	0/128	
8	16	8088	5/8	STD	5				2 MB	0/1 MB	0/1 MB	
8	16	8088	8	STD	5, ± 12	2	16	19.2	1 MB	8/256	0/512	
8	8	64180	6	STD	5, ± 12	2	0	19.2	512	0/128	0/128	x
8	8	64180	6	STD	5, ± 12	2	0	76.8	512	512/512	0/32	x
8	8	64180	6	STD	5, ± 12	2	14	19.2	512	256/256	8/32	x
8	8	64180	6	STD	5, ± 12	2	17	19.2	512	256/256	8/32	x
8	8-32	64180	6,144	STD	5, ± 12	4		307	512	0/64	0/64	x
8	8-32	64180	6,144	STD	5	2	24	38.4	512	0/64	0/64	x
8	8-16	280	4,6	STD	5, ± 12	2		19.2	256			x
8	8-16	280A	2,4,6	STD	5, ± 12				128		28	
8	8	64180	6	STD	5	2	16	19.2	512	256	16/128	x
8	8	6502	1	STD	5, ± 12	3	16		64	8	8	
8	8	6502	2	STD	5	0	72		64	8/56	8/56	
8	8	6502	2	STD	5	0	72		64	8/56	8/56	
8	8	6502	2	STD	5, 12	1	56	19.2	64	8/56	8/56	
8	8	6502	2	STD	5, 12	1	56	19.2	64	8/56	8/56	
8	8	6502	2	STD	5	2	0	19.2	64	8/56	8/56	
8	8	6502	2/4	STD	5	1	32	19.2	128	2/48	0/48	x
8	16	6800	1	STD	5	0	0		64	0/2	0/8	
8	8-24	6800	4	STD	5	0	0		64	1/4	8	x
8	8-20	68008	8,10	STD	5, ± 12	2		19.2	1MB	64	64	x
8	8-24	6809	1/2	STD	5, ± 12	1	0	19.2	64	4/40	8/40	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support				
	x				x	10 msec. timer w/ interrupt capability. DMA compatibility to external memory. Compatible with Z80 interrupt modes. Addressable exp. to 128 kbytes.	7880	Pro-Log	5
			x	x	x	CMOS Version of VL-7806.	SL78C06	VersaLogic	
			x	x	x	CMOS Version of VL-7806.	VL78C06	VersaLogic	
					x	Direct plug-in replacement for Pro-Log 7804A.	VL7804A	VersaLogic	
x	x	x	x	x	x	Four cascadeable counter/timers, two serial RS-232 channels and a 28-pin memory socket.	MCMSBC4	WinSystems	
x	x	x	x	x	x	On board floppy disk controller handles four drives, memory mapping, reset interrupt.	MCPU900	Miller	10
x		x	x	x		CMOS version of te M/E300A	M/E300CA	Mitchell	
x	x	x	x	x	x	CMOS Z80 processor card, four counter/timer channels and 6 byte-wide memory sockets.	LPMCPU2-A	WinSystems	
x	x				x	CMOS 8088 card, two RS-232 or opto isolated 20 mA serial ports, three 16-bit counter/timers, plus interrupt controller.	LPM8088-5	WinSystems	
x	x	x	x	x	x	Very low power, all CMOS, extended temperature (-40°C to +85°C operation. RS-232/485 serial port, 8087 socket, 82C59 PIC and iSBX connector.	LPM-SBC8	WinSystems	
x	x	x	x	x	x	Very low power, all CMOS, extended temperature (-40°C to +85°C) operation. RS-232/485 serial port, 8087 socket, 82C59 PIC and iSBX connector.	LPMSBC8	WinSystems	15
	x				x	NEC V20, IBM PC/XT peripheral devices, timekeeper, power-fail protection, optional battery backup, optional CMOS version.	ZT8808	Ziatech	
					x	Bubble memory data storage unit with 760 Kbyte industrial removable cartridge, media compatible with Magnesys IBM PC subsystem.	ZT8854	Ziatech	
x	x	x	x	x	x	8 Interrupts with 8259 PIC. 8087 Coprocessor socket, three 16-bit counter/timers, watchdog timer and SBX connector.	MCM-SBC8	WinSystems	
					x	2 Mbyte extended main memory or 2 Mbyte PROM/RAM disk capability, EMS and E <sup>2</sup> MS specification for 16K mapping, eight 32-pin JEDEC sockets.	ZT8825	Ziatech	
	x				x	NEC V20, IBM PC/XT peripheral devices, timekeeper, power-fail protection, optional battery backup, optional CMOS version.	ZT8809	Ziatech	20
x	x	x	x	x		2 RS-232, 4 JEDEC Sockets 5 1/4" Floppy Controller (1773).	DSB2100	DSB Systems	
x	x	x	x	x		2 RS-232, 512K DRAM, JEDEC Socket.	DSB2101	DSB Systems	
x	x	x	x	x		2 RS-232, 256K DRAM, JEDEC Socket Centronics, Interrupting Clock/Cal.	DSB2106	DSB Systems	
x	x	x	x	x		2 RS-232, 256K DRAM, JEDEC Socket SCSI.	DSB2108	DSB Systems	
x	x	x	x	x	x	Very low power, -40°C to +85°C operation. Runs all Z80 software and interrupts. Synchronous communications on 2 channels. Two timers.	LPM-SBC5	WinSystems	25
x	x	x	x	x	x	Very low power, -40°C to +85°C operating temperature. Runs all Z80 software. Watchdog timer, Sleep mode, 2 channel DMA. 2 counter/timers.	LPM-SBC6	WinSystems	
	x		x	x	x		ACS80	Datricon	
					x	Interchangeable w/mostek MDX-CPUZA, but with re-worked reset circuit and 28-pin sockets.	ACS2A	Datricon	
	x				x	Links to PC for software development	8000	Cubit	
	x						CPU100	Techno	30
x		x	x	x	x		7510	Cubit	
x		x	x	x	x	CMOS version of 7510	7520	Cubit	
x		x	x	x	x		7530	Cubit	
x		x	x	x	x	CMOS version of 7530	7540	Cubit	
x		x	x	x	x	Includes integral color graphics CRT Controller and Floppy Disk Controller	7550	Cubit	35
x	x		x	x	x	Mixed RAM, ROM sockets 1 serial port, 2 parallel ports and 4 timers. Power fail interrupt and memory protection circuitry allow CMOS RAM to be battery backed.	10812	Enterprise	
x	x	x	x			Fuse-link PROMs used for memory, I/O and DMA control.	ACS/68	ApplSys	
x	x		x		x	Optional external clock input. Tri-State bus drivers may be disabled for DMA operation. Programmable memory for I/O.	7802	Pro-Log	
	x		x	x	x	Battery-backed clock, internal 16-bit counter, I/O device decoding compatible with 68000, interrupt vectoring compatible with Z80 peripherals	ACS68SBC	Datricon	
x	x	x	x	x	x	Software support is OS9 or Sphere. Serial port is RS232 or RS422 with modem control.	ACS09	Datricon	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8-32	6809	4	STD	5	0	0		64	2	8	x
8	8	6809	4/8	STD	5	1	32	19.2	128	2/48	0/48	x
8	8-16	80C85	6.2	STD	5	1		9.6	64	0/32	0/64	x
8	16	80C85A	3	STD	5	1	22		64	256	8	
8	16	80188	5/8	STD	5				1Mb	0/32	0/64	x
8	8	8085	3.072	STD	5, $\pm 12$	2	2	56/4.8	64	1/1	0/8	
8	16	8085A	0.5/5	STD	5	1	0	19.2	64	0.25/2	0/8	
8	8-24	8085A	3/3.125	STD	5	1	0		64	1/4	8	x
8	8-24	8085A	6.144	STD	5	1	0	9.6	64	2	8	x
8	16,32	8088	4.7	STD	5				64	2/64	2/128	x
8	8	8088	5	STD	5	2	16	19200	192	16/64	64/32	
8	8,16	8088	5	STD	5, $\pm 12$	2		19.2	1Mb	0/0	0/16	x
8	16	8088	5	STD	+5, $\pm 12$	1	16	19.2	1000	0/32	0/64	
8	1	8088	5/8	STD	5, $\pm 12$	1	16	19.2	1MB	0/8	0/32	x
8	16	8088	5/8	STD	5				1Mb		0/16	
8	16	8088	8	STD	+5, $\pm 12$	1	16	19.2	1000	0/32	0/64	
8	16	8088	8	STD	5, $\pm 12$	1	16	19.2	1Mb	0/32	0/32	
8	8	V40	7.4	STD bus	5	2	24	19.2	1 MB	64/64	64/128	x
8	8	8088	4.77	STD bus	5,12	2	16	19.2	1 MB	256/572	8/64	x
8	8	64180	4.6	STD bus	5	2	2	19.2	512	64/64	64/128	x
8	8	Z80A	4	STD/SCSI	5				64	to 64	to 64	
8	8-32	Z80	2.5	STD-Z80	5				64			
8	8-24	Z80	2.5/4	STD-Z80	5				128	0/16	0/16	x
8	8-24	Z80	2.5/6	STD-Z80	5	1	16	76.8	128	0/32	0/32	x
8	8-24	Z80	2.5/6	STD-Z80	5	3		76.8	128	0/32	0/32	x
8	8-24	Z80	2.5/8	STD-Z80	5				128	0/64	0/64	x
8	8-24	Z80	2.5/8	STD-Z80	5	1	16	76.8	128	0/32	0/32	x
8	8-24	Z80	2.5/8	STD-Z80	5	1		76.8	128	0/32	0/32	x
8	8-24	Z80	2.5/8	STD-Z80	5	1		76.8	128	0/32	0/32	x
8	8-24	Z80	2.5/8	STD-Z80	5	1		76.8	128	0/32	0/32	x
8	8-32	Z80	2.5/8	STD-Z80	5				64	0.256	0/4	
8	8-32	Z80A	3.68	STD-Z80	5,12	1	8	9.6	64	64	0/32	x
8	8-32	Z80A	3.68	STD-Z80	5,12	1	8	9.6	64	0/40	0/64	x
8	8	HD64180	8	STDbus	5, $\pm 12$	2			512	512	Opt.	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support					Hardware Support	Comments	Model	Source	Line
Assembler	Debug/Monitor	Editor	High Level Language	Operating System					
					x	10 msec. timer w/ interrupt control. DMA control to external memory. Dynamic RAM refresh clock. Single + 5v operation.	7889	Pro-Log	5
x	x		x	x	x	Mixed RAM, ROM sockets 1 serial port, 2 parallel ports and 4 timers. Power fail interrupt and memory protection circuitry allow CMOS RAM to be battery backed.	10809	Enterprise	
x	x	x	x	x	x	CMOS, four 28-pin byte-wide sockets. Equivalent to Pro-Log 78C05 and 78C15 processors.	LPM7815	WinSystems	
						Eight analog inputs, 14-bit counter/timer.	SCMT85-C	Solarcom	
	x				x	2 DMA on-board	ZT8814/8815	Ziatech	
	x				x	Complete STD system with 8085, 2-RS-232C, GPIB controller	ZT7805	Ziatech	10
x	x	x	x		x	Memory and peripheral I/O cards are available for systems.	ACS/80	ApplSys	
x	x		x		x	Optional external clock input. Tri-State bus drivers may be disabled for DMA operation. Addressable words expandable to 116K bytes.	7801	Pro-Log	
	x				x	10 msec. timer w/ interrupt control. Control port for memory expansion. RS232C interface for CRT terminal. Selectable DTE/DCE configuration.	7885	Pro-Log	
						Supports memory battery backup.	SCMT88	Solarcom	
x	x	x	x		x	8 channels, 8 bit A/D, 26 TTL I/O Lines. EPROM programmer. Resident fast, floating point language.	SYS3Z	Octagon	15
x	x				x	Two 20-mA opto-isolated or RS-232 serial channels with modem controls, three counter/timers plus interrupt controller.	MCM8088-5	WinSystems	
	x				x	Single board 8088 (5 MHz) computer-compatible with the 8087 numeric data processor. Optional debugging monitor PROM.	ZT 8806	Ziatech	
x	x		x	x	x	8088, optional 8087, serial, parallel, timer, interrupt I/O, Link to IBM-PC.	SB8088	MicroSys	
	x			x	x	Integrated 8088 Processor. Optional development/monitor PROM, optional 8087 numeric data processor, optional IRMX-86 or CP/M-86 silicon operating system.	ZT8812/8813	Ziatech	
	x				x	Single board 8088 (8 MHz) computer-compatible with the 8087 numeric data processor. Optional debugging monitor PROM.	ZT 8807	Ziatech	20
	x				x	Intelligent OEM Serial Controller. On-board 8MHz 8088 slave CPU, serial port for RS-232C or RS-449, multimodule expansion socket.	ZT8830	Ziatech	
	x				x	All CMOS, 8-bit A/D converter, battery-backed clock/calendar and RAM, Debug firmware Links to PC for software development.	8400	Cubit	
x	x	x	x	x	x	100% PC clone integrated onto backplane of 16-slot cardcage, includes CGA,FDC, COM1, COM2, and LPT1.	CLONE/CAGE	MicroSys	
	x				x	All CMOS, 8-bit A/D converter, battery-backed clock/calendar and RAM, Debug firmware links to PC for software development.	8020	Cubit	
x	x	x	x	x	x	STD bus form factor, 8 byte-wide sockets, CTC, SCSI (full ANSC X3T9.2), STD interrupt structure	SCSI/IOP-STD	Ampro	25
x	x	x	x	x	x	Six 24 pin sockets, four cascable counter/timer channels, automatic, transparent dynamic memory refresh.	MDX-CPU2A	Thomson	
						On-board CTC.	5320	STDMicro	
						General-purpose parallel interface, programmable baud rate.	5323	STDMicro	
						Three synchronous/asynchronous serial channels, programmable baud rate.	5324	STDMicro	
						On-board CTC.	5321	STDMicro	30
						Centronics interface, programmable baud rate.	5322	STDMicro	
						Clock/calendar, programmable baud rate.	5327	STDMicro	
						IEEE488 GPIB, programmable baud rate.	5328	STDMicro	
						9511 arithmetic processor, 9512 floating-point processor, programmable baud rate.	5329	STDMicro	
x	x	x	x	x	x	Flexible memory decoding for EPROM and RAM, four counter/timer channels. CPU1A allows system reset to be generated off the board.	MDX-CPU1	Thomson	
x	x	x	x	x	x	Modem, eight parallel lines plus handshake.	MDX-CPU3	Thomson	
x	x	x	x	x	x	Modem, eight parallel lines plus handshake.	MDX-CPU4	Thomson	
	x			x	x	SCSI interface, RS-232 and RS-422/485 serial ports	80-0037	MicroAide	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

Data Word Size (bits)	Instruction Word Size (bits)	General				I/O			Memory			
		CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8	NSC800	3.144	STDbus	5, $\pm$ 12	1	16	19.2	64	0/32	0/32	x
8	8	Z80	2.5/4	STDbus	5	2		19.2	128			
8	8	Z80A	3.69	STDbus	5, $\pm$ 12	1	8	9.6	128	64/64	8/32	x
8	8	Z80A	4	STDbus	5			1	280	/640	/64xx	x
8	8	Z80	2.5/6	STDbus	5	0	0	0	64	0/96	0/64	x
8	8	Z80	2.5/8	STDbus	5, $\pm$ 12	2	8	19.2	64	0/64	0/32	x
8	8	Z80	4	STDbus	5, $\pm$ 12	1		9.6	64	2/64	4/64	x
8	8	Z80	4/6	STDbus	5				128	16	16	x
8	8	Z80	4/6	STDbus	5				128	64	64	x
8	8	Z80	4/6	STDbus	5	1	16	76.8	128	32	32	x
8	8	Z80	4/6	STDbus	5	1	16	76.8	128	32	32	x
8	8	Z80	4/6	STDbus	5	3		76.8	128	32	32	x
8	8	Z80	4/6	STDbus	5	1		76.8	128	32	32	x
8	8	Z80	4/6	STDbus	5	1		76.8	128	32	32	x
8	8	Z80	4/6	STDbus	5	1		76.8	128			x
8	8	Z80	6	STDbus	5, $\pm$ 12	2		19.2	256	65	Opt.	x
8	8	Z80	6	STDbus	5				256	Opt.	Opt.	x
8	8	Z80	6	STDbus	5	2	16	19.2	256	Opt.	Opt.	x
8	8	Z80	6	STDbus	5, $\pm$ 12				256	Opt.	Opt.	x
8	8	Z80	6	STDbus	5, $\pm$ 12	2	16	19.2	256	Opt.	Opt.	x
8	8-32	Z80a	4	STDbus	5, $\pm$ 12	2	20	667	128	0/256	0/256	x
8	8-24	6801	1	STDbus	5	1				128		
8	8-24	6803	1	STDbus	5	1				2/8		
8	8-16	6809	1/2	STDbus	5				128			
8	8/16	6809	1/2	STDbus	5, $\pm$ 12	2			128			
8	8-16	6809	1/2	STDbus	5, $\pm$ 12	1			128			
8	8-16	6809	2	STDbus	5	0	0		1 MB			
8	8	8031	7.28	STDbus	5	1	16	9.6		1	4	
8	8	8085A	4	STDbus	5, $\pm$ 12	1	24	19.2	128	0/16	8/64	x
8		8088	5/8	STDbus	5		3		272	256	16	
8	8-32	64180	6.144	STDbus	5, $\pm$ 12	4		512	64	0/64	0/64	x
8	8	80188	5/10	STDbus	5	2	24	19.2	1MB	1MB	128	x
8	8	68B09E	2	STDbus	5, $\pm$ 12	1	16	19.2	128	Opt.	Opt.	x
8	8-32	6809	2	STDbus	5, $\pm$ 12	2	36	19.2	128	0/16	0/32	
8	8-16	6809	2	STDbus	5	0	0		64			
8	8	8031	12	STDbus	5	2	59	38.4	128	0/16	0/16	
8	8	8032	12	STDbus	5	2	59	38.4	128	0/16	0/16	
8	8	8052	11	STDbus	5, $\pm$ 12	2	16	19.2	128	8/64	8/64	x
8	8	8052-BASIC	12	STDbus	5	2	59	38.4	128	8/16	8/16	
8	16	8085	3	STDbus	5	1	22		64	256	8	
8	8-16	8085	6.2	STDbus	5	1		9.6	64	0/32	0/64	x
8	8-24	8085A-2	5	STDbus	5, $\pm$ 12	1	23	19.2	64	1/4	16	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Hardware Support	Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System						
x	x	x	x	x	x		Low power, sockets for 16-channel 12-bit A/D converter	7410	Sensoray (4901)	5
x	x				x		Multifunction Processor Card	MF80A	Matrix	
	x		x	x	x		Real-time clock/calendar with on-board battery back-up	STD247	Micro-Link	
	x		F	o	u		r Programmable Counter/Timers	STD205	Micro-Link	
x	x	x	x	x	x		4 separate counter/timer channels, memory bank switching	CPU2	CompDyn	
x	x	x	x	x	x		2 serial channels, 1 parallel printer port, 2 timers, battery-backed clock/calendar	CPU9	CompDyn	10
x	x	x	x	x	x		Integer BASIC interpreter and monitor ROM included	ANC7880	Antona	
							On-board CTC	DSB5320	Davidge	
							On-board CTC	DSB5321	Davidge	
							Centronics interface, programmable baud rate	DSB5322	Davidge	
							General purpose parallel port, programmable baud rate	DSB5323	Davidge	
							3 synch/asynch serial channels, programmable baud rate	DSB5324	Davidge	
							Clock/calendar, programmable baud rate	DSB5327	Davidge	
							IEEE 488 (GPIB) interface, programmable baud rate	DSB5328	Davidge	
							9511 arithmetic processor, 9512 floating point processor, programmable baud rate	DSB5329	Davidge	
	x			x	x		Controller, Z80 DART or RS-232, two 28-pin memory sockets	80-0018	MicroAide	20
					x		Controller with 8 28-pin sockets for JEDEC STD memory	80-0020	MicroAide	
	x				x		Two RS-232 serial ports, Centronics-compatible parallel port	80-0026	MicroAide	
					x		Battery-backed memory and 58274 calendar/clock	80-0027	MicroAide	
	x				x		Controller with GPIB/IEEE-488, 2 RS-232 serial ports	80-0036	MicroAide	
							Master/slave capabilities for multiple CPUs	RSD7808	Robotrol	25
x	x				x			CP1L1	Matrix	
x	x				x		For Test Instrumentation and Machine Control	CP3	Matrix	
x	x	x			x		On-board Watchdog Timer	CP9B	Matrix	
x	x	x			x		Multifunction Processor Card	MF9B	Matrix	
x	x	x			x		Runs OS/9 6809 Level One	SP9B	Matrix	30
x	x	x	x	x	x		Runs OS9/6809 Level 2	CPU/MMU	Sys Datar	
	x	x	x	x			Remote slave processor controller board; communicates to a host controller via RS-422 serial link	VSC31	Gordos	
	x		x	x	x		Three programmable timer/counters. Real-time calendar/clock with battery backup.	STD245	Micro-Link	
			x	x	x		STD 8088 compatible EGA video graphics controller. IBM MDA/CGA/EGA supported plus Hercules, keyboard port, BIOS included	ZT8844	Ziatech	
x	x	x	x	x	x		Uses Hitachi 64180 (Z-80-equivalent) processor; 4 serial I/O channels, Two 16-bit timers, watchdog timer, three 28-pin sockets, DMA	MCMSBC5	WinSystems	35
x	x	x	x	x	x		SBX expansion connector. Two RS-232 serial ports or one RS-232 and one RS-485.	CPU188	CompDyn	
	x				x		Battery-backed memory and calendar/clock, serial RS-232 port	80-0033	MicroAide	
								TS9B	Matrix	
x	x	x	x	x	x		Runs OS9/6809 Level 1	CPU09	Sys Datar	
							RS-232, 48 ports, timers and 4-8 K RAM/PROM sockets	CPU31	AdvMicroSys	40
							8032 processor, stand-alone or STD bus, RS-232, 48 ports, timers and 32K RAM/PROM sockets.	CPU32	AdvMicroSys	
x	x	x	x	x	x		Floating point BASIC interpreter, on board PROM programmer, autostart mode	ANC7852	Antona	
	x	x	x	x			Single board computer, BASIC interpreter, stand-alone or STD bus, RS-232, 48 ports, 8K RAM, 8K EE ROM.	BAS52	AdvMicroSys	
							Eight Analog inputs, 14 bit counter/timer.	SCMT85	Solarcom	
x	x	x	x	x	x		Four 28-pin byte-wide sockets. Equivalent to the Pro-log 7805 and 7815 processors.	MCM7815	WinSystems	40
x	x	x	x	x	x		CP/M type Boot ROM capacity, Timer, RS-232 4 vectored interrupts	CPU1850A	Sertek	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8	8	8088	5	STDbus	5	2		19.2	1MB	0/64	0/128	
8	8	Z80-B	6	S100	8	2	16	19.2	64	128	2	x
8	16	8088	5	S100	5, $\pm 12$	2	8	819	1024	64/1024	4/0	
8	8	68008	8	VMEbus	5, $\pm 12$	2	32	19.2	512	0/512	32/64	
8/16	8	INS8073	4		5	1	27	4.8	64	2	0/4	
8/16	8	68HC11	1/8		5, $\pm 12$	2	40	131	64	8	16	
8/16	8-32	8086	5/8	Multibus	5, $\pm 12$	1	24	38.4	1 MB	128	0/32	
8/16	8-32	8086	5/10	Multibus	5, $\pm 12$	2	24	38.4	1 MB	8/32	0/512	
8/16		80186	10	Multibus						32	32	x
8/16	8-24	80286	8	Multibus	5, $\pm 12$	4	24	38.4	16 MB	1 MB/2 MB	0/128	x
8/16	8/16	80186	8	Multibus	5	8		76.8	16 MB	512	256	x
8/16	8-32	80186	8	Multibus	5	2	24	125	1MB	32/64	128/256	x
8/16	16	80186	8	Multibus	5, $\pm 12$	8		880	512		25	x
8/16	16	80186	8	Multibus	5, $\pm 12$	4		880	512		25	x
8/16	8,16	80186	8	Multibus	5, $\pm 12$	1 or 2	24	19.2	16Mb	512/1Mb	0/128	x
8/16	8-40	80286	6	Multibus		2	24	615	1Gb	48	256	
8/16	8-40	80286	8	Multibus	5, $\pm 12$	4	24	—	16MB	1MB	128	x
8/16	8-24	80286	8	Multibus	5	2	24	56	16 MB	32	512	
8/16	8-24	80286	8	Multibus	5	2	24	800	16 MB	2 MB	128	x
8/16	8-40	80286	8	Multibus	5, $\pm 12$	2	24	615	16 MB	0/128	0/256	
8/16	8-40	80286	8	Multibus	5, $\pm 12$	2	24	615	16 MB	1 MB/4 MB	0/256	x
8/16	8-32	8086	5/8	Multibus	5	1	24	38.4	1MB	512/1MB	32/256	
8/16	8-32	8086	5/10	Multibus	5, $\pm 12$	1	24	38.5	16Mb	128/256	0/256	x
8/16	8-32	8086	5/10	Multibus	5, $\pm 12$	1	24	38.4	16Mb	512/1Mb	0/256	x
8/16	8,16	8086	5/10	Multibus	5, $\pm 12$	1	24	19.2	1024	1024	256	x
8/16	8-24	8086	8	Multibus	5	1	24	19.2	1 MB	128/256	0/128	
8/16	8-24	8086	10	Multibus	5	1	24	19.2	1 MB	512K/1MB	0/256	
8/16	8-32	8086-2	5/8	Multibus	5, $\pm 12$	1	24		64	512	256	x
8/16	8-32	8088	8	Multibus	5, $\pm 12$	3		800	1MB	16	64/64	x
8/16	8-32	80186		Multibus II	5,12					128	128	x
8/16	8-40	80286	8	Multibus II	5, $\pm 12$	2	24	19.2	16MB		128	x
8/16	8-40	80286	8	Multibus II	5, $\pm 12$	2	24	19.2	16MB	1MB	128	x
8/16	8/16	80286	6/10	Passive AT	5, $\pm 12$	0	0		16 MB	0		x
8/16	8/16	65816	4	Proprietary	5, $\pm 12$	2	32	19.2	16MB	8/64	0/64	
8/16	8, 16	INS8070	10	STD	5	1	24	9.6	84	2/8	8/24	

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support										Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support					
X	X	X	X	X	X			7863	Pro-Log	
				X	X	Five- and 8-inch floppy disk controller, 64K or 128K of RAM, 2K or 4K of ROM.		Super 6	AdvDigital	
X	X	X	X	X	X	User Board		DPC88U	ACE	
	X	X	X		X	Multifunction analog digital serial I/O		SL1000	SerialLab	
	X	X	X		X	Low-cost, 3x4-inch board. Includes real time clock/calendar, tiny basic.		MC-1N	Basicon	5
X	X		X	X	X	May be configured for all versions of the 68HC11		FX11	AllenSys	
X	X	X	X	X	X	Multi-master capabilities, socket for 8087, two general purpose timers, and eight levels of programmable interrupt control.		ZX86/28	Zendex	
	X					Full multi-master capabilities, fully software transparent with Intel SBC 85/05 and SBC 86/12A.		ZX86/05A	Zendex	
					X	Peripheral controller subsystem, supports two ST-506/412 drives, four SA450/460 flexible drives, and four QIC-02 streaming tape drives.		SBC 214	Intel	
X	X	X	X	X	X	Intel SBC-286/12 compatible.		ZX286/12	Zendex	10
	X		X			Eight-channel serial communications controller, optional asynchronous, X.25 and SNA on-board protocols		CD21/3518	CentData	
X	X	X	X	X	X	Six programmable timers, 27 levels of interrupt control, two iSBX connectors, iLBX memory interfacing; parallel I/O reconfigurable to SCSI interface.		iSBC186/03A	Intel	
	X			X		Includes CPU, RAM, serial I/O, ethernet controller and VRTX real-time operating executive.		CP2000	Matrox	
	X			X		Includes CPU, RAM, serial I/O, Floppy disk controller and VRTX real-time operating executive.		FP2000	Matrox	
X	X	X	X	X	X	Can contain 128Kb, 512Kb or 1Mb on-board RAM. Optional 8087 floating point processor. Optional multi-protocol dual serial interface controller.		ZX186/30	Zendex	15
X	X	X	X	X	X	Optional 80287 Numeric Data Processor, optional expansion board to 12 JEDEC 28-pin sites		iSBC286/10	Intel	
X	X	X	X	X	X	Fully compatible with Intel SBC 286/12, except it allows one SBX module, four serial interfaces and eight multiplexed DMA channels.		CD21/8286	CentData	
X	X	X	X	X		Intel iSBC-286/10a compatible		DSB286/10A	Den/Pas	
X	X	X	X	X		Intel iSBC-286/12 compatible		DSB286/12	Den/Pas	
X	X	X	X	X	X	Zero wait-state dual-port memory interface. Optional 80287 math coprocessor.		iSBC286/10A	Intel	20
X	X	X	X	X	X	1, 2, or 4 MB, zero-wait-state parity RAM and zero-wait-state memory interface. Optional 80287 math coprocessor and 82258 ADMA controller.		iSBC286/12/14/16	Intel	
X	X	X	X	X	X	512K byte on-board dual-port RAM.		iSBC86/35	Intel	
X	X	X	X	X	X	Two SBX connectors; Optional 8087 numeric data processor; Fully compatible with Intel SBC 86/30 and 86/35.		CD21/8630	CentData	
X	X	X	X	X	X	Two SBX Connectors; Optional 8087 numeric data processor; Fully compatible with Intel SBC 86/30 and 86/35.		CD21/8635	CentData	
X	X	X	X	X	X	Two 16-bit SBX connectors, 8087/8089 support		MC8630/35	Comark	25
X	X	X	X	X		Intel iSBC-86/30 compatible		DSB86/37A	Den/Pas	
X	X	X	X	X		Intel iSBC-86/35 compatible		DSB86/35	Den/Pas	
			X		X	Single board computer		mSBC86/35	MicroInds	
X	X	X	X	X	X	Three HDLC/SDLC communications channels, programmable baud rate, optional numeric data processor		iSBC88/45	Intel	
				X	X	Multibus II peripheral controller		iSBC186/224A	Intel	30
X	X	X	X	X	X	Max. baud rate 64 kb/s synchronous, also iLBX-II bus.		iSBC286/100A	Intel	
X	X	X	X	X	X	Complete integrated system, maximum baud rate 64 kb/s synchronous, also iLBX-II bus.		SYSMB2	Intel	
X	X	X	X	X	X	IBM AT compatible CPU card designed for use in a passive backplane.		CAT286	Comark	
					X	16-bit internal operation, expandable.		65816A	Magnum	
X	X	X	X		X	Similar to SYS-10A with Battery backable RAM. 8 channels of 8 bit A/D and 1 channel of D/A.		Omnocard	Octagon	35

Bold face indicates additional data is provided on the page noted.



## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
8/16	8,16	Z80A	4	STD	5	2	8	9600	128	8/24	16/40	
8/16	8, 16	8088	5	STD	5	2	16	19200	192	16/64	64/32	
8/16	8-32	8088	5	STD	5,-12	1		9.6	1MB	4/8	2/48	x
8/16	8-32	8088	5	STD	5,-12	1		9.6	1MB	8/32	2/48	x
8/16	8-32	8088	5	STD	5,-12	1		9.6	1MB	32	2/48	x
8/16	8	R65F11	1/2	STDbus	5	1	16	9.6	8/64	8/64		x
8/16	16	TMS9995	12	STDbus	5, ± 12	2	13	38.4	64	0/4	0/8	x
8/16	16	TMS9995	12	STDbus	5, ± 12	2	16	38.4	64	24/96	0/64	x
8/16	8/16	64180	6.144	STDbus	5	2	24	19.2	64	24	16	
8/16	8	6500/11	1/2	STDbus	5	1	16	9.6	8/64	8/64		x
8/16	8-16	8088	5, 12	STDbus	5	1	16	19.2	1 MB	32/32	64/64	
8/16	16	Z80/80186	4/8	S100	5, ± 12	2	8/16	819	1024	128/1024	1/16	x
8/16	8/16	8088	8	VMEbus	5	8		38.4	16 MB	64	64	
8, 16	16, 32	68000	10	Multibus	5, ± 12	2	32	19.2	16 M	128	0/192	
8, 16	16, 32	68000	10	Multibus	5, ± 12	2	32	19.2	16 M	512	0/192	
8, 16	8-32	8086-2	5/8	Multibus	5, ± 12	1	24	9.6	1 M	256	0/64	
8, 16	8-32	8086-2	5/8	Multibus	5, ± 12	1	24	9.6	1 M	512	0/256	
8, 16	8-32	8086-2	5/8	Multibus	5, ± 12	1	24	9.6	1 M	1 M	0/256	
8-16	8	F387X	2	F8		1			64	2/4	2	
8-32	24	NS32008/16/32	10		5	1	24		16 MB	32/128	1/8	
8-32	8-32	80386	16	Passive AT	5, ± 12	0	0		16 MB	16 MB	128	x
8-32	8-48	8088	5/8	STDbus	5	0	0		1 MB	0	0/32	x
8-32	8-48	8088	5/8	STDbus	5	1	8	38.4	1 MB	0/16	0/48	x
8-32	16-80	68000	8	VME	5	1	16			128/512	0/64	x
8-32	16-80	68000	8	VME	5,12	1	8	19.2	1MB	12	16	x
8-32	16, 32	68000	8	VMEbus	5, ± 12	3	24	19.2	16 M	128	16/64	
8-32	16, 32	68000	8	VMEbus	5, ± 12	3	24	19.2	16 M	512	16/64	
8-32	16, 32	68000	10	VMEbus	5, ± 12	1	24	19.2	16 M	256	16/64	
8-32	16, 32	68000	10	VMEbus	5, ± 12	1	24	19.2	16 M	512	16/64	
8-64	8-48	8088/8087	5/8	STDbus	5	0	0		1 MB	0	0/8	x
12	12	6100	0/2	Proprietary	4.5-7	0	18		384	0	0	
12	12	6100	0/2.46	Proprietary	4.5-7	0	32		48	4	12	x
12	12	6100	5.7	Proprietary	4.5-7	1	24	9.6	4	0.256	1/1	x
16	16	PDP-11	5		5	4	32	38.2	512	512	64	
16	16	Z8002	4		5, ± 12	2	40	1000	64	8/56	0/56	
16	16	8097	12		5, ± 12	2	48	19.2	48			
16	16	80286	6/10	AT bus	5	0	0		16	512	64	x
16	16	32016	10	CIM bus	5, ± 12	1		19.2	16 MB			x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support				
x	x	x	x		x	Resident floating point, real-time control lang. RS-232C/422, switchable. Auto-run on power up.	890	Octagon	5
x	x	x	x		x	2 Serial ports. Resident interactive BASIC compiler that allows real-time control. Auto-run on power up.	880B	Octagon	
	x	x	x	x	x	Self-contained computer system on STD bus card. Terminal port, printer port and EPROM programmer.	ipc-STD88-1	Vesta	
	x	x	x	x	x	Self-contained computer system on STD bus card. Terminal port, printer port and EPROM programmer.	ipc-STD88-2	Vesta	
	x	x	x	x	x	Self-contained computer system on STD bus card. Terminal port, printer port and EPROM programmer.	IPC-STD88-3	Vesta	
x	x	x	x	x	x	FORTH Kernel in CPU. Programs EPROM/EEPROM. Three 28 pin memory sockets. Can be used as a stand-alone optional floppy disk controller.	STD65F11	HiTech	10
x	x	x	x	x	x	PDOS multiuser, multi-tasking disk operating system with run-module library	SBC95-1	GW-Three	
x	x	x	x	x	x	PDOS, Improved on board memory capability	SBC95-2	GW-Three	
x	x	x	x		x	STD BASIC resident, floating point control language, iSBX multimodule I/O connector.	892	Octagon	
x	x	x	x	x	x	C language runtime code in CPU. Three 28 pin memory sockets. Can be used as a stand-alone optional floppy disk controller.	STD65C11	HiTech	
x	x	x	x		x	RS-232 serial port, resident interactive BASIC compiler allows real time control	886	Octagon	15
x	x	x	x	x	x	High-performance Dual CPU Board	DPC816	ACE	
			x			Adds 8 RS-232 interfaces to the VMEbus, two of which can optionally be RS422/449	CD23/3608	CentData	
				x	x	Includes dual-ported RAM, zero wait-state access, three 16-bit counter/timers	44-020	Anasco	
				x	x	Includes dual-ported RAM, zero wait-state access, three 16-bit counter/timers	44-021	Anasco	
	x			x	x	Includes two iSBX connections, dual-ported RAM, two 16-bit counter/timers	44-004	Anasco	20
	x			x	x	Includes two iSBX connections, dual-ported RAM, three 16-bit counter/timers	44-005	Anasco	
	x			x	x	Includes two iSBX connections, dual-ported RAM, three 16-bit counter/timers	44-006	Anasco	
x	x	x	x	x	x	Includes teletypewriter operating system and programmable baud rates.	F3870-PEP	Fairchild	
x	x	x	x	x	x	Series 32000 development board.	DB32000	National	
x	x	x	x	x	x	Superset IBM AT compatible CPU card designed for use in a passive backplane.	CAT386	Comark	25
	x					Available in CMOS and Military versions	8800	Systek	
	x					SBX multimodule connector, interrupt controller, 3 16-bit counter/timers	8810	Systek	
x	x	x	x	x	x	Memory management unit, byte parity generation and checking for RAM, dual port RAM, programmable VMEbus base address for RAM.	MK75602	Thomson	
x	x	x	x	x	x	R5232C I/O, 8 bit switch input register, two timer/counters, self-test LED.	VME-SBC	Thomson	
x	x			x	x	Includes on-board Monitor, programmable real-time clock, 24-bit timer	44-201	Anasco	30
x	x			x	x	Includes on-board Monitor, programmable real-time clock, 24-bit timer	44-202	Anasco	
x	x					Includes on-board Monitor, on-board FD controller, dual-ported RAM, 16KB SRAM, RTC, 24-bit timer	44-203	Anasco	
x	x					Includes on-board Monitor, on-board FD controller, dual-ported RAM, 16KB SRAM, RTC, 24-bit timer	44-204	Anasco	
	x					Available in CMOS with NEC Floating point processor	8887	Systek	
x	x		x	x		Similar to LP-12 but omits on-board memory. Addresses 32K words of external memory.	LP12P	ICC	35
x	x		x	x		CMOS. Two-latched 12-bit ports and two 4-bit ports.	LP12	ICC	
x	x	x	x	x	x	Keyboard, 2 4-digit LEDs on card.	InterceptJr	GE/Intersil	
	x	x	x	x		A/D parallel port board option	TE1	Trimarchi	
x	x	x	x	x	x	Development board. EPROM programmer, Wire-Wrap area.	SBS100	SingleBoard	
x	x						FX97	AllenSys	
x	x	x	x	x		IBM PC/AT compatible.	MicroAT II	Faraday	
x	x	x	x		x	All CMOS, High Reliability, Low Power	CIM1605	ElecConServ	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16	16	V50	6.29	G-96	5, $\pm$ 12	1	16	1.0	16.8	16/64	0/512	x
16	8-32	80188	8	IBM	5	2	8	38.4	192/1 MB	128/1 MB	64/1 MB	x
16	16	NC4016	6	IBM PC	5	0-10	21	500	160	160		x
16	16	V40	8	IBM PC	5, $\pm$ 12	1		56	640	640		x
16	16	Z80B	4	IBMPc	5	1	4	9.6		2	8	x
16	16-64	80286	6/8	IBMPc	5	-	-	-	16 MB	256K/1 MB	16/64	x
16	Var.	8088		IBMPcbus	5	2		38.4	256	512/768		x
16	16	V50	8	IEEE-488	5				128		16	x
16	64	68008	8	IIOC	5	2	4	19.2	1MB	32	256	x
16	32	68000	12	LSI-11	5, $\pm$ 12	2		19.2	4MB	4MB		x
16	32	68010	10	LSI-11	5, $\pm$ 12	2		19.2	4MB	4MB		x
16	16-32	Custom	4	Maxi-bus	5, $\pm$ 12		32		128	2/6	0/6	x
16	16	F9450	20	Multibus	5, = 12	2		19.2	2MB	64	16/32	
16	16	F9445	16/20	Multibus		2	32		64	8	0/32	
16	16	MIL-STD-1750A	10MHE/40	Multibus	5, $\pm$ 12	2	1	9600	128	2000	128	x
16	16	MKS16	10	Multibus	5	1		19.2	128	2Mb	32	x
16	16	MKS16	10	Multibus	5	1	0	19.2	128	2Mb	2Mb	x
16	16	M68010C	10/12.5	Multibus	5, $\pm$ 12	2	8/16,20	38.4	16MB	1M/16M	128/128	x
16	16	M68010C	10/12.5	Multibus	5, $\pm$ 12	4	8/16	38.4	16MB	1M/16M	128/128	x
16	24	NS16032	10	Multibus		1	24		16000	32/128	1/8	
16	16	Z8001	4/10	Multibus	5, $\pm$ 12	2	40	1000	8MB	512/560	0/128	
16	16	Z8002	4/10	Multibus	5, $\pm$ 12	2	40	1000	1MB	512/560	0/128	
16	8-48	8086	5/8	Multibus	5, $\pm$ 12	1	24	9.6	1 MB	8/16	0/512	x
16	16-64	68000	8/10	Multibus	5, $\pm$ 12	4	8	19.2	16MB	0.256/16	0/64	x
16	16-80	68000	10	Multibus		2	32		16Mb	32/128	0/92	
16	8-32	80C86	5/8	Multibus	5, $\pm$ 12	1	24	19.6	1MB	16/64	256	
16	8-32	80C86	5/8	Multibus	5, $\pm$ 12	1	24	19.2	1MB	32/52	0/256	x
16	16-24	80186	8	Multibus	5	1	24	9.6	1Mb	128/512	0/128	x
16	16-64	80286	6	Multibus	$\pm$ 5, $\pm$ 12	3	16	1 MB	16 MB	1MB/16MB	96/384	x
16	8-48	8080A	5	Multibus		1			1000		0/32	
16	16	8085	10	Multibus	5,12							x
16	16	8085	10	Multibus	5,12							x
16	16	8085	10	Multibus	5,12							x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Hardware Support	Comments	Model	Source	Line
Assembler	Debug/Monitor	Editor	High Level Language	Operating System						
x	x	x	x	x	x		Low power, sockets for 16-channel 12-bit A/D converter	7610	Sensoray	5
x	x	x	x	x			Complete development system including EPROM programmer. Boots MS-DOS, CP/M-86 or stand-alone operating system. High-level language in ROM.	OEM188	Vesta	
x	x	x	x	x	x		Includes Novix Express Operating/Development System.	NB4100	Novix	
x	x			x	x			CPS-PC	InterconMicro	
x	x	x	x	x	x		MS-DOS, Math co-processor, firmware library, four sets of 24-bit up/down counters. Output to Auto CAD.	PC-PRO	Kern	
x	x	x	x	x	x		IBM PC bus board with real time clock and math coprocessor	ATCARD	Sigma Info	10
x	x	x	x	x	x		IBM add-on, each card allows one standard ANSI terminal to become another user of the host machine	PC-SLAVE	AdvDigital	
							Intelligent, programmable IEEE-488 interface for AT&T 3B2 computer.	GPIB3B2	NationalInst	
x	x			x			3 levels of interrupt, Bus Request and Bus Grant lines connected to the bus.	MPM68008	PEP-Modular	
x	x	x	x	x	x		Also available as complete system.	IS68K	IntSolutions	
x	x	x	x	x	x		Also available as complete system.	IS6810	IntSolutions	15
x	x	x	x	x	x		Floating point option, real-time clock, 8 channels of I/O from on-board I/O distributor. Intelligent cable interfaces, Pascal.	NM4/10	CompAuto	
x	x		x	x				SBC50	Fairchild	
x	x		x	x			Prototyping evaluation and programming board, on-board EPROM programmer, $\pm 12V$ supply used for P-S-232C operation only, 25V supply for EPROM programming only.	PEP45	Fairchild	
x	x	x	x	x	x		Single board CMOS implementation of MIL-STD-1750A plus options.	MKS1750/S0	Mikros	
x	x			x	x		Two-card implementation of the USAF MIL-STD-1750A ISA.	MKS1750/MO	Mikros	20
x	x			x	x		Two-card implementation of USAF MIL-STD-1750A ISA.	MKS1750/MO	Mikros	
x	x	x	x	x	x		Single Cycle DMA 68450 on QIC-02/Centronics, and iSBX interface, 1Mb on Card, Multimaster 2 16-bit iSBX, high level software tools.	HK68/ME	Heurikon	
x	x	x	x	x	x		SCSI ANSI X3T9.2 Compatible interface, Single cycle DMA and 68450 to QIC-02/Centronics, iSBX ad SCSI interfaces, MMU 68451 Multimaster, 2 16 bit iSBX, 1 iLBX, FPP 68881, 1 MB on card, Unix Sys V. High level software tools supported by Unix to real-time links.	HK68/M10	Heurikon	
x	x	x	x	x	x			DB16000	National	
x	x	x	x	x	x		One SBX connector, paged MMU, CP/M-8000.	MBX8001	SingleBoard	25
x	x	x	x	x	x		One SBX connector, paged MMU, CP/M-8000.	MBX8002	SingleBoard	
x	x	x	x	x	x		Two programmable timers, nine-level vectored priority interrupts; two iSBXconnectros; optional iSBC337A 8087 math coprocessor.	iSBC86/05A	Intel	
x	x	x	x	x	x		On card 4 channel DMA hard disk and streaming tape interface, BYTE-swap buffer, twin expansion connectors, and memory management unit	HK68A	Heurikon	
x	x	x	x	x	x		ROM, RAM, on-board I/O and off-board addresses user defineable. Contains 3 16-bit timers and 7 levels of vectored interrupts.	OB68K1A-512	Omnibyte	
					x		CMOS, low-power alternative to the 86/05, battery backed-up RAM	CBC86C/05	DiversTech	30
					x		CMOS 86/14, battery back-up RAM.	CBC86C/14	DiversTech	
x		x	x	x	x			MSC8186	MonSys	
x	x	x	x	x	x		Distributed processing, allows ETHERNET network and I/O traffic to be processed without burdening the UNIX environment	DPX86/ME	LitMach	
x	x	x	x	x	x		For severe environment: operating temperature 55° to 85°C vibration 5g 5 Hz to 1kHz, meets MIL-E5400, 16400, and 4158.	SECS86/05	Titan/SESCO	
	x	x			x		Single-board controller for up to two 5-1/4 inch ST506 Winchester drives and two SA400-type 5-1/4 inch floppy drives.	MC5214	Qualogy	
	x	x			x		Single-board controller for up to two 5-1/4 inch ST506 Winchester drives, two SA400-type 5-1/4 inch floppy drives, and one QIC-02 1/4 inch cartridge tape drives.	MC5217B	Qualogy	
	x	x			x		Single-board controller for up to two 5-1/4 inch ESDI Winchester drives, two SA400-type 5-1/4 inch floppy drives, and one QIC-02 1/4 inch cartridge tape drive.	MC5317	Qualogy	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16	16	8085	10	Multibus	5,12							x
16	8-40	8086	5	Multibus		2			1000		0/32	
16	16-64	8086	5/8	Multibus	5, $\pm$ 12	1			1Mb	0/4	0/128	
16	16-64	8086	5/8	Multibus	5, $\pm$ 12	1	24	9.6	1 MB	128/128	0/128	
16	16	8086	5/10	Multibus	5, $\pm$ 12	3	24	880	1Mb	0/8	0/24	x
16	8-32	8086	5/10	Multibus	5, $\pm$ 12	3	24	880	1Mb	0/48	0/192	x
16	8-32	8086	5/10	Multibus	5, $\pm$ 12	3	24	880	1MB	0/8	0/24	x
16	8-48	8086	5/10	Multibus	5, $\pm$ 12	1	24	38.4	1MB	512	128/512	x
16	8-32	8086	5/10	Multibus	5, $\pm$ 12	1	24	38.4	1MB	32/128	0/32	x
16	8-80	8086	5/10	Multibus	5, $\pm$ 12	1	8	19.2	1MB	0/128	0/128	
16	20	8086	5/10	Multibus	5, $\pm$ 12	2	24	38.4	1000	8/16	0/64	x
16	16-64	8086	8	Multibus	5, $\pm$ 12	8/16	16	56	16 MB	4/512	256/256	x
16	8-80	8086/8087	5/10	Multibus	5, $\pm$ 12	1	96	19.2	1 MB	0/1 MB	0/1 MB	
16	20	8086-2	5/8	Multibus	5, $\pm$ 12	1	24	38.4	1000	32/64	0/128	x
16	20	8086-2	5/8	Multibus	5, $\pm$ 12	1	24	38.4	1000	128/256	0/128	x
16	8,16	8086	5/8	Multibus I	5	1	24	Prog.	1 MB			x
16	8,16	8086	5/8	Multibus I	5	1	24	Prog.	1 MB			x
16	16	68000/010	10/12.5	Multibus I	12	2	8	38.4		1 MB	128	x
16	8-32	80186	6	Multibus I	5	10		Prog.		64	64/128	
16	8-32	80186	6/8	Multibus I	5	2		Prog.	16 MB	64	64/128	x
16	8-32	80286	6/8	Multibus I	5	2	1	Prog.	16 MB			x
16	8-32	80286	6/8	Multibus I	5	2	1	Prog.	16 MB			x
16	16	29116	8	Multibus II	5, $\pm$ 12	2		1M	64	64	2K	
16	16	34010	40/50	Multibus II	5, $\pm$ 12	1		19.2	128MB	512/2.2MB	256	x
16	16	80186	8	Multibus II	5, $\pm$ 12	8		76.8	1 MB	512	64/192	x
16	16	80186	8	Multibus II	5, $\pm$ 12				1 MB	512/2 MB	64/64	x
16	16	80186	8	Multibus II	5, $\pm$ 12	2	8	38.4	1 MB	512	64/64	x
16	16	80186	8	Multibus II	5, $\pm$ 12				1 MB	512	64/64	x
16	16	80186	8	Multibus II	5, $\pm$ 12	3	16	9.6	1.2MB	1MB/1MB	0/256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	1		19.2	4GB	512	128	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	1		19.2	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	1	48	19.2	4GB	512	256	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support											
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support						
						Comments	Model	Source			Line
	x	x			x	Single-board controller for up to two 5-1/4 inch ST506 Winchester drives, two SA850-type 8 inch floppy drives, MC-6217B and one QIC-02 1/4 inch cartridge tape drive.	MC6217B	Qualogy			
				x		Two programmable timers, nine level vectored priority interrupts.	SECS80/86	Titan/SESCO			
x	x	x	x	x	x	Optional 8087 floating-point processor. Optional memory management module.	DBC86	Microbar			
	x				x	Optional 8087 FPU, MMU, No wait states, Intel S.W. compatible	GPC86	Microbar			
x	x	x	x	x	x	Three timers, interrupt controller, real-time clock. Stand-alone computer, typically used for real-time control or in a system.	DCS/86/16	DistComp			5
x	x	x	x	x	x	Same as above plus a watchdog timer, 2 iSBX connectors, 10 year battery backup RAM, on board socket for 8087.	DCSICB/86	DistComp			
x	x	x	x	x	x	Three timers, interrupt controller, real-time clock. The DCS 86/16 is usable as a stand-alone computer, typically for real-time control, or in a system.	DCS86/16	DistComp			
x	x	x	x	x	x	Two programmable timers, nine-level vectored interrupts, optional 8087 co-processor.	MBC8b/512B	Matrox			
x	x	x	x	x	x	Two programmable timers, programmable interrupt controller, ROM/PROM expandable to 32K bytes on board.	MBC86/12A	Matrox			
	x	x		x	x	Numeric coprocessor, 16-bit timer, interrupt control, real-time clock. Augat Holtite zero-profile sockets. Also available in CMOS version.	86/50A	VisionsUnlim			10
x	x	x	x		x		ZX86	Zendex			
	x				x	9600 baud, full duplex all 16 channels 100% loaded. On-board firmware supports UNIX terminal I/O.	COM16	Microbar			
						All CMOS except 8087, 3 Farad capacitor backup for memory array	86/500A	VisionsUnlim			
x	x	x	x	x	x	Two programmable 16-Bit timers, 9 levels of direct vectored interrupt with support for bus vectored operation, two iSBX connectors, optional iSBC337A 8087 math coprocessor module.	iSBC86/14	Intel			
x	x	x	x	x	x	Two programmable 16-Bit timers, 9 levels of direct vectored interrupt with support for bus vectored operation, two iSBX connectors, optional iSBC337A 8087 math coprocessor module.	iSBC86/30	Intel			15
			x	x	x		SECS86/10	Titan/SESCO			
			x	x	x	Includes 8087 Numeric Coprocessor	SECS86/20	Titan/SESCO			
	x		x	x	x	Optional 68881 FPU.	HK68/VF	Heurikon			
				x	x	10-channel advanced communications computer	SECS186/48	Titan/SESCO			
			x	x	x	Three programmable 16-bit timers (binary or BCD)	SECS186010	Titan/SESCO			20
			x	x	x		SECS286/010	Titan/SESCO			
			x	x	x	Includes 80287 Numeric Coprocessor	SECS286/020	Titan/SESCO			
x				x		Multibus II to MIL-STD-1553 interface. Central computer and remote terminal simulation, 1553 bus tracer and analyzer	MIBII 1553	MicroInds			
	x				x	Video graphics board with up to 1024x8 display, 24-Bit color palette	MIBII 186/179	MicroInds			
x			x	x	x	Eight channel serial communications controller, optional asynchronous., X.25 protocol, two SBX connectors.	CD22/3800	CentData			25
	x		x	x	x	SCSI and floppy controller board. Supports SCSI rates up to 4M/sec.	CD22/4500	CentData			
	x		x	x	x	80186 single board computer.	CD22/6400	CentData			
	x		x	x	x	Intelligent prototyping board. Provides control circuitry, memory, and processor necessary to create powerful custom I/O board.	CD22/6410	CentData			
	x					Built-in self test. Two serial ports RS-485, SCSI and Centronics interfaces, OME Interface.i	MIBII 186/101	MicroInds			
	x				x	Multibus II interface board, general purpose extension of local bus, two iSBX connectors	MIBII 186/105	MicroInds			30
	x				x	Universal prototype board with two iSBX connectors	MIBII 186/110	MicroInds			
	x				x	Digital I/O board with two iSBX connectors. Supports message passing and Interconnect space	MIBII 186/111	MicroInds			

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16	8-32	80186	8	Multibus II	5, $\pm$ 12	1		19.2	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	3	24	19.2	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	1		19.2	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	1		19.2	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	5		19.2	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	17		19.2	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	2		62.5	4GB	512	256	x
16	8-32	80186	8	Multibus II	5, $\pm$ 12	1		19.2	4GB	512/512	256	x
16	16	9440	12	NOVA		2	8		32	32	4	
16	16	TMS320	6.6/20.5	Parallel	5, $\pm$ 12	3	0	9.6	8	0		x
16	16	TMS320	6.6/40	Parallel	5	2	0	9.6	16	16	0	x
16	16	TMS320	6.6/40	Parallel	5	0	0	0	48	48	0	x
16	16	80286	10	PC/AT	5, $\pm$ 12	1	12	56	16 MB	1 MB	512	x
16	16	80286	6/8	PC/AT bus	5, $\pm$ 12				16MB	512/1MB	256	x
16	16	80286	8/10	PC/AT bus	5, $\pm$ 12				16MB	1MB	256	x
16	8/16	80186	8	PC/AT/XT	5,12	0	0	10	8	256	16	
16	16	TMS320C25	40	PC bus	5	2	0	5	256	32/256	16/128	
16	16	TMS32020	20	PC bus	5	0	0		32	32/256		x
16	16	TMS32020	20	PC bus	5	2	0	2.5	256	32/256	16/128	
16	16	NC4016	8	Proprietary	5					56		x
16	16	TMS9900	3	Proprietary	5, $\pm$ 12	1	16	19.2	64K	2/4	2/8	x
16	16	TMS9900	3	Proprietary	5, $\pm$ 12	1	16	19.2	64K	2/4	2/8	x
16	16	Z8001	4	Proprietary	5	2	32		16	16/16	4/4	
16	16	Z8002	4	Proprietary	5	2	32		16	16/16	4/4	
16	16	80186	8/6	Proprietary	5				68	4	64	
16	116	80186	8/6	Proprietary	5		56		68	4	64	
16	16	80186	10/6	Proprietary	5, $\pm$ 12	2	8	38.2	320	256	64	x
16	20	8086	2.5/5	Proprietary	5	1	48	4.8	1000	2/4	8	x
16	16	9440	8/12	Proprietary		1	0		32	4	2	
16	16	Dual 2901	10	Q-BUS	5	1 diag. port		9600		1M Cache		x
16	16	68000	10	Q-Bus	5	6	0	64		512	128	x
16	16	2901	12	Q-BUS	5,12							x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support					Hardware Support	Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System					
	X				X	Enhanced digital I/O board, hammer-driver outputs, loop-back capability, two iSBX connectors	MIBII 186/112	MicroInds	5
	X				X	Intelligent I/O board with two iSBX connectors. Supports message passing and interconnect space	MIBII 186/130	MicroInds	
	X				X	Analog I/O board, 16 Differential/32 Single-ended inputs, 12-bit A/D, two iSBX connectors	MIBII 186/140	MicroInds	
	X				X	Analog output board, 16 analog outputs, current or voltage, two 12-bit DACs, two iSBX connectors	MIBII 186/141	MicroInds	
	X				X	Serial I/O board, 4 independent RS-232C or RS-422A/449 sync/asyn, two iSBX connectors	MIBII 186/150	MicroInds	
	X				X	16 channel serial I/O board, 16 independent RS-232C asyn channels, two iSBX connectors	MIBII 186/151	MicroInds	10
	X				X	BitBus board. 8044 BitBus interface, two iSBX connectors	MIBII 186/154	MicroInds	
	X				X	Video graphics board, up to 1024x768x4 display, 82720 GDC, two iSBX connectors	MIBII 186/178	MicroInds	
X	X	X	X	X	X	Compatible with industry standard 15'' x 15'' I/O controllers. Up to 8K bytes of program autoload PROMS. Memory control and parity logic.	GLOW16	Fairchild	
X	X		X	X	X	Realtime in-circuit emulation.	RTC/EVM320A-03 TI		
X	X	X		X	X	Realtime in-circuit emulation, for use with second generation TMS320	RTC/EVM320C-06 TI		15
X	X			X	X	PC form factor plug-in board, software support access, realtime in-circuit emulation.	TMDS3268821TI		
X	X	X	X	X	X	80287 coprocessor socket, P2 implemented P2/AT bus.	VME0286AT	LogicalDes	
X	X	X	X	X	X	PC/AT compatible motherboard. 12 slots, BIOS, DOS 3.1	3170	IndTech	
X	X	X	X	X	X	PC/AT compatible motherboard. 12 slots, BIOS, DOS 3.1, zero wait-state operation	3290	IndTech	
	X			X	X	Intelligent 802.3 Ethernet board.	SPC Link2	Intel	20
X	X					PC/XT/AT Plug-in Board with Single 16-bit A/D, D/A at 50 kHz Throughput.	TMS320C25	Pacific	
X	X					PC/XT/AT Plug-in Board with Dual 16-bit A/D, D/A at 50 kHz Throughput.	DSP16	Pacific	
X	X					PC/XT/AT Plug-in Board with Single 16-bit A/D, D/A at 50 kHz Throughput.	TMS32020	Pacific	
X	X	X	X	X	X	Uses polyFORTH Operating System/Novix Express O/S	NB4000	Novix	
X	X	X	X	X	X	Two interval timers.	TM990/ 100MB	TI	25
X	X	X	X	X	X	Three interval timers.	TM990/ 101MB	TI	
X	X	X	X	X	X	Development module for evaluation and debugging of Z8000-based systems.	Z8001DM	Zilog (3418)	
X	X	X	X	X	X	See above.	Z8002DM	Zilog (3418)	
						Multi-axis control board, 4-axis servo motion control. Used in multiprocessor system.	MAC	Slicer	
						Programmable interface controller for machine tool or process control. Used in multiprocessor system.	PIC	Slicer	30
X	X	X	X	X	X	SASI port, floppy disk controller, expansion boards available	Slicer	Slicer	
X	X	X	X	X	X	Buil-in display and keyboard, designed for 8086-based design breadboarding and instruction.	SDK86	Intel	
X	X		X	X		Nova instruction set, PROM resident entry and debugging program. Up to 4 I/O controller boards memory expansion to 64K bytes.	SPARK-16	Fairchild	
						Controller for 5-1/4 inch SA450-compatible floppy disk drive, on-board bootstrap, RX02 emulation, not RX50-compatible.	D4120	Qualogy	
	X		X			High-speed serial communication processor for MicroVAX systems. Designed for gateway (X.25, ISDN) and data acquisition applications.	QCOMM/6	CompModules	30
	X	X		X	X	Controller for AC 8 inch floppy disk SA800 or SA850-compatible, on-board bootstrap, RX02 emulation.	D4140-04	Qualogy	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16	16	2901	12	Q-BUS	5,12							x
16	16	65C802	20	Q-BUS	5	1 maint. port		9600		1M Cache		x
16	16	65C802	20	Q-BUS	5	1 maint. port		9600		1M Cache		x
16	32	32016	10	Qbus		8			4MB	4MB		x
16	16	V40	8	S-100	8,±16	3		56	768	768		x
16	16	8086	8	S-100	8,±16	4		1MB	256	256		
16	16	80186	8	S-100	8,±16	2	20	900	4MB	1MB	4/8	x
16	32	68000	10	S-100					16		8	
16	Var.	80186	8	S-100	5	4	16	19.2	256	1MB	32	x
16	32	8085A	5,±12	S-100		4	0	38.4				x
16	8-80	8086/87	5/8	S-100	8,±16	2	16	19.2	1MB	128/512	4/64	x
16	16	NC4016	7	SBC	5	1	16	38.4	128	8/32	8/32	
16	16-32	Custom	4	Scout-bus	5		16/32		128	0	0	x
16	16	80186	8	SCSI	5	2	8	38.4	512	128-512	16-128	x
16	16	80186	8	SCSI	5,±12	2	33	115.2	1Mb	512	16/64	x
16	16	80186	6/8	Slicer	5,±12	2	SASI	38.4	100	256/512	8/64	x
16	8,16,32	V50	5/8	STD	5	1	24	38.4	1 MB	0/512	0/512	x
16	8,16,32	V50	5/8	STD	5	1	24	38.4	1 MB	0/512	0/512	x
16	16	80186	8	STD	5,12	1	16	19.2	1000	128/512	16/64	x
16	16	8088	8	STD	5,±12	2		19.2	1MB	16		x
16	16	NC4016	6	STDbus	5	1	16	38.4	1 MB	33/65	16/16	x
16	16	68000	4	STDbus	5				16 MB	0/0	0/4	x
16	16	68008	8	STDbus	5,±12	2	16	38.4	1 MB	0/64	32/128	x
16	16-24	80186	5	STDbus	5,±12	2		56	16MB	512	0/256	x
16	16-24	80186	8	STDbus	5,±12	2	0	56	16MB	512	0/256	x
16	16	80188	8	STDbus	5,±12	2	8	56	1 MB	256/256	16/128	x
16	16	8086	4/10	S100	8				1 MB		8/16	x
16	16	80186	10	S100	8,±16	2	16	19.2	1 MB	1 MB	8/64	x
16	16	80286	6/8	S100	8				16 MB		8/64	
16	16	80186	8	S100	8	64	32	19.2	64	1Mb	64	x
16	16-64	80186	8	S100	8,±16	2	16	9.6	1Mb	256	8/64	x
16	16	TMS9900	3	TM990	5,±12	1	16	19.2	64K	0/128	4/16	x
16	32	68000	2	VERSAbus		2	60		16000	16	8/64	
16	16	68000	8	VERSAbus	5,±12	2		19.2	16MB	32/128	0/64	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support				
	x	x		x	x	Controller for DC 8 inch floppy disk Y-E Data YD-180-compatible (SA850-type interface) on-board bootstrap, RX02 emulation.	D4140-05	Qualogy	5
	x			x	x	Controller for up to four ESDI 5-1/4 inch Winchester drives, 1MB cache memory, on-board diagnostics, block mode DMA, ECC, seek ordering.	QE2	Qualogy	
	x			x	x	Controller for up to two SMD 10-1/2 inch disk drives, 1MB cache memory field-loadable microcode, 48-bit ECC, dual-wide controller, LSI-11 and MicroVAX compatible.	QS4	Qualogy	
x	x	x	x	x	x	Available as single-board computer or fully configured system	PYTHON/JR	GENROCO	
x	x			x	x		CPS-MS	InterconMicro	
x	x			x	x		CPS216	InterconMicro	
x	x			x	x		CPZ186	InterconMicro	
						CPU board with 68451 Memory Management Unit.	CPU68000ML10 DUAL		10
x	x	x	x	x	x	Dual-port memory, user-processor slave, 8087 coprocessor available	SUPER-SLAVE AdvDigital 16		
						Intelligent 4-port serial I/O module with DMA transfers for output.	SIO4-DMA DUAL		
x	x	x		x	x	Optional CPU, memory size, I/O configuration	SBC86/87	Teletex	
x	x	x	x	x	x	Includes CM Forth Operating System.	NB4200	Novix	
x	x	x	x	x	x	Isolite auto self test, floating point option, real-time clock. Hardware multiplication and division.	NM4/04	CompAuto	
x	x	x	x	x	x	Mounts on 5- 1/4" floppy, SCSI bus interface, no wait states, boots PC-DOS, 7 watts	Little Board/ 186	Ampro	
x	x	x	x	x	x	Same size as 5 1/4 inch floppy drive. Mounts directly on it.	LittleBoard/ 186	Ampro	15
x	x	x	x	x	x	Floppy-disk controller, SASI port for hard disks.	SLAT256	Slicer	
x	x	x	x	x	x	Very low power, all CMOS, extended temperature (-40°C to +85°C) operation. RS-232/422/485 port. Real time clock and ISBX connector.	LPM-SBC50	WinSystems	
x	x	x	x	x	x	Four memory sockets, real time clock and watchdog timer. Three 16-bit counter/timers and SBX connector.	MCM-SBC50	WinSystems	
	x				x	Includes link to PC for software development.	8500	Cubit	
x	x		x	x		Optional 8087 numeric data processor or floating point co-processor, 8089 I/O processor.	10888	Enterprise	
x	x	x	x	x	x	Includes Novix Express Operating/Development System. Functional as Master or Slave.	NB4300	Novix	
	x		x	x	x	One 24-pin socket for 2Kx8 or 4Kx8 EPROMs, STD-Z80 compatible, PDOS operating system.	STD203	Micro-Link	20
	x		x	x	x	Three 16-bit Timer/Counter Channels, STD-Z80 compatible, PDOS operating system, IBM PC communication software.	STD202	Micro-Link	
x	x	x	x	x	x	NEC V50 (80186 compatible), 8080 emulation mode, battery backed RAM and real-time clock. AC/DC power fail protection, optional floating point coprocessor, 3 counter/timers	ZT8816	Ziatech	
x	x	x	x	x	x	NEC V50 (80186 compatible), 8080 emulation mode, battery-backed RAM and real-time clock. AC/DC power fail protection, optional floating point coprocessor, three counter timers	ZT8817	Ziatech	
	x		x	x	x	On-board interrupt controller, three counter/timers, RS-232 and RS-422 ports.	STD206	Micro-Link	
x	x	x	x	x	x	CD/M-86, MS-DOS and concurrent CP/M-86, also 8087 and 8089 CPU.	Lightning One	Lomas	
x	x	x	x	x	x	Includes CC-DOS, CPM-86 and MS DOS available, 8087 optional.	Thunder Plus	Lomas	
x	x	x	x	x	x	CP/M-86, MS-DOS and concurrent CP/M-86.	Lightning 286	Lomas	30
				x	x	Five- and 8-inch floppy disk controller, Math coprocessor, real-time clock, 256K or 1MB of RAM, up to 64K of ROM.	Super 186	AdvDigital	
x	x	x	x	x	x	Concurrent CP/M-86.	Thunder 186	Lomas	
x	x	x	x	x	x	Memory mapped address space to 1M bytes.	TM990/102	TI	
	x		x				VMC68K/15	National	
x	x	x	x	x		Shared RAM permits DMA operation with VERSAbus intelligent peripheral controller modules. Has local 8-bit I/O bus and three 16-bit timers.	M68KVM02	Motorola	

Bold face indicates additional data is provided on the page noted.



## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16	16	68000	8	VERSAbus	5, $\pm$ 12	2	40	9.6	16MB	32/64	0/64	x
16	16	68000	8	VME	5, $\pm$ 12	2	16	38.4	192	2/32	0/64	
16	16	68000	8	VME	5, $\pm$ 12	2	16	38.4	384	2/64	0/128	
16	16	68000	8	VME	5, $\pm$ 12	2	16	38.4	192	2/32	0/64	
16	16	68000	8	VME	5, $\pm$ 12	2	16	38.4	384	2/64	0/128	
16	32	68000	8/12.5	VME	5, $\pm$ 12	3	24	38.4	16MB	512	32/256	
16	16	68000	10	VME	5, $\pm$ 12	2	16	38.4	192	2/32	0/64	
16	16	68000	10	VME	5, $\pm$ 12	2	16	38.4	384	2/64	0/128	
16	16	68000	10	VME	5, $\pm$ 12	2	16	38.4	192	2/32	0/64	
16	16	68000	10	VME	5, $\pm$ 12	2	16	38.4	384	2/64	0/128	
16	32	68000	16.7	VME	5, $\pm$ 12	2	0	38.4	16 MB	128	32/256	x
16	16	68010	10	VME	5, $\pm$ 12	2	16	38.4	192	2/32	0/64	
16	16	68010	10	VME	5, $\pm$ 12	2	16	38.4	384	2/64	0/128	
16	16	68010	10	VME	5, $\pm$ 12	2	16	38.4	192	2/32	0/64	
16	16	68010	10	VME	5, $\pm$ 12	2	16	38.4	384	2/64	0/128	
16	16	68010	10	VME	5, $\pm$ 12	2	16	38.4	384	0/64	0/256	x
16	16	68010	10	VME	5, $\pm$ 12	2	16	38.4	384	0/64	0/256	x
16	32	68010	12.5	VME	5, $\pm$ 12	2	0	38.4	16MB	128	32/256	x
16	32	68010	12.5	VME	5, $\pm$ 12	3	24	38.4	16MB	512	32/256	
16	16	68010	12.5	VME	5, $\pm$ 12	2	16	38.4	384	0/64	0/256	x
16	32	68000	8	VME	5, $\pm$ 12	1	8	—	16MB			
16	32	68000	8	VME	5, $\pm$ 12	1	—	19.2	16MB	16	16	x
16	32	68010	8/10	VME	+ 5, $\pm$ 12	1	24	38.4	16Mb	1024	16/32	
16	32	68010	8/10	VME	5, $\pm$ 12	1	0	38.4	16Mc	1024	16	x
16	32	68010	10/12.5	VME	5, $\pm$ 12	1	16	38.4	16Mc	128	16/512	x
16	16	68000/010	10	VME bus	5, $\pm$ 12	2		38.4	16 MB	512/512	32/128	
16	16	68010	10	VME bus	5, $\pm$ 12	4		38.4	16 MB	512/576	32/128	
16	16	M68010C	10/12.5	VMEbus	5, $\pm$ 12	2	8	38.4	16MB	1M/16M	128/128	x
16	16	M68010C	10/12.5	VMEbus	5, $\pm$ 12	2		38.4	16MB	1M/16M	128/128	x
16	16	68000	8	VMEbus	5, $\pm$ 12	1		9.6	16 MB	0/64	0/384	
16	16	68000	8/10	VMEbus	5, $\pm$ 12	1		9.6	16MB	0/64	0/128	
16	16	68000	10	VMEbus	5, $\pm$ 12	2		38.4	16 MB	512	128	
16	16	68000	10	VMEbus	5, $\pm$ 12	4		38.4	16M	512	256	
16	16	68000	10	VMEbus	5, $\pm$ 12	2	0	38.4	16MB	0/64	0/256	x
16	16	68000	10	VMEbus	5, $\pm$ 12	2	0	38.4	16MB	0/64	0/256	x
16	16	68000	10	VMEbus	5, $\pm$ 12	1		9.6	16 MB	0/64	0/384	
16	16	68000	10	VMEbus	5, $\pm$ 12	1		9.6	16 MB	512/704	0/384	
16	16	68000	10	VMEbus	5, $\pm$ 12	1		9.6	16 MB	1 MB/1.2 MB	0/384	
16	32	68000	12.5	VMEbus	5	0-4	0-40	3M	16MB	512	0/256	x
16	16	68010	10	VMEbus	5	8	opt.	19.2	10MB	2MB	128	x
16	16	68010	10	VMEbus	5, $\pm$ 12	2	0	38.4	16MB	0/64	0/256	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support							Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System	Hardware Support					
x	x	x	x	x			Programmable timer/counter VERSA bus interface, system controller functions include bus arbitration, system interrupt processing, test signal, and self-test.	VERSAmodule	Motorola	5
							Includes system controller functions.	PG2004	MicroInds	
							Includes system controller functions.	PG2004/10	MicroInds	
							Includes system controller functions, 68451 MMU.	PG2005	MicroInds	
							Includes system controller functions, 68451 MMU.	PG2005/10	MicroInds	
x	x	x	x	x	x		68881 FPCP, counter/timer, real-time clock, forcebug monitor.	CPU6	Force	10
							Includes system controller functions.	PG2006	MicroInds	
							Includes system controller functions.	PG2006/10	MicroInds	
							Includes system controller functions, 68451 MMU.	PG2007	MicroInds	
							Includes system controller functions, 68451 MMU.	PG2007/10	MicroInds	
x	x	x	x	x	x		Zero wait-state SRAM, 68450 DMAC, floating point coprocessor.	CPU5A	Force	15
							Includes system controller functions.	PG2008	MicroInds	
							Includes system controller functions.	PG2008/10	MicroInds	
							Includes system controller functions, 68451 MMU.	PG2009	MicroInds	
							Includes system controller functions, 68451 MMU.	PG2009/10	MicroInds	
							2 JEDEC sockets for dual port memory VMX bus interface.	PG2030	MicroInds	20
							2 JEDEC sockets for dual-port memory, 68451 MMU, VMX bus interface.	PG2031	MicroInds	
x	x	x	x	x	x		Zero wait-state SRAM, 68450 DMAC, floating point coprocessor.	CPU5V	Force	
x	x	x	x	x	x		68881 FPCP, counter/timer, real-time clock, forcebug monitor.	CPU6V	Force	
							2 JEDEC sockets for dual-port memory, VMX bus interface.	PG2035	MicroInds	
					x		Controller, 1024 x 1024 Graphics display controller. 4 to 11 bits per pixel.	GDC1	Force	25
x	x				x		Controller, Intelligent SASI host adapter 68450 DMA controller.	SASI1	Force	
x	x	x	x	x	x		Dual Ported DRAM.	CPU2	Force	
x	x	x	x	x	x		68450 DMA, 68451 MMU for multi user applications	CPU3	Force	
x	x	x	x	x	x		Zero wait-state access to SRAM 6850 DMAC, 4 level arbiter.	CPU4	Force	
	x		x	x	x		3U single board computer, PDOS operating system, monitor/boot EPROM	VME211	Micro-Link	30
	x		x	x	x		Two counter/timers, real-time clock with battery back-up.	VME212	Micro-Link	
x	x	x	x	x	x		DMAC 68450, 2 iSBX connectors, OPT 68881, FPP, 1 MB on-board, Multimaster. High level software tools supported by UNIX to real-time links.	HK68/VE	Heurikon	
x	x	x	x	x	x		68451 MMU, 1 MB RAM on Card, 68881 FPP, RS-422 Opt. 68450 DMAC, iLBX, SCSI QIC.02, Multimaster, high level software tools supported by UNIX to real-time links.	HK68/V10	Heurikon	
							Motorola MVME 110-1 CPU Replacement Card.	TVME 1612-1	TLIndustries	
							Motorola MVME 110-1 compatible CPU card	TVME 1612	TLIndustries	35
	x		x	x			Optional 68010 processor. Dual-port RAM, zero-wait state memory, 16-bit counter/timer.	45148020L	Bicc-Vero	
	x		x	x			Optional 68010 processor. 68881 FPP, 68451 MMU, real-time clock, system controller, two 16-bit counter/timers.	45148024K	Bicc-Vero	
x	x	x	x	x	x		Single-Height CPU, System Controller, No-Wait States	MS-CPU00	Matrix	
x	x	x	x	x	x		Same as MS-CPU00 with Battery Back-up for SRAM Sockets and Power-Fail Protection.	MS-CPU00B	Matrix	
							Motorola MVME 110-1 CPU Replacement Card.	TVME 1612-2	TLIndustries	40
							Motorola MVME 110-1 CPU Replacement Card.	TVME 1613-1	TLIndustries	
							Motorola MVME 110-1 CPU Replacement Card.	TVME 1613-2	TLIndustries	
x	x	x	x	x	x		All I/O on daughter boards, Bus Interrupter, System Controller and DMA optional	OB68K/ VSBC1	Omnibyte	
x	x	x	x	x	x		HP412/ST506/ESDI/5.25 inch floppy disk controller included. Demand paged MMU, optional QIC-02 tape, Centronics printer port.	BASEboard	Interphase	
x	x	x	x	x	x		Single-Height CPU, No-Wait States.	MS-CPU10	Matrix	

Bold face indicates additional data is provided on the page noted.



## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	0	38.4	16MB	0/64	0/256	x
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16MB	512/4MB	0/256	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16 MB	512	0/256	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16 MB	512	0.256	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16 MB	1 MB	0/256	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16 MB	1 MB	0/256	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16 MB	2 MB	0/256	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16 MB	2 MB	0/256	
16	16	68010	10	VMEbus	5, $\pm$ 12	2	20	19.2	16 MB	4 MB	0/256	
16	16	68010	10	vmeBUS	5, $\pm$ 12	2	20	19.2	16 MB	4 MB	0/256	
16	16	68000	8	VMEbus	5, $\pm$ 12	8		1 MB	16 MB	48	16/64	x
16	16/32	68000	8	VMEbus	5, $\pm$ 12	2	16	19.2	16MB	256	64	
16	16	68000	8	VMEbus	5, $\pm$ 12	1		9.6	16MB	0/64K	0/128	x
16	8-32	68000	8	VMEbus	5, $\pm$ 12	2	16	38.4	16MB	8/0	0/48K	x
16	32	68000	8/10/12.5	VMEbus	5	2	60	19.2		2000	256	x
16	16	68000	8/12	VMEbus	5, $\pm$ 12	1	4	19.2	16MB	16/64	16/128	x
16	16	68000	8/12.5	VMEbus	5, $\pm$ 12	2	2	38.4	16 MB	128/512	0/128	
16	16	68000	10	VMEbus	5, $\pm$ 12	2	0	38.4	16 MB	512	0/128	
16		68000/010	8/10	VMEbus	5, $\pm$ 12	1	16	38.4		1000	64	
16		68000/010	10	VMEbus	5, $\pm$ 12	1	8/16	38.4		4000	128	
16		68000/010	10	VMEbus	5, $\pm$ 12	2		38.4		2000	256	x
16	16-32	68010	8/12	VMEbus	5, $\pm$ 12	2	8	207	16MB	128	128	x
16	16	68010	8/12.5	VMEbus	5, $\pm$ 12	2	2	38.4	16 MB	128/512	0/128	
16	32	68010	10	VMEbus	5	2		19.2		512/1 MB	128	x
16	16	68010	10	VMEbus	5, $\pm$ 12	2	0	38.4	16 MB	512	0/128	
16	16-80	68010	10/12.5	VMEbus	5, $\pm$ 12	2	16	19.2	16MB	512/1 MB	64	
16	8-40	80186	Multibus II	5	5	2	24	64	1 MB	512 KB	128 KB	x
16/32	16-48	Z8001/2	4-10	Multibus	5, $\pm$ 12	2	40	1000	8MB	32/128/512	128	
16/32	16-80	68000	4/8	Multibus	5, $\pm$ 12	2	24		16MB	0/4	0/32	
16/32	16-80	68000	10	Multibus		2	32	19.2	16M	128/0	0/192	
16/32	16	68000	10	Multibus	5	2	16	880	2 MB	128/256	32	
16/32	16-80	68000	10/12	Multibus	5, $\pm$ 12	2	iSBX		16Mb	128/256	0/128	
16/32	16-80	68000	10/12	Multibus	5	4	4	880	16 MB	1 MB/16 MB	32/256	
16/32	16-80	68000	10/12	Multibus	5	4	4	880	16 MB	1 MB/16 MB	32/256	
16/32	16-80	68000/010	10/12	Multibus	5, $\pm$ 12	2	16	880	16 MB	128/3 MB	0/256	x
16/32	16	68000/68010	8/12.5	Multibus	5, $\pm$ 12	4	0	1MB	16MB	256/2MB	0/256	
16/32	16	68000, 68010	10	Multibus	5	2	16	880	24MB	256/1MB	128	

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Hardware Support	Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System						
x	x	x	x	x	x		Same as MS-CPU10 with Battery Back-up for SRAM Sockets and Power-Fail Protection.	MS-CPU10B	Matrix	5
							Motorola MVME 117-3 compatible CPU card utilizing SMT	TVME 1611	TLIndustries	
							Motorola MVME Replacement Card for MVME 117-3 CPU, Utilizes SMT.	TVME 1611-1	TLIndustries	
							Motorola MVME117-3FP CPU Replacement Card, Utilizing SMT.	TVME 1611-2	TLIndustries	
							Motorola MVME 117-3 CPU Replacement Card with 1 MB RAM, Utilizing SMT.	TVME 1611-3	TLIndustries	
							Motorola MVME 117-3FP CPU Replacement Card with 1 MB RAM.	TVME 1611-4	TLIndustries	
							Motorola MVME 117-3 CPU Replacement Card with 2 MB RAM.	TVME 1611-5	TLIndustries	
							Motorola MVME 117-3FP CPU Replacement Card with 2 MB RAM.	TVME 1611-6	TLIndustries	
							Motorola MVME 117-3 CPU Replacement Card with 4 MB RAM.	TVME 1611-7	TLIndustries	
							Motorola MVME 117-3FP CPU Replacement Card with 4 MB RAM.	TVME 1611-8	TLIndustries	
x	x	x	x	x	x		Serial communications processor, system controller	48760G	Bicc-Vero	10
x	x	x	x	x			Single ported RAM. Flag register for multi-processing.	IoVME 101	IoInc	
				x	x		Supports I/O channel for large variety of peripheral and I/O functions.	MVME110	Motorola	
x	x		x	x			CPU module, optional memory management unit, programmable real-time clock, 7 levels of interrupt.	SMVME2000	Signetics	
								GMSV06	GenMicro	
x	x		x	x			Single height Eurocard format with programmable address modifiers, serial port can be RS-232, RS-422 or 20mA loop.	VMPM68KA	PEP-Modular	
x	x	x	x	x	x		CPU, system controller, optional 68451 MMU	48350J	Bicc-Vero	
x	x	x	x	x	x		CPU, system controller, no wait state memory	48010D	Bicc-Vero	
x		x	x	x	x		Floppy disk controller, programmable real-time clock with calendar, dual-port RAM.	PME 68-2	PlesseyMicro	
x		x	x	x	x		Floppy disk controller, real-time clock, 16K byte high-speed static RAM.	PME 68-12	PlesseyMicro	
x		x	x	x	x		Optional MC68881 math coprocessor, real-time clock, dual-port RAM.	PME 68-14	PlesseyMicro	20
x	x		x	x			Includes 128K of EPROM, address modifiers are fully programmable, serial port can be RS-232, RS-422, RS-485 or 20mA current loop.	VMPM68KB	PEP-Modular	
x	x	x	x	x	x		CPU, system controller, optional 68451 MMU	48354H	Bicc-Vero	
x	x	x	x	x	x		Up to 2 optional MMUs, up to 8 MB of DRAM	A68VME	Alcyon	
x	x	x	x	x	x		CPU, system controller, no wait state memory	48014C	Bicc-Vero	
x	x	x	x	x	x		No wait state dynamic RAM, system controller, with single level arbiter, 2-Byte-wide sockets, optional floating point processor.	IV1602	Ironics	
x	x	x	x	x	x		Includes 8087 socket; iSBX connector.	iSBC186/100	Intel	
x	x	x	x	x	x		SBX connector, static RAM capability, EEPROM, CP/M-8000 available, SASI interface, six 16-bit counter-timers	MBX8000	SingleBoard	
x	x	x	x	x	x		Optional two-level page-oriented memory mapping and protection. Dual bus architecture.	DBC68K	Microbar	
x	x	x	x	x	x			OB68K1A-128	Omnibyte	
	x	x	x	x	x		SUN compatible, no-wait state MMU, master only.	PM68K	PacificM	30
x	x	x	x	x	x		Optional two-level page-oriented memory mapping and protection. Dual bus architecture.	DBC68K2	Microbar	
x	x	x	x	x	x		1.5 MB/s SCSI controller, real-time clock, 2-level demand-paged MMU, optional 68020 and 68881 daughter board, 16 MB dual-port no-wait-state RAM.	SM68F	Synergy	
x	x	x	x	x	x		1.5 MB/s SCSI controller, real-time clock, 2-level demand-paged MMU, optional 68020 and 68881 daughter board, up to 16 MB no-wait-state RAM, :SBX connector, optional parallel port.	SM68M	Synergy	
x	x	x	x	x	x		12 MHz CPU with up to 3MB no-wait DRAM	GPC68K	Microbar	
x	x							OB68K/ MSBC1	Omnibyte	
x	x	x	x	x	x		Has 68000 or 68010 CPU. No wait state 8MB context MMU with dual ported RAM, 7 Mailbox interrupts.	PM68D	PacificM	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16/32	16	68000, 68010	10/12.5	Multibus	5	2	16	880	16 MB	1 MB/4 MB	64K/1 MB	x
16/32	16-48	Z8001	10	Multibus I	5				8 MB		0/32	
16/32	16-48	Z8002	4	Multibus I	5, $\pm$ 12	2	24	64	512	32	0/8	
16/32	16-48	Z8002	4	Multibus I	5, $\pm$ 12	2	24	64	1 MB	128	0/16	
16/32	16	68000, 68010	10	Multibus I	5, $\pm$ 12	2	24	4M	16MB	128/512	-/256	x
16/32	16	68000, 68010	10	Multibus I	5, $\pm$ 12	4		800	16MB	128/512	-/256	x
16/32	16	68000, 68010	10	Multibus I	5, $\pm$ 12	8		800	16MB	128/512	-/256	x
16/32	16	68000, 68010	10	Multibus I	5, $\pm$ 12	2	24	4M	16MB	128/512	-/256	x
16/32	16	68000, 68010	10	Multibus I	5, $\pm$ 12	2		880	16MB	512/8MB	-/64	
16/32	16	68000, 68010	10	Multibus I	5	2	24	880	16MB	128/1MB	-/128	
16/32	16	68000, 68010	15.5	Multibus I	5, $\pm$ 12	2	24	800	16MB	128/4MB	-/256	x
16/32	32	68020	12.5/16.6/20	Multibus I	5, $\pm$ 12	2	24	64	24MB	1MB/8MB	-/256	
16/32	16/32	68020	12.5/16.67	Multibus II	5, $\pm$ 12	2	16	38.4	4.2 GB	1MB/4MB	256	x
16/32	32	68010	10	Q-bus	5,12				4Mb		0.5	x
16/32	16	68008	5.0688	STD	5	1		19.2	1Mb	2	8	
16/32	16	68010	12	STDbus	5				16MB	1MB/1MB	16/128	x
16/32	16	68000	12.5	VERSAbus	5	4		38.4	16Mb	0/16Mb	16	x
16/32	16	68000	20	VME bus	5	0				256	8	x
16/32	16	J11	15	VMEbus	5, $\pm$ 12	4	20	38.4	4000	64	256	
16/32	16	J11	15	VMEbus	5, $\pm$ 12	2		38.4	4MB	1MB		x
16/32	16	68000, 68010	10	VMEbus	5, $\pm$ 12	8		19.2	16MB	16/64	-/256	
16/32	16-80	68010	10/12.5	VMEbus	5, $\pm$ 12	2-4	16		16MB	1 MB	0/320	
16/32		68000	8/10	VMEbus	5, $\pm$ 12	3	24	19.2	16MB	512	16/128	
16/32	16	68000	12.5	VMEbus	5	4		38.4	16Mb	0/16Mb	16	x
16/32	16	68000/68010	8/12.5	VMEbus	5, $\pm$ 12	2	16	38.4	16MB	0/128	0/512	
16/32	16	68010	8/10	VMEbus	5, $\pm$ 12	1	8/16	38.4	16Mb	256/1Mb	16	
16/32	32	68010	10	VMEbus	5, $\pm$ 12	1			16MB	128		x
16/32	32	68010	10	VMEbus	5, $\pm$ 12	1			16MB	128		x
16/32	32	68010	10/2	VMEbus	5, $\pm$ 12	2	16		16MB	128/512		x
16/32	32	68010	10/2	VMEbus	5, $\pm$ 12	2	16		16MB	128/512		x
16/32	32	68010	10/2	VMEbus	5, $\pm$ 12	2	16		16MB	128/512		x
16/32	32	68010	10/2	VMEbus	5, $\pm$ 12	2	16		16MB	128/512		x
16/32	32	68010/20	12/16	VMEbus	5, $\pm$ 12	2		19.2	8/256MB			x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support					Hardware Support	Comments	Model	Source	Line
Assembler	Debug/Monitor	Editor	High Level Language	Operating System					
X	X	X	X	X	X	Two level memory management; no-wait states with on-board memory; iSBX interface and three 16-bit counter/timers.	M680R	PacificM	
X	X	X	X				MB1801	SingleBoard	
X	X	X	X				MB4116	SingleBoard	
X	X	X	X				MB4126	SingleBoard	
X	X	X	X	X	X	68450 DMA controller, two 68561s for asynchronous/synchronous communications to 4Mb/s	COM2	SBE	5
X	X	X	X	X	X	Two 68450 DMA controllers, two 8530 SCCs for async/sync communications to 800kb/s	COM4	SBE	
X	X	X	X	X	X	68450 DMA controller, four 8530 SCCs for async/sync communications to 800Kb/s	COM8	SBE	
X	X	X	X	X	X	68450 DMA controller, Signetics 68562 DUSCC chip for async/sync communications to 4Mb/s, AMD LANCE for 802.3 Ethernet support.	MLAN-E	SBE	
X	X	X	X	X	X	MMU board set, companion memory boards/private memory bus.	M68CPU	SBE	
X	X	X		X		Memory expansion module, triple 16-bit counter/timer, and two 8-bit iSBX connectors	M68K10	SBE	10
X	X	X	X	X	X	SBE Mailbox, 68450 DMA controller	MPU12	SBE	
X	X	X	X	X	X	Optional 68881 floating point coprocessor; optional memory management module	MPU20	SBE	
X	X	X	X	X	X	Used for Multitasking using Real-Time Operating Systems. Optional DMA, FPU, and MMU.	MT68020A	Microbar	
X	X	X	X	X	X	Runs AT&T UNIX System 5.2. (Add-on memory also available)	UNIVAX68010	Cambridge	
X	X					The 68008 is a 68000 with 8-bit wide path to the outside world. DMA can be provided off board. Up to 8K RAM on board. Serial lines are RS-232C buffered.	FX688	AllenSys	15
X	X	X	X	X	X	PDOS multi-user, multitasking disk operating system. Onboard 6840 internal timer.	CPU68K-1	GW-Three	
X	X	X	X	X	X	Supported by UNOS and VN/System V operating systems. Includes second 68000 for IOP.	CP32	CharlesRiver	
	X				X	SCSI high-speed dual ported intelligent controller. Synchronous or asynchronous, supports up to seven SCSI bus devices per port.	MCT6008	MiniCompTech	
					X	Instruction set compatible with DEC PDP-11, optional on-board lithium battery.	VME1120D	LogicalDes	
X	X	X	X	X	X	SCSI port, optional floating point co-processor, 0.5 or 1MB dual-ported no wait state RAM, bootstrap PROM	VME1130D	LogicalDes	20
X	X		X		X	Intelligent 8-channel communications board	VCOM8	SBE	
X	X	X	X	X	X	No wait-state dynamic RAM, up to 4 serial I/O parts, SASI/SCSI bus mass-storage interface, buffered parallel printer port, 3-channel programmable counter/timer.	IV1600	Ironics	
X	X	X	X	X	X	All Force CPU's function as slot 1 system control.	CPU1	Force	
X	X	X	X	X	X	Includes 4Kb cache, supported by UNOS and UN/System V.	VCP2000	CharlesRiver	
X	X						OB68K VME1-MDmnibyte		25
X	X	X	X	X	X	Disk Controller, Real-Time Clock with Battery, Virtual Memory and Multiprocessing Support.	PME68-2/102	PlesseyMicro	
	X		X	X	X	VME Module with 10 MHz 68010 MPU, 68451 MMU, 128 Kbytes of RAM, 4Kbytes of no wait state instruction cache	MVME120	Motorola	
	X		X	X	X	VME Module with 12.5 MHz 68010 MPU, 68451 MMU, 128 Kbytes of RAM, 4Kbytes of no wait state instruction cache	MVME122	Motorola	
X			X	X	X	VME module with 128 Kbytes of zero wait state DRAM, SCSI bus interface, battery backed time of day clock, 4 EPROM sockets, and 68881 floating point processor.	MVME117-1	Motorola	
X			X	X	X	VME module with 128 Kbytes of zero wait state DRAM, battery backed time of day clock, 4 EPROM sockets, and 68881 floating point processor.	MVME117-2	Motorola	
X			X	X	X	VME module with 512 Kbytes of zero wait state DRAM, SCSI bus interface, battery backed time of day clock, 4 EPROM sockets, and 68881 floating point processor.	MVME117-3	Motorola	
X			X	X	X	VME module with 512 Kbytes of zero wait state DRAM, SCSI bus interface, battery backed time of day clock, 4 EPROM sockets, and 68881 processor on board.	MVME117-3FP	Motorola	
X			X	X	X	VME module with 128 Kbytes of zero wait state DRAM, SCSI bus interface, battery backed time of day clock, 4 EPROM sockets, and 68881 floating point processor.	MVME117-4	Motorola	
X	X	X	X	X	X	Also available as complete system.	VME6810	IntSolutions	30

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

Data Word Size (bits)	Instruction Word Size (bits)	General				I/O			Memory			
		CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
16-8	16-8	8088	8	QBus	5	1		250	192/768	192/768		
16-8	16-80	8088	8	Unibus	5	3		250	256/768	256/1Mb		
16-32	16-80	68010	10/12.5	VME/VMX	5, $\pm$ 12	—			16 MB	512/1 MB		
32	N/A	TMS34010	50	IBM PC	5, $\pm$ 12	1				768	1	
32	32	80386	16/20	IBM PC	5				4 GB	1 MB/24 MB		x
32	32	NS32332	10/20	MaxiBus	5	4	1	19.2	14	1/14	128	x
32	32	NS32332	15	Multibus	5	2	40		4 GB	2 MB	256	
32	32	68020	16.67	Multibus	5, $\pm$ 12	2	16	880	32 MB	1 MB/32 MB	64/1 MB	x
32	32	68020	16.67	Multibus	5, $\pm$ 12	2	16	880	32 MB	1 MB/32 MB	64K/1 MB	
32	8-40	80386	16	Multibus	5	1		19.2	16 MB	1/16 MB	0/512	
32	8-40	80386	16	Multibus	5	1		19.2	16 MB	2/16 MB	0/512	
32	8-40	80386	16	Multibus	5	1		19.2	16 MB	4/16 MB	0/512	
32	8-40	80386	16	Multibus	5	1		19.2	16 MB	8/16 MB	0/512	
32	8-40	80386	20	Multibus	5	1		19.2	16 MB	1/16	0/512	
32	8-40	80386	20	Multibus	5	1		19.2	16 MB	2/16	0/512	
32	8-40	80386	20	Multibus	5	1		19.2	16 MB	4/16	0/512	
32	8-40	80386	20	Multibus	5	1		19.2	16 MB	8/16	0/512	
32	32	32032	10	Multibus	5, $\pm$ 12	2		38.4	128	8	512	x
32	32	32032	10	Multibus	5, $\pm$ 12	2		38.4	20MB	256/4MB	32/128	
32	32	68000	10	Multibus	5, $\pm$ 12	2			16MB	128/1MB		x
32	16-80	68020	12/16	Multibus	5, -12	4	4	880	4GB	1 MB/64 MB	32/256	
32	16-64	68020	12.5/16.7	Multibus	5, $\pm$ 12	2	16	880	32 MB	1MB/8MB	64/320	x
32	16-64	68020	12.5/16.7	Multibus	5, $\pm$ 12	2	16	880	4 GB	1MB/12MB	64/320	x
32	32	68020	16.7	Multibus	5, $\pm$ 12	2		880	256	8	768	x
32	32	MC68020	12.5	Multibus I	5, $\pm$ 12	5				1 MB	—/512	x
32	32	68020	12.5/25	Multibus I	12	2	8	62.4	4 GB	1 MB/4 MB	256	

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Hardware Support	Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System						
x	x	x	x	x	x	Allows DEC-LSI-11 and PDP-11 computers to execute PC-SOC or CP/M-86 programs from any terminal on the DEC system. Has an RS-232C compatible serial channel. Comes with a control program resident to the native DEC operating system.	QCP11 +	Logiccraft	5	
x	x	x	x	x	x	One, two or three 8088 microprocessors, each having from 256K to 768K RAM and an RS-232C compatible serial channel. Enables DEC PDP-11 and VAX computers access to PC-DOS and/or CP/M-86 Micro programs and DEC applications can run simultaneously.	HCP11	Logiccraft		
x	x	x	x	x	x	No wait-state dynamic RAM, dual-port static RAM. 2-Byte-wide sockets, interrupt handler, optional floating-point processor.	IV1601	Ironics		
x	x		x		x	Used for development and debugging of TMS34010 application programs	TMDS3411804420 TI			
x	x	x	x	x	x	Optional 80387 Floating Point Coprocessor. OS/386 operating system.	386 Humming Board AI Architects			
x	x	x	x	x	x	Integrated computer module	ICM332-1	National	10	
x	x	x	x	x	x	Development board for the NS32332.	DB332 +	National		
x	x	x	x	x	x	MMU, PMIX daughter board port, dual-port memory, five 16-bit counter timers, 1 MB RAM, 68881 math coprocessor.	M682	PacificM		
x	x	x	x	x	x	Two level memory management; On-board RAM expandable to 8 MB; 32-bit wide local architecture; five 16-bit counter/timers. Optional 68881 math coprocessor.	M682K	PacificM		
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/21	Intel		
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/22	Intel		
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/24	Intel		
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/28	Intel		
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/31	Intel		
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/32	Intel		
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/34	Intel	15	
x	x	x	x	x	x	Includes 80387 coprocessor; 64 KB zero wait-state cache memory; 16-level interrupt controller; iSBX connector for I/O expansion; uses iSBCMMOX series modules for memory expansion.	iSBC386/38	Intel		
	x					Dual 32032 processors, optional memory management unit and floating point processor, supports 32-bit memory bus.	NAP2000	Matrox		
x	x		x	x	x	Direct 32-bit processor to memory data path, ECC protection of memory data	32032M	OwlComp		
			x	x		24-bit programmable timer, battery-backed real-time clock and calendar	229A025	Amtelco		
x	x	x	x	x	x	1.5 MB/s SCSI controller, real-time clock, 2-level demand-paged MMU, up to 64 MB dual-port no-wait-state RAM.	M020	Synergy	20	
x	x	x	x	x	x	UNIX 5.2, UNIX/VRTX R/T interprocessor communication S.W., opt 68881 FPU, 68851 MMU	GPC68020	Microbar		
x	x	x	x	x	x	UNIX 5.2, UNIX/VRTX R/T interprocessor communication S.W., opt 68881 FPU, 68851 MMU	MT68020	Microbar		
	x					Includes on-board memory management unit and floating point processor, supports dedicated 32-bit memory bus.	MAP2000	Matrox		
x	x				x	Multibus I Architecture with MC68881 or MC68882 Coprocessor.	STEL68020	STI (3213)		
	x		x	x	x	Mailbox interrupts, runs UNIX, OS/9, VRTX.	HK68/M120	Heurikon	25	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
32	32	68030	16.7/25	Multibus I	5, ± 12	2-4	20-40	1 Mb/s	16 MB	4 MB	256	x
32	32	68020	12.5/25	Multibus II	12	2		62.4	4 GB	1 MB/4 MB	256	
32	8-40	80386	16	Multibus II	5	1	0	19.2	4 GB	1/16 MB	128 KB	x
32	8-40	80386	16	Multibus II	5	1	0	19.2	4 GB	2/16 MB	128 KB	x
32	8-40	80386	16	Multibus II	5	1	0	19.2	4 GB	4/16 MB	128 KB	x
32	8-40	80386	16	Multibus II	5	1	0	19.2	4 GB	8/16 MB	128 KB	x
32	8-40	80386	20	Multibus II	5	1	0	19.2	4 GB	1/16 MB	128 KB	x
32	8-40	80386	20	Multibus II	5	1	0	19.2	4 GB	2/16 MB	128 KB	x
32	8-40	80386	20	Multibus II	5	1	0	19.2	4 GB	4/16 MB	128 KB	x
32	8-40	80386	20	Multibus II	5	1	0	19.2	4 GB	8/16 MB	128 KB	x
32	32	80386	20	Multibus II	5, ± 12	1	16	9.6	2.2MB	1MB/1MB	0/256	x
32	112	ADSP-3221	8	PC/AT	5				256	256	28	
32	32	NS32032	10	Q-Bus	5,12	16-64		19.2	16MB	16MB		x
32	32	32332	15	Qbus		up to 128			120MB	16 to 128MB		x
32	16-32	68020	12.5	VERSAbus	5, ± 12			800	4Gb			
32	32	MC68000	10	VME						512		x
32	32	MC68000	10	VME						512	128	
32	32	WE32100	10/14	VME	5					64/32		
32	32	WE32100	10/14	VME	5	2	32	19.2	4Gb	1Mb	128	x
32	32	68020	12.5	VME	5, ± 12	2	0	38.4	4GB	512/4MB	100/512	
32	32	68020	12.5/25	VME	5, ± 12	2	0	38.4	4GB	1MB/1MB	100/4MB	
32	32	68020	16.7/20	VME	5, ± 12	2	0	38.4	4GB	256/1MB	100/4MB	x
32	32	68020	16.7/20	VME	5, ± 12	2	0	38.4	4GB	512/4MB	32/64	
32	32	68020	16.7/20	VME	5, ± 12	4	0	38.4	4GB	1MB/4MB	100/4MB	x
32	32	68020	25	VME	5, ± 12	2	0	38.4	4GB	512/4MB	100/512	
32	32	68020	25	VME	5, ± 12	2	0	38.4	4GB	512/4MB	100/512	
32	32	68030	20/25	VME	5, ± 12	4		38.4	4MB	1MB/4MB	0/128	x
32	32	80386	16	VME	5, ± 12	3	0	38.4	4GB	2MB/8MB	48/512	
32	32	68000	10	VME						64	x	
32	32	68020	12.5/25	VME bus	12	1		62.4	4 GB	1 MB/4 MB	128	
32	32	68020	16/20	VME bus	5	0	0	0	4 GB	4MB	64Kx8	
32	32	68020	12.5/16/20	VME/VMX	5			19.2		512/1MB	64	
32	32	68020	12.5	VMEbus	5, ± 12				4GB	512/1MB	512	x

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support						Hardware Support	Comments	Model	Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System						
x	x	x	x	x	x		Optional I/O on Omnimodule daughter boards.	OB68K/ MSBC30	Omnibyte	5
	x		x	x	x		Message passing support, UNIX, OS/9, and VRTX support.	HK68/M220	Heurikon	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 116M01	Intel	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 116M02	Intel	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 116M04	Intel	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 116M08	Intel	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 120M01	Intel	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 120M02	Intel	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 120M04	Intel	
x	x	x	x	x	x		Includes 80387 coprocessor; 64K Bytes; zero wait state cache; iSBX connector; 1 MByte DRAM.	iSBC386/ 120M08	Intel	
	x						Built in-self test. SCSI and OME interfaces optional cache. Optional 80387 numeric coprocessor.	MIBII 386/101	MicroInds	10
x	x		x	x			Array processor board capable of 16 MFLOP performance. 32 or 64-bit floating point.	APB3264AT	Marinco	
x	x	x	x	x	x		Python is a 32-bit Supermicro which runs UNIX V O/S. Provides support for up to 64 users.	PYTHON/32T	GENROCO	
x	x	x	x	x	x		High-Performance multiuser UNIX engine, supports over 100 users, blockmode DMA, cache memory, 4 Gbyte virtual addressing	SUPER PYTHON	GENROCO	
x	x	x	x	x	x		Optional demand paged virtual memory management module, on board software transparent cache configured as 4K entries, RAMbus interface, and two 28-pin ROM sockets.	M68KVM04	Motorola	
							Controls up to 4 ESDI drives with up to 15 Mb/sec. data rate. ESDI Controller.	VESDI-32	DUAL	
							Motorola I/O bus interface on board. Input/Output processor.	VIOP	DUAL	
x	x	x	x	x	x		Evaluation board for WE32100 CUP and WE32101 MMu. Interactive monitor program, individually maskable interrupts, 3 16-bit timers	WE321EB	AT&T (2526)	
	x	x	x	x	x			WE321SB	AT&T (2526)	
x	x	x	x	x	x		Zero wait-state SRAM, VME PROM real-time software included.	CPU20S	Force	
x	x	x	x	x	x		Zero wait-state SRAM, two 24-bit counter/timers, VME PROM real-time software included, VSB interface.	CPU29	Force	20
x	x	x	x	x	x		Zero wait-state dual-ported SRAM, 32-bit DMA, 16 location monitors, two 8 byte message buffers, 68882 FPCP, optional VMXbus interface, VME PROM included.	CPU22	Force	
x	x	x	x	x	x		Zero wait-state SRAM, 68851 MMU, 68881 FPCP, 24-bit timer, designed for UNIX systems.	CPU25	Force	
x	x	x	x	x	x		Dual-port DRAM, 32-bit DMAC, SCSI interface, floppy controller, 16 location monitors, two 8 byte message buffers, VME PROM real-time software included.	CPU26	Force	
x	x	x	x	x	x		Fastest 68020 with zero wait-state memory VME PROM real-time software included.	CPU20B	Force	
x	x	x	x	x	x		Fastest 68020 with zero wait-state memory, floating point processor, VME PROM real-time software included.	CPU21B	Force	
							SCSI controller, battery-backed RAM and real-time clock, VMS bus support opt. FPP.	PG211X	MicroInds	
x	x	x	x	x	x		High speed interleaved DRAM, MMU on CPU, 80387 numeric coprocessor, electronic "tag", five 8-bit counters/timers, forcebug included.	CPU386	Force	
							Universal storage controller. SCSI, ST-506, and SA450 interfaces on one board.	VUSC	DUAL	
	x		x	x	x		Mailbox interrupts, OS/9, VRTX support.	HK68/V2F	Heurikon	
x	x	x	x	x	x		Multiprocessing features, 68881, UNIX and V.2	IV3204	Ironics	30
x	x	x	x	x	x		No wait state RAM access, floating point co-processor, 16-bit programmable timer.	IV3201	Ironics	
x	x	x	x	x	x		Zero wait-state operation, MC68881 FPPU	CPU21S	Force	

Bold face indicates additional data is provided on the page noted.

## MICROCOMPUTER BOARDS (Cont'd)

General						I/O			Memory			
Data Word Size (bits)	Instruction Word Size (bits)	CPU Type	Clock Frequency Min/Max (MHz)	Bus Type	Supply Voltage (V)	No. of Serial Ports	No. of Parallel Lines	Max. Baud Rate (kb/s)	Directly Addressable Words (Kbytes)	Supplied/Extra Capacity		DMA Capability
										RAM (Kbytes)	(P)ROM (Kbytes)	
32	32	68020	12.5	VMEbus	5	2-4	16-36	3M	4GB	1MB	0/256	
32	32-64	68020	12.5/25	VMEbus	5, $\pm 12$	2		307.2	16MB	1MB	256	x
32	32	68020	16.67	VMEbus	5, $\pm 12$	2		880	32 MB	1 MB/32 MB	64K/1 MB	x
32	32	68020	16.7	VMEbus		2				1	128	x
32	32	68020	16.7	VMEbus	5, $\pm 12$	2	0	38.4	4GB	512/4MB	100/512	
32	32	68020	16.7	VMEbus	5, $\pm 12$	2	0	38.4	4GB	512/4MB	100/512	
32	32	68020	20	VMEbus	5, $\pm 12$	2	0	38.4	4GB	512/4MB	100/512	
32	32	68020	20	VMEbus	5, $\pm 12$	2	0	38.4	4GB	512/4MB	100/512	
32	32	68020	25	VMEbus	5	1				4MB	64	x
32	32	32032	10	VMEbus	5, $\pm 12$	2		38.4	16MB		32/128	
32	32	68000	10	VMEbus						512		x
32	16	68000	10	VMEbus	5	2	2	38.4	16Mb	4/112	8/512	
32	32	68010	10/12.5	VMEbus	5, 12	1			16MB	512		x
32	32	68010	10/12.5	VMEbus	5, 12	1			16MB	512		x
32	16-80	68020	12/16	VMEBUS	5, -12	4	4	880	4GB	1 MB/64 MB	32/256	
32	32	68020	12.5	VMEbus	5/ $\pm 12$	2				1MB		
32	32	68020	12.5	VMEbus	5, $\pm 12$	2		38.4	4 GB	128/2 MB	512/4 MB	
32	32	68020	12.5/16.67	VMEbus	5, $\pm 12$	1	0	38.4	4GB	2MB/2MB	0/256	
32	32	68020	12.5/24	VMEbus	12	1		62.5		1MB	128	
32	32	68020	12.5/25	VMEbus	5, $\pm 12$	3	24	38.4	4 GB	1 MB/4 MB	—/4 MB	
32	32	68020	12.5/25	VMEbus	5, $\pm 12$	2	24	38.4	4 GB	1 MB/4 MB	—/4 MB	
32	32	68020	16	VMEbus	5, $\pm 12$	2		38.4	4 GB	2 MB/8 MB	—/512	
32	32	68020	16/25	VMEbus	5, $\pm 12$	2		38.4	4 GB	2 MB	—/512	
32	32	68020	16/33	VMEbus	5, $\pm 12$	2		38.4	4 GB	4 MB	—/2MB	
32	32	68020	16.67	VMEbus						1MB	32	
32	32	68020	16.67	VMEbus	5/ $\pm 12$	2				1MB		

Sequenced alphanumerically by data word size, CPU type, and increasing clock frequency.



Software Support					Hardware Support	Comments	Model		Source	Line
Assembler	Debug/ Monitor	Editor	High Level Language	Operating System						
x	x	x	x	x	x	Optional I/O on daughter boards, optional system controller	OB68K/ VSBC20	Omnibyte		
x	x	x	x	x		On-board FPPU. Will support RS-232/422, Multidrop, 20mA current loop, fiber optic, and X.25 protocols	VMPM68KC	PEP-Modular		
x	x	x	x	x	x	MMU, PMIX daughter board port, dual-port memory, five 16-bit counter timers, 1 MB RAM, 68881, math co-processor.	V682	PacificM		
x	x	x	x	x		Optional MC68851 PMMU, MC68881 FPPU	A68VME-020	Alcyon		
x	x	x	x	x	x	PDOS and UniFLEX operating system available	CPU20	Force		5
x	x	x	x	x	x	Zero wait-state operation, MC68881 FPPU, PDOS and UniFLEX operating systems available	CPU21	Force		
x	x	x	x	x	x	Zero wait-state operation, PDOS and UniFLEX operating systems available	CPU20A	Force		
x	x	x	x	x	x	Zero wait-state operation, MC68881 FPPU, PDOS and UniFLEX operating systems available	CPU21A	Force		
	x				x	VMEbus Multiprocessor unit with MC68851 Paged Memory Management Unit (PMMU)	VMPU4M	DUAL		
x	x		x	x	x	Optional 32081 floating point unit and 32082 MMU	32032V	OwlComp		10
						Controls up to 3 SMD drives with up to 20Mb/s data rate. SMD Disk Controller.	VSMD32	DUAL		
x	x	x	x	x	x	Fully functional system controller, 16 universal JEDEC 28-pin sockets for RAM/ROM.	OB68K/VME1	Omnibyte		
x			x	x	x	Includes 4KB of zero wait-state instruction cache memory for execution speedup. MMU on board.	MVME121	Motorola		
x			x	x	x	Similar to MVME-121 without MMU.	MVME123	Motorola		
x	x	x	x	x	x	SCSI controller, real-time clock, 2-level demand-paged MMU, up to 64 MB dual-port no-wait-state RAM, on board arbiter.	V020	Synergy		15
						Includes 68881 Floating Point Coprocessor, 1 MB of DRAM, three 8-bit timers, seven-level interrupt handler	MVME133	Motorola		
x	x	x	x	x	x	32-bit real-time full military or ruggedized processor with VSB compatible local bus.	PMV CPU-1	PlesseyMicro		
x	x						OB68K/V022	Omnibyte		
	x		x	x	x	Up to 24 Hmz 68020 MPU, Up to 4MB on-card RAM, 128k EPROM, non-volatile RAM, 68851 PMMU, 68881 Floating Point Coprocessor, VSB/MVMx32 Memory Expansion Bus, Mailbox Interrupts. UNIX and VRTX supported.	HK68/V20	Heurikon		
x	x	x	x	x	x	32-bit real-time processor, floppy controller, and mailbox interrupt.	PME 68-23	PlesseyMicro		20
x	x	x	x	x	x	32-bit multi-master processor, optional 68881, mailbox facilities, and plessey extension bus (PEX), for standard and custom interfaces.	PME 68-25	PlesseyMicro		
x	x	x	x	x	x	32-bit single board computer with on-board SCSI. Ideal for UNIX and real-time environments.	PME 68-22	PlesseyMicro		
x	x	x	x	x	x	No-wait states, VSB interface to support high-speed local bus; four timer/counters provide heart beat for real-time operating system.	PME 68-21	PlesseyMicro		
x	x	x	x	x	x	32-bit single board computer, optional 68882, mailbox facilities, Plessey extension bus (PEX), for standard and custom interfaces.	PME 68-32	PlesseyMicro		
						Paged Memory Management 68851, Floating Point MC68881 on board.	VMPU32	DUAL		25
						Includes 68881 Floating point Coprocessor, 1 MB of DRAM, three 8-bit timers, seven-level interrupt handler	MVME133-1	Motorola		

Bold face indicates additional data is provided on the page noted.



## MICROCOMPUTER—SUPPORT BOARDS

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Apple</b>				<b>CIMbus</b>			
<b>Speech Circuits</b>				<b>Controllers</b>			
Board level voice synthesizer for the IBM PC/XT/AT and compatibles. Utilizes the Votrax SC-02 phoneme speech chip to produce unlimited text-to-speech output, sound effects, and music. Includes software driven text-to-speech algorithm, and phonetic speech editor to aid in the development of words and phrases.	VOTALKERIB	Votrax		Clock/calendar, real-time clock, 4-year calendar, provision for up to 32Kx8 battery-backed RAM.	CIM510	National	
Processor for Apple II +	MIMIC	Mimic		<b>Graphics</b>			
Same as votalker IB except for the Apple II, II + , & IIC line of computers.	VOTALKERAP	Votrax		Video terminal board. Includes on-board NVRAM that retains important set-up parameters such as baud rate, parity and full/half duplex operation.	CARDINAL-02	SMC	
Synthesizer. Uses SC-02 phoneme speech chip to produce unlimited text-to-speech output, sound effects and music.	VOTALKER AP	Votrax		<b>I/O</b>			
<b>Miscellaneous</b>				Analog input, 32 single-ended, 16 differential, or 8 differential and 16 single-ended channels.	CIM411	National	
Digital to analog interface for Apple Macintosh II. Provides six channels of D/A conversion.	NB-A06	NationalInst	5	Analog output, 12-bit resolution on either of two output channels.	CIM421	National	
IEEE-488 interface hardware and software for the Apple Macintosh SE.	GPIB-SE NB-GPIB	NationalInst NationalInst		Distributed I/O bus interface.	CIM230	National	25
Multifunction interface for the Macintosh II NuBus. Provides 16 channels of A/D, two channels of D/A, eight digital inputs and outputs.	NB-M1016	NationalInst		Frequency/period measurement, interface to tachometers and voltage-to-frequency converters.	CIM220	National	
<b>Bit Bus</b>				Interface to a CIMBUS system via the distributed I/O bus.	CIM311	National	
<b>Controllers</b>				Parallel, 40-bit programmable I/O lines with provisions for interchangeable line drivers and terminators.	CIM210	National	
Analog I/O board; 16 input/2 output channels; 12 bit resolution; with 12 MHz 8044 microcontroller; multitasking real-time executive in firmware; up to 64 kB RAM, ROM.	IRCB44/20A	Intel	10	Serial, single-channel asynchronous transfer.	CIM201	National	
Digital I/O board, 24 lines; with 12 MHz 8044 microcontroller; multitasking real-time executive in firmware; up to 64 kB RAM, ROM.	IRCB44/10A	Intel		Dual channel serial, independent asynchronous I/O channels.	CIM203	National	30
<b>I/O</b>				<b>Mathematics</b>			
Interfaces BITBUS network with an iSBX bus.	iSBX3444A	Intel		Processor, 2 MHz, implements transcendental math functions with AM9511 chip.	CIM550	National	
Interfaces BITBUS network with PC bus.	iPCX344A	Intel		Processor, 4 MHz, implements transcendental math functions with AM9511 chip.	CIM551	National	
<b>Multifunction</b>				<b>Memories</b>			
Remote interface	DT901/901-I	DataTrans		Local memory for CIM-1605 CPU board. Contains 15 28-pin sockets for up to 256K of EPROM or SRAM. 512 KB of static CMOS RAM or EPROM, low power and high reliability.	CIM0130	ElecConServ	
<b>Miscellaneous</b>				PROM/RAM expansion, no RAM installed.	CIM100	National	
Optical isolation/signal termination panel for iRCB 44/10A digital I/O controller board. Accepts up to 24 industry standard plug-in solid state input/output modules.	iRCX910 iRCX920	Intel Intel	15	PROM/RAM expansion, 8 Kbyte RAM installed.	CIM104	National	35
<b>C-44</b>				PROM/RAM expansion, 16 Kbyte RAM installed.	CIM108	National	
<b>Converters</b>				<b>Miscellaneous</b>			
A/D, 12-bit.	MOR800	Onset		Prototyping board 32 16-pin DIP capacity.	CIM630	National	
<b>I/O</b>				Prototyping board 63 16-pin DIP capacity.	CIM631	National	
Parallel port, 40-line.	PAR40	Onset		Voltage regulator, supplies 5, 15, and -15 Vdc to Cimbus interface.	CIM610 CIM612	National National	40
<b>Memories</b>				<b>Ethernet</b>			
Data logging, 64 Kbytes.	DS64	Onset		<b>Communications</b>			
64 Kbyte RAM.	MEM64	Onset		Ethernet node processor/LAN controller, provides 10 Mbp/s Ethernet interface, on-board EPROM.	M68KVM33	Motorola	
512K Dynamic RAM board.	RAM512	Onset	20	<b>EXORbus</b>			
				<b>Communications</b>			
				Data encryption processor.	9659	CreMicro	
				<b>Controllers</b>			
				Color RF/video.	GMS6512	GenMicro	

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>EXORbus</b>				256 Kbyte RAM, 200-ns access time.			
<b>Controllers</b>				9633 CreMicro			
<b>(Cont'd)</b>				<b>Prototyping Boards</b>			
IEEE-488 GPIB.	GMS6514	GenMicro		Board	9610	CreMicro	
Intelligent floppy disk, for 8-inch diskette drives.	9671	CreMicro		Board, buffered.	9612	CreMicro	
Intelligent Winchester floppy controller.	GMS6529	GenMicro		Board, design prototyping	GMS6513	GenMicro	
Mini-floppy controller.	GMS6519B	GenMicro		<b>Speech Circuits</b>			
QUAD ACIA and TTV.	GMS6511	GenMicro		Synthesizer and badge encoder.	9623	CreMicro	
SCSI Controller.	GMS6509	GenMicro	5	<b>Miscellaneous</b>			
<b>Converters</b>				Clock/calendar/timer.	GMS6523	GenMicro	40
A/D, 12, 14 and 16-bit, 6 inputs.	GMS6503	GenMicro		Controller, CRT/Keyboard Controller.	GMS6523	GenMicro	
D/A, 10- or 12-bit.	GMS6502	GenMicro		Debug/Monitor Module with TBUG EPROM is a self-contained development aid for 6809 systems. Also available for 6800 and 6808 systems.	MIKUL6001	TLIndustries	
Data acquisition module, 12-bit sample/hold, programmable differential gain amplifier.	GMS6520	GenMicro		Extender module	GMS6516	GenMicro	
8-Channel opto isolated D/A. Option of 8, 9 or 10-Bit accuracy, 5, or 10V range, unipolar or bipolar. 5 ms settling time.	MIKUL6077	TLIndustries	10	Intelligent, time-date subsystem, quartz referenced, non-volatile source.	9661	CreMicro	
<b>I/O</b>				Multiple programmable timer, eight MC6840 triple-programmable timers.	9640A	CreMicro	45
Analog output, 10-bit resolution for any selected bipolar span on sixteen channels between -5 Vdc to +5 Vdc.	9663	CreMicro		<b>Exorciser</b>			
Asynchronous eight channel duplex serial.	9650A	CreMicro		<b>I/O</b>			
Combination serial-parallel.	9622	CreMicro		Floppy controller.	FP950	AppBusComp	
Digital, 80 bidirectional I/O lines, 8 timers.	GMS6501	GenMicro		Video controller.	CRT80	AppBusComp	
Form C contact closure module	96703	CreMicro	15	<b>Memories</b>			
Intelligent parallel.	9657	CreMicro		EPROM Programmer.	PP6432	AppBusComp	
Parallel, sixteen 8-bit ports.	9620A	CreMicro		Memory board.	MB64	AppBusComp	
Parallel, 32 terminated inputs, 32 latched outputs.	96103	CreMicro		<b>IBM PC</b>			
Printer interface.	9625	CreMicro		<b>Communications</b>			
Processor module	9642	CreMicro	20	ARCNET controller card with fiber optic connector. For use with IBM PC/AT bus system.	ARCNET-PC300 SMC		50
Reed relay contact closure with 32 Form "A" contact sets.	96702	CreMicro		ARCNET, Token passing, network controller cards with coaxial driver. For use with IBM PC/AT bus system.	ARCNET-PC100 SMC ARCNET-PC200 SMC		
Signal switching, 8 solid-state relays, 16 mechanical relays, 32-transistors, 16 analog switches.	GMS6504	GenMicro		Ethernet PC adapter board. 10 Mbps operation, operates in IBM PC, PC/XT, PC/AT, and PS/2 systems.	WD8003E	WDC	
32 Inputs multiplexed in 4 Bytes, 32 outputs latched in 4 bytes, configured for 16-bit data transfer	MIKUL6032	TLIndustries		High-performance, twisted-pair local area network board for IBM PC/XT, PC/AT. Data rate transfer up to 2.5Mb/s, RS-422 modified.	NET-BOARD	PC-Office	
64-Input Buffered interface with schmitt trigger inputs and provision for capacitors for an RC filter. Data output selected by addressing a one-of eight decoder.	MIKUL6064-I	TLIndustries		Intelligent Ethernet controller for PC-Bus systems. 80186 CPU, 256 KB RAM, on-board transceiver optional. Supports TCP/IP Internet protocols.	EXOS205	Excelan	55
64-Output driver interface. Eight latched output bytes with high power open collector drivers.	MIKUL6064-O	TLIndustries	25	Intelligent 802.3 Ethernet board. On-board 80186 processor.	SPC Link2	Intel	
<b>Mathematics</b>				Interfaces BITBUS network with PC Bus.	iPCX344A iSBX344A	Intel	
Arithmetic processor/memory module provides both dedicated binary fixed/floating point and 16 Kbyte memory.	9611	CreMicro		LANalyzer EX 5000E Ethernet network analyzer. LAN analysis for Ethernet and StarLAN networks. LANalyzer software required.	EXOS225	Excelan	
<b>Memories</b>				StarLAN PC Adapter Board	WD8000S	Western (4911)	60
EPROM Programmer.	GMS6522	GenMicro		StarLAN PC Adapter Board with Integrated Hub	WD8000SH	Western (4911)	
16 Kbyte static RAM, with parity, clock speed 1 or 2 MHz.	MEX6816-22S	Motorola		X.25 Packet Switching Board for IBM PC/XT/AT Compatibles	WD4025A-PCD	Western	
32 Kbyte EPROM/RAM.	9616A	CreMicro		1200 baud half-card size internal modem. Works with PS/2 system.	1090	Microcosm	
32 Kbyte non-volatile memory (battery backed).	GMS6524	GenMicro	30				
64 Kbyte RAM, accommodates 20 address lines.	9638	CreMicro					
64 Kbyte, 256 Kbyte, 1 Mbyte Dynamic RAM.	GMS6505	GenMicro					
128 Kbyte EPROM/RAM.	GMS6508	GenMicro					
128 Kbyte RAM, up to 20 address lines.	9634	CreMicro					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>IBM PC (Cont'd)</b>							
<b>Controllers</b>							
A full size PC/AT bus-compatible board providing both a Centronics-compatible device controller and a Versatec-compatible device controller. For connection of various electrostatic plotters/printers, laser printers, color copies, etc.	10092	IKON		Stepper motor controller for three axis. Independently controls up to three four-phase stepper motors. Step rate, acceleration, deceleration, number of steps, direction, and ramp-down points are controlled. Output allows rates of up to 240K pps. Features three SBX connectors. Five limit inputs per axis.	5000	Tech80	
Coprocessor/real-time controller board. On-board NC4016 processor. 128K bytes of high-speed CMOS static RAM permits predictable and repeatable operation for real-time hardware development.	NB4100	Novix		Supports SMD or SMD-E drives, high-speed DMA, 20 Mb/s disk data rates, Overlapped seeks, bad media mapping, hardware and software compatible with IBM, PC, XT, AT, and compatibles.	MAVERICK	Interphase	
Distributed controller with CPU and I/O that networks into any PC/XT, or PC/AT.	60IOMUX	Digitronics		Winchester and floppy disk, supports ST506/412 and ESDI interfaces consecutive sector transfer.	OMTI8620	SMS	
Ethernet/IEEE 802.3 communications controller, menu-driven diagnostics perform internal and network testing, for PC, XT, AT, and COMPAQ	NI5010	Micom Int		Winchester Disk and Floppy Disk Controller with IBM PC/AT Interface	WD1003A-WA2	Western	20
Ethernet/IEEE 802.3 communications controller, TCP, IP, and XNS protocols	NP600	Micom Int		Winchester Disk Controller, ESKI to IBM PC/AT Interface	WD1005-WAH	Western	
Ethernet intelligent controller with 80186 microprocessor, DMA capability, TCP/IP transport protocols.	EXOS205	Excelan		Winchester Disk Controller, ST506 to IBM PC/AT, SMT Half-Slot	WD1002A-WX1	Western	
GPIO controller—backplate accepts GPIB stackable connectors directly; support for 5 languages; small format fits XT-type short slots.	ZT1444	Ziatech	5	Winchester Disk Controller, ST506 to IBM PC/AT, 1:1 Interleave	WD1006-WAH	Western	
Graphics controller for IBM PC and compatibles. Based on the TI 34010 GSP, works with Microsoft Windows and high end CAD applications as well as desktop publishing. Has 512K bytes of dual-ported video RAM.	Rendition I	Renaissance		Winchester Disk Controller, ST506 to IBM PC/XT, SMT Half-Slot, RLL	WD1002-27X	Western	25
Graphics display controller. 640x480 resolution provides fast zoom, pan for users of PC-CAD. Eliminates the need for using a 19-inch high resolution monitor. Compatible with VersaCAD, AutoCAD, and DataCAD software. For the IBM PC/XT/AT or COMPAQ 386 and compatibles	Nth Engine	NthGraphics		Winchester Disk Controller with IBM PC/AT Interface	WD1003S-WAH	Western	
Graphics display controller for the IBM PC/XT, AT COMPAQ 386 or compatibles. Provides fast pans and zooms for PC CAD users. Works with AutoCAD, VersaCAD, and DataCAD software.	752	NthGraphics		Winchester Disk Controller with IBM PC Interface	WD1002S-WX2A	Western	
Graphics display controller provides fast pans and zooms for PC CAD users. Has 1024 x 768 resolution for use with 19" monitors. Works with AutoCAD, VersaCAD, DataCAD software. For the IBM PC/XT, AT, COMPAQ 386 and compatibles.	1024	NthGraphics		Winchester disk drive controller; controls two drives with ST506/412 interface. Compatible with IBM PC/XT host interface, 5 Mbps data rate.	SMC4000-PC	SMC	
IBM PC AT host bus	OMTI8000	SMS		Winchester disk, supports ESDI drives up to 10 megabit drive transfer rate.	OMTI6510	SMS	
Intelligent servo motor controller. Controls one dc servo motor. Thirty-two bits of position, velocity, acceleration/deceleration. Position and velocity changing, analog output to motor. Trigger and $\pm 10$ V outputs to an oscilloscope. Two channels and index for TTL or CMOS-level incremental encoder feedback.	5628 5629	Tech80 Tech80		Winchester disk, supports ST506/412 drives, MFM or 2,7 RLL encoding, consecutive sector transfer.	OMTI5520 OMTI5526 OMTI5527 OMTI5529	SMS SMS SMS SMS	30
Multifunction GPIB controller—backplate accepts GPIB stackable connectors directly; support for 5 languages; Multimodule expansion socket; battery back-up clock/calendar.	ZT 1488A	Ziatech		Dual Winchester drive controller card. For use with IBM PC/XT bus system.	SMC4003-PC	SMC	
Short slot surface mount dual Winchester controller. For use with IBM PC/XT bus system.	SMC4004-PC	SMC		1280x968 color graphics processor, 256 colors from 4096 color look-up table, 100% IBM software compatible.	PG1280	Matrox	
				512x512 x 8-bit image processor combines image digitization and display, includes software image processing subroutine library.	PIP512	Matrox	35
				640x480 color graphics processor, 256 colors from 4096 color look-up table, 100% IBM software compatible.	PG640	Matrox	
				<b>Converters</b>			
				A/D converter, 8-channel, 15-bit, $\pm 10$ V to $\pm 20$ mV in five ranges. Measures resistance, current, thermocouples, RTD's and thermistors, has DC/DC converter and DSP function.	409	Sensoray (4901)	
				64-input A/D converter, 24 parallel lines	A/D64-PC	IndComp	
				64-output A/D converter, 24 parallel lines	D/A64-PC	IndComp	
				128 channel common-node A/D, D/A. 128 analog inputs, 128 analog outputs. Each A/D input connected to respective D/A output.	ADA128	IndComp	40
				32-Input high-resolution analog converter. 32 single-ended/16 differential analog inputs, 12-bit input converter resolution. For IBM PC/XT, PC/AT, or compatibles.	A/D12B32	IndComp	

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>IBM PC</b>							
<b>(Cont'd)</b>							
<b>Data Acquisition Systems</b>							
High-speed data acquisition module with 12-bit resolution. 180 kHz throughput rate using DMA, eight channel input.	PCI20023M-1	Burr-Brown		Switching graphics adapter that utilizes Microsoft Windows silicon and emulates all four industry graphics standards. Applications for high-end CAD, desktop publishing, spreadsheets, and word processing are supported.	Legacy II	Renaissance	
<b>Digital Signal Processing</b>				The original Hercules graphics board which has third party software support packages available.	Graphics Card	Hercules	
Digital signal processor board used with ASPI's Algorithm Development Package (ADP) to provide a development system for the TMS32020 DSP microcomputer.	320/PC-20	Atlanta		TMS340 color graphics controller board configured to support 640x480x4 resolutions, uses TMS34061, TMS34070, and TMS4161	TMDS3471804000	TI	
<b>Graphics</b>				Single board frame grabber from IBM PC/XT, 512x512x8 resolution, holds two images.	PCVISIONplus	Imaging	20
Acquisition, storage and display for machine vision, factory automation, medical imaging, and teleconferencing.	IVG128	Datacube		Single board real-time image processor with 512x512x8 resolution. Holds four images, split-scan mode, driver software, for IBM PC/AT computers.	Series 100	Imaging	
Auxiliary frame processor for high speed image processing with the DT2851 High Resolution Frame Grabber. 512x512x16 bit frame processing, zoom, pan, scroll, and logic operations.	DT2858	DataTrans		Single board triple frame buffer plus ALU in hardware. Source coded software for image processing.	MAXVISION	Datacube	
Comparable to the IBM Color Graphics Adapter (CGA). Uses a half-size slot of the IBM PC/XT or compatibles.	Color Card	Hercules	5	<b>I/O</b>			
Displays text, but not graphics on monochrome monitors. Half card size replacement for IBM Monochrome Display Adapter (MDA).	Text Card	Hercules		Analog input and digital I/O, 16 digital I/O lines, 32 single-ended or 16 differential channels, programmable gains up to 500	RTI800	AD	
EGA graphics board. Provides compatibility with the IBM Enhanced Graphics Adapter (EGA). Supports 16 color graphics at resolutions up to 640x350 pixels and offers text resolutions up to 720x350 pixels. Has 256K bytes of RAM, works with the IBM PC and compatibles.	Renegade	Renaissance		Analog output board, 4 or 8 analog input channels, 12-bit resolution	RTI802	AD	
Frame grabber, 512x512x8 bit for real-time digital image processing on the PC/AT.	DT2853	DataTrans		Analog output, on-board processor, 12-bit resolution	DA12	Robotrol	25
Genlock/insertion and on-board CGA. Synchronizes graphics/alphanumerics with user supplied RS-170A video signal. Can also be used as CGA alone. Composite video outputs to VCR/monitor, compatible with IBM CGA software.	VO-CGA	KSystems		Analog, 8 differential or 16 single-ended, 12-bit resolution	ADA88	Robotrol	
Has ability to display 730 by 348 pixel resolution in 16 colors out of a 64-color palette. Has Hercules' RamFont mode and is compatible with Hercules monochrome cards.	InColor Card	Hercules	10	BITBUS network to iSBX bus interface.	iSBX344A	Intel	
High performance subsystem for IBM PC/AT. Includes all of the module listed in the Series 150 (VMEbus section).	Series 151	Imaging		Digital input/output board, 24 channels, parallel data transfer	RTI817x2	AD	
High-resolution frame grabber for real-time digital image processing on the IBM PC/AT. 512x512x8 bit resolution, 256 gray levels. Real-time processing includes: frame averaging, frame addition, and subtraction, and logic operations.	DT2851	DataTrans		Digital input/output, 24 channels, three 8-bit ports	RTI817	AD	
Highlights the capabilities of the RamFont display mode and combines the speed of text mode with the graphics mode.	Graphics Plus	Hercules		Discrete and analog I/O interfaces. Direct line to I/O racks external to the computer at up to 2M points/s.	6-IBM/IO	Digitronics	30
Low cost digital imaging system for the IBM PC, XT, AT and compatibles.	Micron Eye	MicronTech		Enables the IBM PC to become a master on the VMEbus. This allows the IBM PC to communicate with any slave on the VMEbus.	PC/VME-STD	AjidaTech	
Low-cost version of the Color Card that does not include a parallel printer port	Color Card/NP	Hercules		High-level analog and digital I/O system	DT2801	DataTrans	
Solids Modeling Engine (graphics accelerator)	WTE7100	Weitek		High-speed analog and digital I/O system for PC/AT applications; A/D conversion. Support for 5-level bus interrupt, 16 digital I/O lines.	DT2827	DataTrans	
				High-speed PF474 string comparator.	Proximity Board	Proximity	
				I/O, Digital, MIL-STD-1397 (NTDS) Type A (SLOW) or B (FAST), 16/32 bit, Peripheral/computer/Intercomputer Modules, DMA or non-DMA bus interface, single card.	850701	Syscon	35
				IBM PC/AT to Multibus adaptor.	402	Bit3Comp	
				IBM PC/AT to VME bus adaptor.	403	Bit3Comp	
				IBM PC to Multibus adaptor.	401	Bit3Comp	
					404	Bit3Comp	
				IBM-PC/XT/AT MIL-STD-1397 (NTDS) I/O interface board. Provides full duplex interface to a MIL-STD-1397 (NTDS) type C peripheral, intercomputer or computer I/O channel.	860901	Syscon	40
				IEEE-488 Interface and handler GPIB-PC II.	77609201	NationalInst	
				IEEE-488 Interface and handler GPIB-PC III.	77611401	NationalInst	
			15	Industrial distributed LAN controller, up to 307.2K baud	6-IBM/N	Digitronics	
				Intelligent serial networking Board w/Dual RS-232C parts, Z80A processor, 64kRAM, Calendar/Clock w/Battery Backup, Serial Networking Software and IBM-PC Drivers on Diskette.	INFOCAP1000	IndComp	

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>IBM PC (Cont'd)</b>							
<b>I/O</b>				Floating point array processor for IBM PC, PC/XT, or PC/AT computers. 32-bit floating point addition, subtraction, and multiplication.	DT7010	DataTrans	25
Low-level analog and digital I/O system	DT2805	DataTrans		Floating-point array processor, 32-bit for the IBM PC/AT.	DT7020	DataTrans	
MIL-STD-1397 (NTDS) type A/B communications interface card for the AT/248/386.	870401	Syscon		Numeric data processor module. Plugs into the socket of the 8088 processor. This module has sockets on it for both the 8088 and the 8087 numeric data processor	zSBC337	Ziatech	
Modular data acquisition system. Easily set up to provide thousands of acquisition, test, measurement and/or control options. Carrier and module boards allow hardware changes or additions as your needs change. A selection of 21 software packages support the family.	PCI20000Family	Burr-Brown		<b>Memories</b>			
Multifunction analog and digital I/O board, 16 analog input channels, software programmable gains, 8 digital input/output channels, supports DMA, polled status, and interrupt operation	RTI800x2	AD		EPROM/RAM board socketed for up to 256K of RAM, half card size.	PRC4-PC	IndComp	
Multifunction analog input and digital I/O board, 2 analog output channels, 12-bit resolution, 3 counter/timer channels	RTI815x2	AD	5	Expandable dynamic RAM designed for Zenith 150/Z-160 PC's, game port or real time clock optional with battery back-up IBM-PC compatible.	Z-150MB	Teletex	
Multifunction I/O Board.	I/O A +	AppBusComp		Holds eight E/PROM Chips which may be 2764, 27128, 27256, or 27512's.	714100025	Inventive	30
Multifunction I/O board for data acquisition and control	DT2806	DataTrans		IBM PC/RT compatible memory board with 8MB configuration. Fast cycle times of 170 ns.	CI-RT	Chrislin	
Multifunction, two 12-bit analog output channels, 32 single-ended or 16 differential channels	RTI815	AD		Memory card, battery-backed CMOS RAM. For IBM PC/XT systems.	2160	IndTech	
Serial/parallel I/O board with option for second parallel port. Works with PS/2 system.	1045	Microcosm		Memory card, battery-backed CMOS RAM, 128K to 1Mbyte. For IBM PC/AT systems.	2170	IndTech	
Similar to the PC/VME-STD, except that it supports the double-high VME bus with full 32-bit data and address capability.	PC/VME-EXT	AjidaTech	10	ROM disk with DOS. Systems with disk drives acts as a memory expansion board, systems without disk drives acts as a diskless PC/AT system.	FE5410	Faraday	
Simultaneous sample and hold analog and digital I/O	DT2818	DataTrans		Two Mbyte memory board for the IBM PC, XT and compatibles. Software available for debug and diagnostics.	1204	MicronTech	35
Turns an IBM or compatible into an I/O simulator and on-line monitor for the Allen-Bradley PLC-2/20 and PLC-2/30 programmable controllers.	PLC2	HEI		Four Mbyte memory board for the IBM AT and compatibles with debug and diagnostic software available.	1306/8/10	MicronTech	
Video subsystem for video digitization and display	DT2803	DataTrans		0.5 Mbyte memory board.	AI1512	AppBusComp	
Voice Synthesizer—64 unique phonemes for unlimited vocabulary, on-board 4W audio amplifier.	MSI-VS01	MicroCompSys		1 MB DRAM memory, 4 and 8 MB capacity, no switches or jumpers. For IBM PC/AT Models 6050 and 6051.	RTRAM	Clearpoint	
Single board analog and digital I/O	DT2808	DataTrans	15	1 Mbyte primary AT memory board (no loaded memory).	1067	Microcosm	
Single board analog and digital I/O system featuring 20 kHz A/D converter, two 50 kHz D/A converters, eight digital input lines, eight digital output lines, and a programmable clock.	DT2811	DataTrans		1 Mbyte secondary AT memory board (no loaded memory).	1071	Microcosm	40
128-line parallel I/O board with two RS-232C serial ports	1018PC	IndComp		2 to 4 Mbyte secondary AT memory board (no loaded memory).	1074	Microcosm	
16 channel analog input, 12 bit, 220 khz, 256 k Sample memory	RTI860	AD		<b>Multifunction</b>			
64 Analog Inputs (12 bits), 16KHZ 16 Analog Outputs(12 bits) 24 Digital I/O	RTI820	AD		Accelerator board for the IBM PC and PC/XT. Provides full 10 MHz clock speed, on-board 80286 processor and 80287 coprocessor. Runs with 4.77/8/10 MHz motherboards.	ACCELERATOR286	EdsunLabs	
8 channel analog input, 16 bit, 40 khz, 256k sample memory	RTI850	AD	20	Bus interface with wait-state generator, 8 memory sockets (64K/256K static), digital I/O, keypad input, alphanumeric LCD driver, prototype area, interrupt request lines, A/D converter, D/A converters.	MFC	Vesta	
<b>Mathematics</b>				Data line monitor. EIA RS-232C, CCITT interfaces, full duplex and half duplex display capability. Real-time passive line monitoring to 19.2K baud.	Metascope-PC	Metatek	
Array processor, capable of performing integer and floating point math, 8 MOPS. Extensive software libraries available. For IBM PC-AT	APB3024AT	Marinco		Memory board.	MAGA A +	AppBusComp	45
Array processor, capable of performing integer or floating point math. Can be programmed for signal processing, image processing, graphics, and seismic analysis	APB3016PC	Marinco		MIL-STD-1553 bus controller and remote terminal unit. Interfaces the IBM PC to the MIL-STD-1553 data bus.	BUS65515	ILC-DDC	
Array processor, capable of 16 MFLOPs. Extensive software libraries and programming tools available. Both 32-bit and 64-bit floating point.	APB3264AT	Marinco		Multifunction board capable of master/slave bus control. Supports 20-bit address bus and 8-bit data. On-board NC4016 16-bit processor.	NB4300	Novix	
Array processor with 20 million floating point operations/second.	POINT-1	DSP-Systems					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line	
<b>IBM PC</b>				<b>Miscellaneous</b>				
<b>Multifunction (Cont'd)</b>								
Multifunction board with up to 2 MB of memory. Includes a serial and a parallel port, works with PS/2 system.	1092	Microcosm		A complete high performance development package that converts any IBM PC/XT/AT or compatible in to an environment that supports series 32000 applications. Supports the following devices in this family: NS32032 CPU, NS32082 MMU, NS32201 TCU, and NS32081 FPU.	SYS32/20	National		
Multifunction board with 6809 MPU, 8K RAM, three ROM sockets, two RS-232 serial ports, four parallel ports, watchdog timer, and real-time clock.	MCH48	Wintek	(4913)	Adapts the IBM PC, PC/XT, PC/AT, and compatible computers to the SCSI bus.	ADP31S	NCR		
POACH/AT evaluation system. Intended for analysis of PC/AT related systems. Based on the ZyMOS standard POACH/AT chip set, it can be used to verify hardware and software compatibility with associated AT products.	ZyAT1	ZyMOS		Daughter board to upgrade 68000 CPU's to 68020 with 68881 floating point chip.	D020	IoInc	15	
POACH/AT-12 evaluation system. High-performance 12 MHz, zero-wait state evaluation board intended to show the capabilities of the POACH/AT chip set. Has independent operating frequencies for the processor, coprocessor, expansion bus, and keyboard interface.	ZyAT2	ZyMOS		Digital filter design system with real-time digital filter and FIR filter development system for the IBM PC. Programmable filter with 1 to 128 taps.	DFS001-PC	Calmos	(2553)	
POACH/ATB evaluation system. Integrates all of the functions of a standard PC/AT in an expansion card format. Uses the POACH/AT chip set and the POACH/ATB chip which is 80286 compatible.	ZyATB1	ZyMOS		Host adaptor, connects the IBM PC bus to the SCSI bus.	OMTI510 OMTI512	SMS SMS		
POACH/AT386-32 evaluation system. Employs the POACH/AT386, a companion part of POACH/AT chip. Integrates all the functions of a standard PC/AT motherboard. Supports 16- or 32-bit AT-compatible designs that use standard AT busses.	ZyAT386-32	ZyMOS		IEEE-488 interface hardware and software for the IBM PC convertible.	GPIB-PC/CONV GPIB-RTPC MC-GPIB	NationalInst NationalInst NationalInst	20	
POACH/XT-1 evaluation system. Integrates all of the functions of a standard PC/XT motherboard. Includes the 8088 microprocessor, the 8087 coprocessor, 64 Kbytes of ROM, 640 Kbytes of RAM, all standard XT I/O functions, and a standard interface to the system expansion bus, the I/O channel or system bus.	ZyXT1	ZyMOS		Interface between IBM PC and VME bus. Enables PC to act as a master on the VME bus. Single high and double high version available.	PC/VME	AjidaTech		
POACH/XT88 and POACH/XTB evaluation system. Comprises all the functions of a standard PC/XT motherboard. Includes the 8088 microprocessor, an 8087 coprocessor socket, 64 Kbytes of ROM, 640 Kbytes of RAM, all standard XT I/O functions, and a standard interface to the system expansion bus, the I/O channel or system bus.	ZyXTB1	ZyMOS		IRIG-B synchronizable reader/generator, event register, propagation delay correction, FIFO bus interface, AGC, auto-parity. Compatible with PC/AT, 1µs accuracy, on-time rate and frequency outputs.	AITG-PC	KSystems		
Dual tasking accelerator for IBM PC/AT. V20 microprocessor at 8 MHz, 640K bytes of additional RAM for use with second task.	BiTURBO	Alloy		IRIG-B time code reader. IRIG-B time code stripper with AGC, on-board event time measurement, PC bus interface, high-speed forward/reverse read. Start/stop match option.	VTTR-PC	KSystems		
16-Bit adapter card for IBM PC/AT systems. RAM expandable to 3Mbyte. Four serial ports, game port, parallel printer port, and status port.	2270	IndTech		Multisensor A/D interface for thermocouples, voltage, RTDs, thermistors, or current. Software programmable gains, eight channels. Full range sensor linearization using on-board microprocessor and 14-bit A/D.	409 7409	Sensoray Sensoray	(4901) (4901)	25
				TMS34010 software development board used to develop/debug TMS34010 application programs.	TMDS3411804420 TI			
				Single-slot add-on card supports three SBX modules.	LSBX-AT/MOTHER	CompModules		
				4 (Or More) Axes counters, Accepting input Data Streams at up to 4-MHZ PROM linear or rotary encoders.	01-86-010	Kern		
<b>Prototyping Boards</b>				<b>IIOC</b>				
				<b>Controllers</b>				
Personal prototyping system. Multipurpose interface and prototyping system for IBM PC and compatibles. Includes D/A, A/D, timers digital I/O, hardware and software.	PPS	AjidaTech		Color graphics expansion for GPM, 3 memory sizes for GPM expansion: 64, 128, and 192 Kbytes	GME	PEP-Modular	30	
				Color graphics expansion module for PDC board, blinking and brightness control possible	FGZ	PEP-Modular		
				Color graphics processing module, color expansion with GME module, light pen connectable, up to 255 color or gray steps, ASCII character set available	GPM	PEP-Modular		
				Floppy disk controller module for 3-1/2, 5-1/4, or 8-inch drives	FDC	PEP-Modular		
				Multiple mass-storage device controller with on-board FIFO. Simultaneously supports two Winchester drives (ST-506) and four floppy drives (mixable 5 1/4", 3 1/2", and 8") with one streaming tape.	MSC	PEP-Modular		
				Power relay module, 8 SPDT relays with 24 V coil	RLM1	PEP-Modular	35	
				SASI bus interface module for control of Winchester drives and tape drives	DIO	PEP-Modular		
<b>Speech Circuits</b>								
Synthesizer. Uses SC-02 phoneme speech chip to produce unlimited text-to-speech output, sound effects and music.	VOTALKER IB	Votrax						

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>IIOC</b>				<b>Miscellaneous</b>			
<b>Controllers</b>				<b>I/O Channel</b>			
<b>(Cont'd)</b>				<b>Controllers</b>			
Video monitor controller with 4 Kbytes of RAM, TTL or video output	PDC	PEP-Modular		EPROM programmer for 2Kx8 through 64Kx8 chips. Programmer software available for several operating systems.	UEP2	PEP-Modular	
<b>Converters</b>				<b>Converters</b>			
Analog to digital, 16 single-ended and 8 differential inputs, 12-bit resolution	ADI-1A	PEP-Modular		A/D input expander module, adds 8/16 additional differential/single ended inputs to MVME600.	MVME601	Motorola	
Data acquisition module, A/D, D/A converter, 8-bit resolution	DAM	PEP-Modular		12-bit A/D converter, 8/16 differential/single-ended channels with four full-scale input voltage ranges of 0.5, 1.0, 5.0 or 10.0 V.	MVME600	Motorola	
Digital to analog, four independent channels, 12-bit resolution	DAI-1A	PEP-Modular		16/32-channel differential/single-ended intelligent A/D conversion. Controls 12-bit A/D converter and multiplexed analog inputs from 16/32 channels.	M68RAD1-1	Motorola	
<b>I/O</b>				<b>iSBC</b>			
Bus coupler, link between the PDVNET line (75 ohm coaxial/fiber optic) and the serial interface module IFC	BK	PEP-Modular	5	<b>Communications</b>			
Parallel I/O module, 40 lines (TTL level), 1-MHz system frequency	PIM2A	PEP-Modular		Advanced data communications processor offers three HDLC/SDLC half/full duplex communications channels-optional ASYNC/SYNC on two channels, supports RS232C (including modem support) CCITT V.24 or RS442A/449 interfaces, on-board DMA supports 800K baud operation, self-clocking NRZI SDLC loop data interface, 16Kbytes static RAM, two iSBX bus connectors.			
Parallel opto-isolated I/O module, up to 2 A output current	PIO4	PEP-Modular		<b>Controllers</b>			
Parallel opto-isolated input module, 12 to 60 Vac/dc signals	IIO	PEP-Modular		Controls up to four soft sectored SMD interface compatible disk drives, 12 Mbyte to 2.4 Gbyte per controller, on-board diagnostic, ECC and full sector buffering.	iSBC220	Intel	
Parallel opto-isolated input module, 32-channel optional LED per channel for line status	PI	PEP-Modular		Flexible diskette controller for most single and double density disk drives, on-board, iSBX bus for additional functions, read and write on single or multiple sectors.	iSBC208	Intel	
Position/velocity sensor module, used in NC/CNC machines to keep track of the relative position, direction, and velocity	PVM	PEP-Modular	10	Generic Winchester controller for up to four 5-1/4, 8 or 14-inch Winchester disk drives, compatible with standard multibus, supports ANSI X3T9/1226 standard interface. On-board diagnostics and ECC plus full sector buffering.	iSBC215	Intel	30
Real time clock module, programmable switch on and switch off possibilities, output data for year, month, day, hour, minute, and seconds, output format in binary or BCD	CEU	PEP-Modular		Intelligent communications controller with 4 programmable USART channels, 8085A CPU, clock, 16 Kbytes dual-port RAM, 12-level programmable vectored interrupt control, RS232C drivers and receivers.	iSBC544	Intel	
Serial I/O module with either four RS-232C or Four 20mA current loop interfaces	SIO4	PEP-Modular		Intelligent digital I/O Controller with up to four microprocessors, 3 MHz 8085A central control processor, three operational modes-stand-alone digital controller, multibus master, intelligent slave (slave to multibus master); 2 Kbytes dual port static RAM, sockets for up to 8 Kbytes of 2758, 2716, 2732 EPROMs; 48 programmable parallel I/O lines, three programmable counters, 12 levels of programmable interrupt control.	iSBC569	Intel	
Serial interface module to provide a link between the Bus Coupler and the IIOC, cable length may be up to 25 meters	IFC	PEP-Modular		Single density flexible diskette controller has direct compatibility with most soft-sectored standard 8-inch and 5-1/4-inch drives, DMA I/O, support by cp/M operating system.	iSBC204	Intel	
Temperature sensor module for use with type J or type K thermocouples	TSM	PEP-Modular					
Quad serial interface module for IIOC. Available with two serial ports to optionally support RS-232/422, Multidrop, 20 mA current loop, fiber optics, and X.25.	SIO4N	PEP-Modular	15				
Two PIAs, programmable timer (MC6840), 2 serial interfaces (MC6850) for RS-232 and 20mA current loop	CIM2	PEP-Modular					
40 parallel I/O lines (TTL level), 3 independent 16-bit timers, RS-232, and RS-422 serial ports	CIM3	PEP-Modular	20				
<b>Mathematics</b>							
Arithmetic module for trigonometric or other math functions, fixed or floating point	APM	PEP-Modular					
<b>Memories</b>							
Dynamic RAM module with byte parity, hidden refresh	512K8	PEP-Modular					
Static RAM/EPROM module, 64Kbytes, power up/down logic protects RAM against overwriting, on-board battery backup	BMU2	PEP-Modular					
<b>Prototyping Boards</b>							
Board, address range up to 64 Kbytes	PRM	PEP-Modular					

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‡ High Radiation Resistance

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>iSBC</b>							
<b>Controllers (Cont'd)</b>							
4-Channel communications controller, 4 RS232C or 20 mA current loop buffered USART channels plus Auto-Call Unit Interface with programmable baud rates.	iSBC534	Intel	5	4 Kbyte of static RAM directly to iSBC 80/24 or iSBC 88/40 single board computers, 0.5 watts incremental power dissipation.	iSBC301	Intel	20
1/4-inch tape drive interface provides tape backup capability for iSBC215G generic Winchester controller. Supports transfer rates of 90 Kbyte, 30 Kbyte or 17 Kbyte/s depending on tape speed.	iSBC217B	Intel		4 Mbyte Parity RAM, iLBX, synchronous interface	iSBC040EX	Intel	
				8 Kbyte RAM expansion diectly to iSBC 86/05 and iSBC 88/25 single board computers, single + 5V supply.	iSBC302	Intel	
				26 Kbyte RAM expansion through direct multibus interface, on-board parity generator/checker and error status register, jumper selectable base address on any 4 Kbyte boundary within a 16 Mbyte address space.	iSBC056A	Intel	25
			28-pin multimodule EPROM with sockets for up to 64 Kbyte of expansion with 27128 EPROMS.	iSBC341	Intel		
			32 Kbyte of dual port dynamic RAM and plugs directly into iSBC86/12A single board computer.	iSBC300	Intel		
			32 Kbyte RAM expansion through direct multibus interface, on-board parity generator/checker and error status register, jumper selectable base address on any 4 Kbyte boundary within a 16 Mbyte address space.	iSBC032A	Intel	30	
			64 Kbyte EPROM expansion via direct multibus interface, switch selectable base address on 4 Kbyte boundaries for each memory bank.	iSBC464	Intel		
			64 Kbyte RAM expansion through direct multibus interface, on-board parity generator/checker and error status register, jumper selectable base address on any 4 Kbyte boundary within a 16 Mbyte address space.	iSBC064A	Intel		
			128 Kbyte of dual port RAM expansion for iSBC 86/30 single board computer.	iSBC304 iSBC3042	Intel Intel	35	
			128 Kbyte parity RAM multimodule expansion for iSBC188/48 single board computer.	iSBC307	Intel		
			128 Kbyte RAM, direct IEEE P796 multibus interface, single-bit error correction and double bit error correction via Intel 8206 device.	iSBC028C	Intel		
			128 Kbyte RAM expansion through direct multibus interface, on-board parity generator/checker and error status register, jumper selectable base address on any 4 Kbyte boundary within a 16 Mbyte address space.	iSBC028A	Intel	10	
			256 Kbyte RAM, direct IEEE P796 multibus interface, single-bit error correction and double bit error correction via Intel 8206 device.	iSBC056C	Intel		
			512 Kbyte Parity RAM, iLBX, synchronous interface	iSBC012EX	Intel		
			512 Kbyte RAM, direct IEEE P796 multibus interface, single-bit error correction and double bit error correction via Intel 8206 device.	iSBC012C	Intel	15	
			512 Kbyte RAM, direct multibus interface to iSBC86, iSBC88 or iSBC 80 single board computer; on-board parity generator/checker and error status register.	iSBC012B	Intel		
				<b>iSBX</b>			
<b>Memories</b>				<b>Communications</b>			
Bubble memory, 512 Kbyte, automatic error correction, DMA capability non-volatile storage.	iSBC254S	Intel	15	Modem, Bell standard 212A and 103, DTMF or pulse dialing, software controlled interface, parity generation/checking, sync byte detection/insertion, sync or async operation, single-wide SBX board.	ZBX212	Zendex	
iLBX 128 Kbyte RAM allows access to both multibus and iLBX interfaces, single bit error correction and double bit error detection, 16 Mbyte addressing capability.	iSBC028CX	Intel		Modem module provides Bell 103/212A compatible communication link. 300 or 1200 baud. Pulse or DTMF dialing with ring detect. Operates in interrupt or polled mode.	MSBX355	MicrolInds	
iLBX 256 Kbyte RAM allows access to both multibus and iLBX interfaces, single bit error correction and double bit error detection, 16 Mbyte addressing capability.	iSBC056CX	Intel		Serial communications expansion module. Two independent RS-232 ports, programmable baud rate with rates to 64K baud, single width.	SERX232	SBE	
iLBX 512 Kbyte RAM allows access to both multibus and iLBX interfaces, single bit error correction and double bit error detection, 16 Mbyte addressing capability.	iSBC012CX	Intel					
Univerbal site memory expansion board supports EPROM, ROM, E <sup>2</sup> PROM, SRAM, IRAM and NURAM. Contains sixteen 28-pin sockets, iLBX Bus or multibus selectable.	iSBC428	Intel					
Up to 16 Kbyte EPROM expansion plugs directly into iSBC 86/12A single board computer.	iSBC340	Intel					
1 Mbyte ECC RAM, iLBX	iSBC010CX	Intel					
1 Mbyte Parity RAM, iLBX, synchronous interface	iSBC010EX	Intel					
2 Mbyte advanced 4 Mbit controller	iSBC264	Intel					
2 Mbyte ECC RAM, iLBX	iSBC020CX	Intel					
2 Mbyte Parity RAM, iLBX, synchronous interface	iSBC020EX	Intel					

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‡ High Radiation Resistance

\*Typical Value

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>iSBX</b>				12-bit A/D and D/A converter. 16 single-ended/8 differential inputs, 8 outputs.			
<b>Communications (Cont'd)</b>				RBX388 Robotrol			
Serial data communications peripheral system offers secure data communications over standard telephone lines. The modem is available without the data encryption as CDX-MOD. Similarly, the data encryption is available without the modem as CDX-SAF.				<b>Graphics</b>			
CDX-SAF/MOD CompDyn				Audio/visual display SBX module provides six hexadecimal points and one audio transducer, digit blanking, colons, decimal points, alpha-numeric display and audio annunciation are included.			
<b>Controllers</b>				ZBX901 Zendex			
Flexible disk controller is software and hardware compatible replacement for iSBX 218 module. Controls most single/double density and single/double sided floppy drives, read and write on single or multiple sectors.				High-speed graphics multimodule			
iSBX218A Intel				MSBX900 Matrix			
Floppy disk controller for up to four single/double sided, single/double density floppy disks. Supports 3.5", 5.25", or 8" drives.				MSBX900 Matrox			
ZBX218B Zendex				Video graphic module interfaces to color or monochrome monitors. 640x480 pixels, non-interlaced. RGB analog output on 9-pin connector.			
Floppy disk controller—supports any combination of 5-1/4, 8 inch, single or double side/density drives, IBM standard formats. Western Digital 2793/1793 software interface.				mSBX278 MicroIncls			
SBSxFDC SingleBoard				<b>I/O</b>			
Floppy disk controller, 3.5", 5.25", WD2793 supports single, double, and high density drives, single-wide iSBX module.				Analog I/O board. High speed intelligent analog I/O.			
210A318 Amtelco				RBX428 Robotrol			
Floppy disk controller, 5- 1/4 or 8-inch single or double density, up to 4 drives, DMA or I/O operation				Analog input. IEEE P959 (SBX) analog input module 8 differential, 16 single-ended inputs programmable gain 12-bit resolution. 18 kHz sample rate.			
CBXFDC Comark				mSBX311 MicroIncls			
LAN Controller, 10Mbps IEEE 802.3 Ethernet compatible, 8 MHz 82586 LAN coprocessor, 16K Bytes of dual-parted buffer RAM, single-wide iSBX Multimodule.				Analog Input board. 16 single-ended/8 differential inputs with 12-bit resolution, 50 kHz throughput rate.			
iSBX586 Intel				RBX311 Robotrol			
SCSI bus controller, NCR53C90, supports up to eight devices, single-wide iSBX module.				Analog input module with 16 SE/8DI channels			
210A319 Amtelco				DTX311 DataTrans			
SCSI bus controller, WD33C93, supports up to eight devices, single-wide iSBX module.				Analog output module, 8-channel D/A			
210A305 Amtelco				DTX328 DataTrans			
Servo motor controller provides position proportional velocity, trapezoidal profile, and integral velocity control for up to two dc servo motors. Pulse/analog output control, 24-bit position counter and programmable interrupt control.				Analog output multimodule			
ZBX750 Zendex				mSBX328 MicroIncls			
Stepper motor controller. Controls any three, four, or five phase stepper motor in full/half-step modes. Maximum of 10,000 steps per second.				Analog to digital input and digital to analog output SBX module. Two 8-bit ADC and two 8-bit DAC. Full microprocessor interface and precision voltage reference.			
ZBX740 Zendex				ZBX324 Zendex			
Stepper Motor, programmable ramping, half stepping, pulse rate, home and emergency stop motion routines				Analog to Digital, 16 differential or 32 single-ended inputs 12-bit resolution			
4316 Tech80				CBX-AD832 Comark			
Video alpha-numeric controller provides either black and white or eight color displays in 7x9, 5x7 or 6x8 character fonts, on-board keyboard and light pen interface, 50 or 60Hz frame rate operation.				Bit serial communications multimodule, provides HDLC/SDLC half/full duplex communications channel for iSBX bus compatible microcomputers, supports one RS232C or RS449/442A interface, software programmable baud rate up to 64K baud.			
iSBX270 Intel				iSBX352 Intel			
Video graphics controller interfaces to either black and white or color display monitors on-board refresh memory supports 512x512 b&w or 256x256 eight color display resolution, drawing commands include line, arc, circle, rectangle, character, area fill, pan and scroll.				Centronics printer interface SBX module provides direct interface to Centronics compatible parallel printers. Generates data strobe and latches data.			
iSBX275 Intel				ZBX349 Zendex			
Four channel serial communications controller. RS-232, uses Zilog Z8530 SCC, double-wide iSBX module.				Digital I/O. IEEE P959 (SBX) parallel input/output 24 programmable lines with termination provisions.			
210A296 Amtelco				mSBX350 MicroIncls			
640 x 400 color graphics, on-board display controller executes graphics primitives.				Digital I/O module			
MSBX800 Matrox				DTX350 DataTrans			
<b>Converters</b>				Expands DTX311 to 64SE/32 DI channels			
A/D converter, 12-bit. Eight differential or 16 single-ended inputs. 5 $\mu$ s conversion rates.				DTX311EX DataTrans			
CDX-A/D-816 CompDyn				General purpose interface bus (GPIB) provides complete talker/listener functions as well as controller functions.			
				mSBX488 MicroIncls			
				GPIB controller interface with 300 Kbytes of DMA transfer speeds, listener and talker capabilities.			
				zSBX20 Ziotech			
				zSBX30 Ziotech			
				GPIB interface. Complete intelligent interface with standard protocol handled automatically through TI TMS-9914 GPIB adapter chip. Drivers available.			
				ZBX488 Zendex			
				IEEE-488 GPIB interface supplied with cable and MCS-80/85 or iAPX 86/88 software drivers.			
				$\mu$ DX488 MicroDesigns			
				IEEE $\pm$ 488 Hardware interface GPIB-SBX, handler available.			
				77606901 $\diamond$ NationalInst			
				Interrupt and timer expansion, 8 priority-encoded interrupts, three 16-bit counter/timers			
				MX501 Abionics			
				Multiple counter/timers, twelve 16-bit counter/timers, 9 buffered clock sources, buffered I/O to ribbon cable			
				MX502 Abionics			

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>iSBX</b>				<b>Mathematics</b>			
<b>I/O (Cont'd)</b>							
Parallel I/O board. 48 channels with Z80 mode interrupts. Direct connection to solid-state relay racks. Handshaking modes are implemented.	CDX-P48	CompDyn		Fixed/floating point math expansion 4MHz operation, fixed point single and double precision (16x32-bit), floating point double precision (32-bit), binary data formats.	iSBX331	Intel	
Parallel I/O board. IEEE-P959 (SBX) compatible. Employs 68230 PI, 16 bidirectional I/O lines with programmable timer.	PG3911	MicroInds		Floating point math expansion, 4MHz operation, single (32-bit)/double (64-bit) precision arithmetic and data manipulation commands, add, subtract, multiply and divide functions.	iSBX332	Intel	
Parallel I/O board. SBX module with 24 parallel lines, utilizes 8255A programmable peripheral interface.	ZBX350	Zendex		Floating point multimodule board	mSBC332	MicroInds	25
Parallel I/O multimodule, iSBX bus compatible expansion, 24 programmable I/O lines with sockets for interchangeable line drivers and terminators, three jumper selectable interrupt request sources.	iSBX350	Intel		Mathematics. IEEE P959 (SBX) fixed/floating point math module. Single or double precision.	mBLX331 mSBC331	MicroInds MicroInds	
Parallel I/O SBX module	CD24/8350	CentData	5	Numeric data processor	mSBC337	MicroInds	
Parallel, 24 programmable lines, bidirectional bus drivers	CBX-DI240	Comark		<b>Memories</b>			
Parallel, 48 programmable lines (two 8255As). Fully buffered, on-board configuration for easy centronics interface.	μDX548	MicroDesigns		Bubble memory, 128 Kbyte, automatic error correction, compatible with DMA controller, non-volatile storage.	iSBX251	Intel	
Serial, dual asynchronous RS-232 interface, software-selectable baud rates for each channel from 50 to 38.4K	MX301	Abionics		Stack-oriented memory and real-time clock with battery back-up. Intel iSBX compatible. Supports 8K, 16K, 32K, 128Kx8 RAM or EPROM devices. Seven different interrupt intervals. AM/PM or 24 hour formats. interrupt intervals. AM/PM or 24 hour formats.	CDX-MEM/CLOCK	CompDyn	30
Serial, dual RS-232 and RS-422 asynchronous interface, software-selectable baud rates to 38.4K	MX304	Abionics		<b>Multifunction</b>			
Serial I/O board. Dual synchronous or asynchronous, full-duplex channels. RS-232C or RS-422 interfaces with programmable baud rate.	mSBX354	MicroInds	10	Combination SCSI and Centronics interfaces. All features of SBSxCEN combined on one single-width SBX module.	SBSxSCSI/CEN	SingleBoard	
Serial I/O board. One RS-232C or RS-422 buffered USART channel. Programmable baud rate, includes two timer/counters.	mSBX351	MicroInds		GPIB multimodule has talker/listener functions including: addressing, handshake protocol, service request, serial and parallel polling schemes; controller functions include: transfer control, service requests and remote enable.	iSBX488	Intel	
Serial I/O board. IEEE-P959 (SBX) compatible. Two RS-232C channels with programmable baud rates up to 38.4 Kbaud.	PG3910	MicroInds		real-time clock, two synchronous/asynchronous serial ports, 2 Kbyte or 8 Kbyte CMOS RAM, battery backup.	μDX221	MicroDesigns	
Serial I/O board. SBX module provides single RS-232-C or RS-449/422 port via an 8215A USART. Two general purpose programmable 16-bit counter/timers.	ZBX351	Zendex		<b>Prototyping Boards</b>			
Serial I/O board. Two full duplex channels, programmable baud rates with extension to 614K baud.	SERX422	SBE		Board, expansion module	mBLX391	MicroInds	
Serial I/O multimodule, iSBX bus compatible I/O expansion, programmable synchronous/asynchronous communications channel with RS232C or RS4449/442 interface, software programmable baud rate generator, two programmable 16 bit BCD or binary timers/event counters.	iSBX351	Intel	15	Prototyping board. SBX module accepts any size DIP package. Power and ground traces provided with 153 prototyping points.	ZBX391	Zendex	35
Serial I/O SBX module. Two channel sync/async, HDLC, CCITT, SDLX, X.25, RS-232, RS-422/485, DMA capability and full speed operation. Hardware and software compatible with Intel SBX-354.	ZBX354	Zendex		Single width multimodule prototype board. All holes plated thru, holds up to 7-16 pin IC's or 1-40 pm, 2-14 pin and 4-16 pin IC's in combination 30 pm external connector.	BE00103	Bummer	
Serial SBX I/O module	CD24/8351	CentData		<b>Miscellaneous</b>			
Serial SBX module, dual-channel	CD24/3530	CentData		Clock/calendar, Battery-backed clock/calendar with date and time information for milliseconds through months	MX201A	Abionics	
Dual serial, asynchronous or bisynchronous bit-sync operation, two FDX transmitters, DMA	CBX-S1200	Comark		Clock/calendar, PC/AT compatible with 2Kx8 bytes of battery backed RAM.	MX202	Abionics	
Quadrature encoder input has a 16-bit counter for direction and position, synchronous clocking which prevents false counting in noisy environments.	ZBX760	Zendex	20	Clock/calendar SBX module provides seconds, minutes, hours, day of week, date, month and year. RMX utilities available.	ZBX348	Zendex	
Three-channel shaft encoder interface, 8031 processor based, triple 12-bit counters with TTL quadrature input, RS-485 serial channel	MX701	Abionics		SCSI interface utilizes NCR 5380. RMX, CP/M and concurrent DOS drivers available. Has header or edge connector. Optional CMOS version. Transfer rate up to 1.5 MB/s.	ZBX280	Zendex	40
Eight channel serial I/O multimodule board. RS-232C interface, baud rates programmable from 50 to 19.2K baud.	mSBX358	MicroInds					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>iSBX</b>							
<b>Miscellaneous</b>							
Single width iSBX bus interface card. SASI interface to disk and tape controllers. Also works with most SCSI controllers.	SASX	SBE		VT100 with AVO emulation and DLV-11 interface 80/132 column, 24 row, smooth scroll, non-volatile setup memory, true 75000 baud speed, on-board Z80, keyboard, auxiliary I/O parts, composite, separate video outputs. Dual size module.	TFL100	KSystems	
8 Output relay module, 1 byte command sequence, form "C" outputs.	MX901	Abionics		<b>Micro Bus</b>			
<b>LSI-11</b>				<b>Controllers</b>			
<b>Converters</b>				Parallel printer controller emulates 4221 line printer controller, optional 64 Kb buffer, Centronics interface.	DLP1	IntelComp	
High-speed high-resolution A/D	DT2757	DataTrans		<b>Memories</b>			
<b>Graphics</b>				Magnetic Tape Coupler, interfaces DG desktop generation to 1/2 inch tape drives equipped with an industry standard formatter, including streaming tape drives.	DMT1	IntelComp	
Video Inserter, IRIG Reader, Clock, Reticle Alphanumeric titling, time, crosswire/box reticle intertion into RS170, NTSC, CCIR video. IRIG reader sets on-board battery backup clock. Optional A/D inputs and binary video data insertion. Dual card.	VICCUR	KSystems		523 Kbytes increments through 2M total capacity dynamic RAM, 18 bits wide including parity.	DMM1	IntelComp	
Video Overlay. Dual module, Synchronizes CRT controller to incoming RS170/CCIR/NTSC. Supplies pixel clock to CRT controller. Inserts TTL video signals from CRT controller into video. Compatible with KTL-100, TFL-100.	VOQ	KSystems		<b>Micromodule</b>			
<b>I/O</b>				<b>I/O</b>			
Analog Input for simultaneous sample and hold	DT3368 DT3388	DataTrans DataTrans		5 Analog input subsystem, 32 single-ended, 16 differential inputs, 12-bit resolution.	RTI1230	AD	
Analog input subsystem, 32 single-ended, 16 differential inputs, 12-bit resolution.	RTI1250	AD		Analog input, 32 differential (64 single-ended), 2-channel output, 8-bit resolution.	MP7432-AO	Burr-Brown	
Analog output subsystem, four channels, 12-bit resolution.	RTI1252	AD		Analog output subsystem, four channel output, 12-bit resolution.	RTI1232	AD	
Combination analog subsystem, 16 single-ended, 8 differential inputs, 2-channel output, 12-bit I/O resolution.	RTI1251	AD		Combination analog subsystem, 32 single-ended, 16 differential inputs, two channel output, 12-bit resolution.	RTI1231	AD	
DMA analog input system	DT2752	DataTrans		<b>MS DOS 2.0</b>			
DMA Analog output system	DT2751	DataTrans		<b>Communications</b>			
Intelligent color graphics interface	DT2750	DataTrans		10 Telephone add-on personal telephone management system (card) that turns IBM PC compatibles or an XT into a sophisticated telephone recording and playback system. It will answer calls, distributor messages, automatically dial, call forward and can be remotely controlled. Requires 192K of RAM in a PC.	pc Dial/Log	CMCIntl	
QIC 2 Tape controller.	IS-QIC2	IntSolutions		<b>Memories</b>			
Simultaneous sample and hold	DT2758	DataTrans		15 Hard disk, tape and cartridge. Provides sub-system storage to IBM PC, XT and compatibles including Compaq, Columbia, Corona, Tava, Televideo 1605. Capacities of 10,15,31MB. 5MB removable cartridge media, or 1/4 tape in 25 or 55Mbyte capacity.	Targa I	CMCIntl	
Four Port Synchronous Modem Interface 4 bidirectional 2400bps/24000bps ports with DMA 120/240 bit message format with programmable sync. Dual size module with done and 1/2 done interrupts. Loss of sync, loss of clock indicators.	FPMI	KSystems		Hard disk, tape and cartridge. Same as Targa I except the unit can have two drives either one of which could be 10, 15, or 31MB hard disk with tape backup (25 or 55MB) or removable 5MB cartridge.	Targa II	CMCIntl	
5-1/2 inch Winchester (ST506 compatible) controller.	RL101	IntSolutions		Hard disk, tape and cartridge. Same as Targa II with expansion slots available for adding up to 5 additional IBM PC compatible cards.	Targa III	CMCIntl	
<b>Memories</b>				<b>Miscellaneous</b>			
RAM, (dual ported) 512 Kbyte to 1 Mbyte, or 1, 2 and 3 Mbyte versions.	IS-68XM-XXX	IntSolutions		Piggyback board for both NMOS/CMOS TLCS-42 microcomputer evaluation system.	BM4211	Toshiba	
<b>Miscellaneous</b>				Piggyback board for TLCS-47 NMOS microcomputer version with 4096x8 external ROM and 256x4 RAM.	TMP4799C	Toshiba	
CRT emulator. Complete VT100 with AVO emulation 80/132 column, 24 row, smooth scroll, non-volatile setup memory, true 19200 speed, on-board Z80, keyboard, serial I/O ports, composite or separate video outputs. Dual size module.	KTL100	KSystems					
IRIG-B synchronizable reader/generator, event register, propagation delay correction, FIFO bus interface, AGC, auto-polarity, Dual size module, 1 microsecond accuracy on-time rate and frequency outputs.	AITG	KSystems					
Programmable real-time clock board	DT2769	DataTrans					

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‡ High Radiation Resistance

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus</b>							
<b>Communications</b>							
Communications Controller, High performance terminal I/O, intelligent 8-channel single board computer for asynchronous terminal control applications, on-board firmware, 128K Bytes zero, wait-state DRAM, 8MHz 80186 microprocessor, RS232 support on 8 channels, driver support from the Intel RMX and Xenix operating systems.	iSBC548	Intel		Controller, multifunction, supports ST506 disk drives, QIC-02 1/4" tape drives and SA-400 floppy disks. Disk data rates up to 512 Kbytes/sec. DMA up to 2.5 MB/sec. Separate data path architecture allows simultaneous transfers from Winchester disk and either tape or floppy. Automatic ECC correction, programmable DMA throttle. Drivers for Xenix and RMX-86 available.	431	Xylogics	
Communications Controller, Eight channel general purpose, 256K Bytes DRAM, sockets-for 128K bytes of PROM expandable to 192K Bytes with S8C341 Multimodule, 8MHz 80188 microprocessor, on-board firmware for terminal control applications, 2 iSBX Bus connectors, RS232C on 6 channels, RS232C or RS422A/RS449 on 2 channels.	iSBC18856	Intel		Disk subsystem. Two 3.5 inch floppy disk drives mounted on Multibus I card. On-board floppy disk controller.	ZX735i	Zendex	
Intelligent communications controller for IEEE-796 bus computers. CSMA/CD protocols, on-board CPU and communications management firmware.	NIB100/02	Destek		DMA board for high speed transfer of 8 or 16 bit data. Controls actual transfer of up to 65,536 words of data between memory and an external device.	MIB501A	MicrolInds	20
Intelligent Ethernet controller for Multibus systems. Uses 80186 or 80286CPU. Up to 512 KB RAM, supports TCP/IP Internet protocols.	EXOS201 EXOS301	Excelan Excelan	5	DMA for up to 330 Kbytes	mSBC501	MicrolInds	
Maximum GPIB data transfer rate of 1 Mb/s, 2Kbyte dual port RAM mappable anywhere in 1 Mb memory space.	mBLC8488	MicrolInds		Double density diskette controller to interface and iSBC to a double density flexible disc drive. Soft sectored format allowing 500 Kbyte data storage capacity per double density diskette. DMA logic.	mSBC202	MicrolInds	
Serial communication controller, 8/16 channels, up to 56k baud full duplex. On board firmware supports UNIX terminal I/O.	COM16	Microbar		Double density floppy disk	mBLC8222 mBLC8224	MicrolInds MicrolInds	
Ties systems together at 2 Mb/s data rates. Used with twisted pair to 400 feet, broadband/baseband coax to 5 miles, T1 and satellite links.	WNC5190	Interphase		Ethernet/IEEE 802.3 communications controller with TCP/IP and XNS protocols	NP300	Micom Int	25
USART, RS232C.	MS534	Comark		Ethernet/IEEE 802.3 data link controller, DMA capability	NI3210A	Micom Int	
Four-channel asynchronous/synchronous full-duplex serial controller. Supports RS-232, RS-423, RS-485, or RS-449, up to 1.5 Mb/s data rate.	LSBX-SERIAL/4	CompModules		Ethernet/IEEE-802.3 data link controller, 8-Kbyte dual-port RAM, on-board DMA controller, byte swap facility, diagnostic and software support provided	NI3210	Micom Int	
Four-channel RS-232 serial communications card using Zilog 8530 (SCC). Baud rates from 50 to 19.2K, optional clock/calendar function.	210A262	Amtelco		Ethernet intelligent controller with 80186 microprocessor, DMA capability, TCP/IP transport protocols.	EXOS201	Excelan	
4-channel multiprotocol serial comm. board, each channel can be independently configured to be RS232C, RS422, RS423, or RS485, S/W drivers available, double-wide SBX module.	LSBXSERIAL4	CompModules		Floppy disk controller. For four double sided standard 8" or three 5.25" drives, with 48 KB of dual-ported DRAM with DMA.	ZX209	Zendex	
<b>Controllers</b>				Floppy disk controller. Single/double density, up to four single sided 8" drives, ISIS II compatible.	ZX200A	Zendex	30
1/2-inch magnetic tape, DMA, IEEE 796 addressing	MT86	Comark		Floppy disk controller. Single or double density, up to 4 drives with 8 surfaces.	mBLX218	MicrolInds	
1/2-inch magnetic tape, 20-bit memory mapped	MT80	Comark		Floppy disk controller for up to four drives. Controls single and double density disk drives. Compatible with SA1000 floppy disk interface (industry standard).	SECS80/208	Titan/SESCO	
Color Graphics Display Processor. 640x480x8 pixel, 4096 color look-up table, draws at 10 K vectors/second.	SX900	Matrox		Floppy Disk controller, fully SBC-208 compatible. Controls up to four 8" or 5 1/4" single/double sided, single/double density FDDs.	ZX208B	Zendex	
Controller, high performance disk controller, SMD disk interface supports data rates up to 2.4MB/sec., DMA up to 3.0 MB/sec., 8 Kbytes FIFO buffer, automatic ECC correction, programmable DMA throttle. Drivers for Xenix and RMX-86 available.	451	Xylogics		Floppy drive card. Contains two 3.5" floppy disk drives, 2 MB of unformatted storage, IBM 3740 and SYS 34 formats, programmable sector lengths, supports DMA or non-DMA data transfers, available with or without controller.	ZX7XX	Zendex	
Controller, multifunction, supports ESDI disk drives, QIC-02 1/4" tape drives and SA-400 floppy disks. Disk data rates up to 1.2MB/sec. DMA up to 2.5MB/sec. Separate data path architecture allows simultaneous transfers from Winchester disk and either tape or floppy. Automatic ECC correction, programmable DMA throttle. Drivers for Xenix and RMX-86 available.	432	Xylogics		GPIB, polled or interrupt driven, 50 kHz transfers	42-009	Anasco	35
				Graphics display controller, NEC 7220, 80186 display list processor, 1024x1024x4 pixels, 16 color, 4096 color look-up-table, light pen interface, one RS232C.	GDC186	InnovRes	
				Hardcopy peripheral device controller for any Versatec-compatible or Centronics-compatible plotter/printer, including laser printers and color copiers.	10085	IKON	
				High performance disk controller, SMD disk interface supports data rate up to 2.0 Mbytes/sec (enhanced SMD), DMA up to 3.0 Mbytes/sec, 2 Kbytes or 8 Kbytes FIFO buffer, automatic ECC correction, programmable DMA throttle. Drivers for XENIX and RMX-86 supplied.	450	Xylogics	

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus</b>							
<b>Controllers (Cont'd)</b>							
High performance tape controller, Pertec formatted interface, supports tape speeds from 12.5 ips. to 200 ips; densities of 800, 1600, 3200, and 6250 fcbi; DMA data rate up to 2.8 Mbytes/sec, supports either start/stop or streaming tape drives. Drivers for XENIX and RMX-86 supplied.	472	Xylogics	5	SBX module, SCSI controller, NCR 5380	SBX380	Systek	20
High-speed controller with on-board DMA and dual ported memory (64Kbytes). No DMA support is required from system CPU board.	ZT87	Ziatech		SCSI bus controller supporting up to 8 devices, S/W drivers available, single-wide SBX module.	LSBXSCSI	CompModules	
High-speed GPIB controller, on-board DMA, 500 kHz transfer	42-008	Anasco		Supports ESDI and ST506 Drives, QIC-02, Tape, Floppy, M68000 Virtual Buffer architecture, Intelligent Caching plus Zero Latency Operation, Concurrent Disk and Streaming Tape, Simultaneous Disk and Bus Transfers.	STORAGER	Interphase	
IEEE-488 (GPIB) controller supporting up to 15 talkers/listeners, GPIB cable included, S/W drivers available, single-wide SBX module.	LSBX488	CompModules		Supports ESDI disk drives, floppy disks and QIC-02 1/4-inch tape drives. Track cache, ECC. Software compatible with iRMX-286, Xenix-286.	SMS8009	SMS	
Intelligent color video controller	CD21/7052	CentData		Supports ST506 Winchester, floppy disks and QIC-02 1/4-inch tape drives. Track cache, ECC. Software compatible with iRMX-286, Xenix-286.	SMS8007	SMS	
Intelligent Ethernet controller for Multibus systems. 80186 or 80286 CPU, up to 512 KB RAM, supports TCP/IP Internet protocols.	EXOS301	Excelan	10	Supports 2 SMD or SMD-E drives; 24 MB/s data rates, Intelligent Caching, 1:1 Interleave, Very high-speed DMA with throttling, Bad media mapping.	SMD2190	Interphase	25
Intelligent floppy disk controller, controls 4 5 1/4" and 8" floppy disk drives concurrently.	CD21/4130	CentData		Video Monitor/Keyboard Controller.	mBLC8228 mBLC8229	MicroInds MicroInds	
Intelligent networking, one Mb/s DMA transfer rate on fiber or coax in SDLC protocol. Up to 99 other stations on LAN.	LM-1	Computrol		VMEbus system controller printer port, calendar clock, iSBX connector, and up to 128K of battery backed RAM	OB68K/VSRM	Omnibyte	
Intelligent RS-422 communications controller, 8 serial channels, on-board processor with DMA interface to Multibus, independent baud rates up to 880K, HDLC/SDLC/Async, transient suppression optional.	MX422	Morrow		Winchester disk interface, compatible with ST506 (industry standard). Controls up to four Winchester disk drives, on-board PLL data separator assures integrity of data.	SECS80/506	Titan/SESCO	
Interface between Multibus-compatible computers and any QIC-02 compatible 1/4-inch streamer tape transport.	STC4400	Systech		Single board controller for up to two 5 1/4" ST506 Winchester drives, two SA850-type 8" floppy drives, and one QIC-02 1/4" cartridge tape drive.	MC6217B	Qualogy	
LAN Controller, 10 Mbps IEEE 802.3 Ethernet compatible 6MHz 80186 microprocessor, with 82586 LAN co-processor, 128K Bytes of dual-ported RAM expandable to 256K Bytes, two RS-232C and RS-422A/RS-449 compatible serial interfaces, two iSBX bus connectors, supports on-board execution of Intel ISO 8073 Transport and higher layer of communication software such as RMX-NET.	iSBC18651	Intel	15	Single-board controller for up to two 5 1/4" ESDI Winchester drives, two SA400-type 5 1/4" floppy drives, and one QIC-02 1/4" cartridge tape drive.	MC5317	Qualogy	30
LAN Controller, 10 Mbps IEEE 802.4 MAP compatible, 8MHz 80186 microprocessor, 256K Bytes of RAM, One iSBX Bus connector, supports on-board execution of Intel's Layer 3-7 MAP software, high performance dedicated LAN front-end for Multibus systems, off-loads host CPU from communications task.	iSBC554	Intel		Single-board controller for up to two 5 1/4" ST506 Winchester drives and two SA400-type 5 1/4" floppy drives.	MC5214 MC5217B	Qualogy Qualogy	
LAN Controller, 10Mbps IEEE 802.3 Ethernet compatible, 8.MHZ 80186 microprocessor with 82586 LAN co-processor, 256K Byte zero wait-state DRAM, supports on-board execution of Intel ISO 8073 transport and ISO 8473 Network software, high-performance dedicated LAN front-end for multibus systems, off-loads host cpu from communications task.	iSBC552A	Intel		Dual-channel Versatec printer/plotter, one channel supports the Versatec printer/plotter while the second channel supports any standard Centronics or Dataproducts printer	VPC2200	Systech	
Magnetic tape controller for 1/2 inch tape units, DMA circuitry for full 24-bit addressing range	HTC4000	Systech		Dual-port line printer/controller. Interface between Multibus-compatible computers and any Centronics or Dataproducts line printer	MLP2000	Systech	
Motor control interface card, 12-bit D/A, encoder interface with marker decoding logic	9702	NCAI		Four multi-protocol serial communications channels, full duplex DMA operation on all four channels, up to 512 Kbytes of zero wait-state RAM with parity.	DCP8804	Systech	
Multi-media controller.	CD21/4300	CentData	15	Four-channel video controller with EIA RS-170 compatible output	210A212	Amtelco	35
Priam Disk Plus Card provides access for up to 4 Priam Winchester disk drives via the Priam Smart E controller	210A171	Amtelco		1 or 2 axis programmable motion controller, controls position, velocity, or torque, communicates via Multibus or RS-232, motion sequence may be stored in memory	DMC200	Galil	
QIC-02 Cartridge tape controller	CD21/4029	CentData		8- or 5- 1/4-inch, single or double-side, double-density, IBM compatible	MF85	Comark	
				1024x768 color graphics processor, 256 colors from 4096 color look-up table.	GXB1000A	Matrox	
				5 1/4" Floppy disk controller	CD21/4055	CentData	
				512x512x8 Image processor, includes software image processing subroutine library.	MIP512	Matrox	40
				8-inch Double density floppy disk controller	CD21/4015	CentData	

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus (Cont'd)</b>				Video pixel processor board. Operates on 16 bit data at 10.08 MHZ. Enables real time operations such as frame integration and summation, background subtractions, consultations and filtering. The processor can be programmed to perform 2 different operations in a single pass through the image data. Processor cascading is possible for higher performance system. The PX-501M is compatible with the AS-501M I/O board and the DS-501M digital storage unit.			
<b>Converters</b>				PX501M	Recognition		
A/D and D/A converter. 12-bit resolution with 0 to 500 kHz sample rates, buffer memory included.	MADA	DSP-Systems		Single-board real-time image processor with 512x512x8 resolution. Holds four images, split-scan mode, driver software.			
High-level A/D converter	DT711	DataTrans		Series 100	Imaging		
	DT712	DataTrans		Single-board triple frame buffer with ALU in hardware.			
	DT772	DataTrans		MINIVIDEO	Datacube		25
High-level A/D expansion board for DT712	DT713	DataTrans	5	<b>I/O</b>			
Low-level A/D converter	DT714	DataTrans		Analog board			
	DT774	DataTrans		DT732	DataTrans		
Low-level A/D expansion board for DT714	DT715	DataTrans		Analog I/O board with memory: 32 single ended/16 differential channels. No output channels. Programmable gain amplifier.			
SBX module, 8 channel A/D, 8 channel D/A, 8-bit resolution	SBX408	Systek		MIB8737-1	MicroInds		
SBX module, 16-channel A/D, 12-bit resolution, instrumentation and programmable gain amplifiers	SBX412	Systek	10	MIB8737-3	MicroInds		
Two 16-bit synchro/resolver-to-digital converters and one 16-bit digital-to-synchro/resolver converter.	5401C	Transmag		Analog I/O module with 32 single-ended/16 differential A/D input channels. Two 12-bit D/A output channels. Includes sample and hold, and programmable gain amplifier.			
Three 12-bit resolver-to-digital converters including a turns counter.	5401C-22	Transmag		SECS80/732	Titan/SESCO		
Three 16-bit digital-to-synchro converters or digital-to-resolver converters.	5401C-14	Transmag		Analog I/O with 16 differential or 32 single-ended inputs, programmable gain, 12 analog outputs with 12-bit resolution			
Three 16-bit synchro/resolver-to-digital converters or resolver-to-digital converter.	5401C-17	Transmag		RMB741	Robotrol		30
Three-channel resolver-to-digital converter. The board gives position and turns count data which is formatted into three 8-bit bytes per channel and transferred via Multibus signals.	DDC35500	ILC-DDC	15	Analog input expander, 48 differential, 96 single-ended analog input channels (must be used with MP8418 series).			
13 Bit Multi-Channel D/A output card.	NPC1300	Northern		MP8418-EXP	Burr-Brown		
<b>Graphics</b>				Analog input/output, 8 channels			
Acquisition, storage and display for machine vision, factory automation, medical imaging, and teleconferencing.	VG128	Datacube		mBLC8737-3	MicroInds		
Family of seven mix and match boards allows users to perform advanced image processing operations in hardware, such as convolutions, histogram equalization, feature extraction, and arithmetic and logic operations.	IP512	Imaging		Analog input system, (16 single-ended or 8 differential), (32 single-ended or 16 differential) or (64 single-ended or 32 differential) channels.			
Graphics/Video display controller. 1Kx1K bit-mapped, available in color or black and white. Graphics software library available.	ZX1000	Zendex		DT1742	DataTrans		
Real-time image acquisition and signal processing. Contains complete alpha-numeric display as well as pan, zoom, and scroll features.	VG123	Datacube	20	Analog input, 8 channels			
Video input and video output board. Accepts up to 4 camera and VCR inputs. 512x512 resolution. Features include programmable gain, offset, and look up tables. Compatible with the DS-501M digital storage unit and FX-501M pipeline pixel processor.	AS501M	Recognition		mBLC8737-1	MicroInds		
Video memory board. Accepts a 512x512 array of 8 bit image data and stores it as a 512x512x9 image. The 9th bit is used for extra features such as graphics overlay, pixel protection and conditional processing control. Scroll and pan is available on a per pixel basis. System is available memory mapped or register accessed from Multibus and with one or four frame stores per board. The DS-501M is compatible with the AS-501M I/O board and the PX-501M pipeline pixel processor.	DS501M	Recognition		Analog input, 15 channel differential, 31 channel single-ended, resistor-programmable gain, 12-bit resolution.			
				MP8418	Burr-Brown		35
				MP8418-AO	Burr-Brown		
				Analog input, 15-channel differential, 31-channel single-ended, 12-bit resolution, software programmable gain.			
				MP8418-PGA	Burr-Brown		
				MP8418-PGA-AO	Burr-Brown		
				Analog input, 16-channel RTD input digitizer, excitation resistor compensation, 12-bit resolution.			
				MP8430	Burr-Brown		
				Analog input, 16-channel, 1000 V transformer isolated, 12-bit resolution.			
				MP8450	Burr-Brown		40
				Analog input, 32 single-ended/16 differential channels, 12-bit resolution, programmable gains of 1, 2, 4, and 8			
				41-010	Anasco		
				Analog input, 32 single-ended and 16 differential inputs, programmable gain, 12-bit resolution			
				RMB725	Robotrol		
				Analog output board			
				DT724	DataTrans		
				Analog output expansion modules, single channel of digital to analog conversion, 10-bit resolution, concurrent voltage and current modes.			
				mBLX321	MicroInds		
				Analog output module. Four 12-bit D/A channels with on-board DC-to-DC converter.			
				SECS80/724	Titan/SESCO		45
				Analog output subsystem with four analog outputs that can be user configured.			
				ITGII21	Analogic		
				Analog output, 4 channels, 12-bit resolution			
				41-011	Anasco		

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus</b>							
<b>I/O</b>							
<b>(Cont'd)</b>				Intelligent high-isolation A/D, 8 differential, 12-bit resolution.	41-025	Anasco	
Analog output, 16 channels, 12-bit resolution, high-level inputs.	MP8316-V	Burr-Brown		Intelligent high-speed A/D, 32 single-ended/16 differential, 12 or 14-bit resolution, up to 132 kHz throughput.	41-036	Anasco	
Analog output, 12-bit resolution	RMB710	Robotrol		Intelligent isolated A/D, 16 differential inputs, 12 or 14-bit resolution, on-board linearization and CJC, RS-422, 1 kV isolation.	41-020	Anasco	30
Analog subsystem combination, 32 single-ended, 16 differential analog inputs, two analog outputs, 12-bit resolution.	RTI732	AD		Intelligent isolated analog subsystem, 8/16 differential inputs, 14-bit resolution, 2 analog outputs, on-board linearization and CJC, RS-422, 1 kV isolation	41-022	Anasco	
Analog subsystem, four analog-output channels, 12-bit resolution.	RTI724	AD		Intelligent octal serial interface.	CD21/3044	CentData	
Analog subsystem, 32 single-ended, 16 differential analog-input channels, 12 bit resolution.	RTI711	AD	5	Intelligent SCSI host adapter permits host-to-peripheral and host-to-host communication.	ADP32	NCR	
Combination analog subsystem, 32 single-ended/16 differential inputs, programmable gains of 1, 2, 4, and 8, 2-channel output, 12-bit resolution	41-012	Anasco		ISBX Motherboard with 6 connectors, 4 having DMA.	ZX564	Zendex	
Current loop adapter provides current loop conversion for RS232C I/O channels, extends series/80 capability.	mBLC530	MicroInds		Isolated A/D expansion multiplexer, 8 single-ended/16 differential. Expandable to 128 DI.	41-023	Anasco	35
Digital I/O, 72 lines, solid-state I/O compatible.	41-014	Anasco		Isolated analog input system, 4 differential channels.	DT1748	DataTrans	
Digital Input and Output. Intelligent card with 32 bits output, 32 bits input, 8 control lines out, and 8 control lines in.	53210100	Inventive		Isolated analog input, 16 differential channels, 12-bit resolution, programmable gains of 100mV to 10 V isolation	41-015	Anasco	
Digital input, 5 channels, isolated, time measurement.	MP821-05	Burr-Brown	10	Low level analog input, (16 single-ended or 8 differential), (32 single-ended or 16 differential) or (64 single-ended or 32 differential).	DT1744	DataTrans	
Digital input, 15 channels, isolated, time measurement.	MP821-15	Burr-Brown		MIL-STD-1553 remote terminal or bus controller interface module. Requires CPU and memory with 16-bit word transfer capability.	SECS80/1553	Titan/SESCO	
Digital output, 16 channels, isolated, relay output.	MP801	Burr-Brown		Multi-channel communications controller, interfaces eight terminals or modems to IEEE-796, RS-232C port, programmable baud rates up to 19.2K baud.	MTI850/1650	Systech	40
Digital output, 32 channels, isolated relay output.	MP802	Burr-Brown		Multibus II to MIL-STD-1553 interface. Central computer and remote terminal simulation. 1553 bus tracer and analyzer.	MIBII 1553	MicroInds	
Digital to analog output, 8-channel 12-bit or 4-channel 12-bit.	DT1842	DataTrans		Multibus-I to Multibus-I adaptor.	421	Bit3Comp	
Digital-to-analog output, 8-channel 8-bit or 4-channel 8-bit.	DT1843	DataTrans	15	Multibus-I to VME bus adaptor.	422	Bit3Comp	
Disk Subsystem. Two 3.5 inch floppy disk drives mounted on Multibus I card.	ZX735	Zendex		Optically isolated interface with 24 parallel lines	mBLC556	MicroInds	
Emulation of DEC DR11-W high-speed parallel DMA interface for use as interprocessor link or general purpose peripheral device interface. 2M byte/second transfer rate.	10077	IKON		Parallel and serial I/O module for 386 or other high density SBC. Includes three 8-bit parallel ports and two high speed multi-protocol serial channels.	LSBX386I/O	CompModules	45
Expansion board. Independently controlled 8 bit parallel ports, interrupts for reduced system overhead control, automatic input port interrupt (8 external available), switch selected port address, variable-width strobed outputs.	mBLC508	MicroInds		SBX module, quad UART, RS-232, DTE/DCE, CMOS	SBX301	Systek	
GCR tape drive interface provides a DMA type interface between Multibus based computer systems and a telex interface compatible formatter—can interface with up to 4 tape drives.	4100	MTC		SBX module, 24 parallel lines, six counter/timers, Centronics compatible	SBX224	Systek	
High Performance FIFO-Buffered version of Model 10077-NSC.	10091	IKON		SCSI interface on ISBX module utilizes NCR 5380 RMX drivers availab	ZBX280	Zendex	
High performance version of Model 10077 FIFO-buffered, 4M byte/second transfer rate.	10087	IKON		SCSI interface plus clock/calendar on ISBX module, utilizes NCR 5380 & OKI MSM 624 RS. RMX Drivers available.	ZBX288	Zendex	
High-level analog-to-digital output, 16 single-ended or 8 differential channels.	DT1751	DataTrans		Serial communications, allows up to eight RS-232 channels, eight 20mA current loop channels, four RS-422/449 channels, or a combination	CD21/3088	CentData	50
IBM PC to Multibus Adaptor.	404	Bit3Comp		Serial I/O board. Five 8215's provide five channels of serial I/O.	ZX515	Zendex	
IEEE-488 Hardware interface GPIB-796 DMA I/O, handler available.	77606601	NationalInst		Simultaneous sample and hold for high-level, single-ended analog inputs	DT778	DataTrans	
IEEE-488 Hardware interface GPIB-796 P-1 program I/O handler available.	77606701	NationalInst	25	Smart communications controller with 16 channels of serial RS-232 ports using an on-board Z-80 processor.	210A20B	Amtelco	
Industrial distributed I/O controller for factory automation, up to 1024 I/O points controlled by 2 wires at 307.2 Kbaud	6-SBX/N	Digitronics		Dual channel serial I/O on ISBX module. Utilizes 8251A.	ZBX361	Zendex	
Industrial I/O controller for factory automation	6-SBX/IO	Digitronics		Dual channel serial I/O with HOLC/SDLC protocol. Runs at full speed. Upgrade of Intel ISBX-354.	ZBX354	Zendex	55
				Quad serial interface	CD21/3038	CentData	
				Octal serial interface.	CD21/3043	CentData	

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

\*Macrocell

Bold face indicates additional data is provided on the page noted.



## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus</b>							
<b>I/O</b>							
<b>(Cont'd)</b>							
Two printer ports and 4 RS-232 serial ports	OB68/MPSIO	Omnibyte		Disk cache, 500 Kbyte cache and 196K byte print spooler supports up to 4 double density floppy drives. Works in conjunction with Intel, National and Zendex controller boards.	OR88C	Origin	25
Four serial ports, printer port, SASI interface, calendar clock with battery backup	OB68K/INT-S	Omnibyte		DRAM expansion module. Up to 128 KB with built-in error correction and detection. Internal or external refresh control.	SECS80/028	Titan/SESCO	
Eight channel intelligent serial I/O board. Achieves 9600 baud full duplex operation on all eight channels.	CD21/3100	CentData		DRAM expansion module, up to 256 KB with built-in error detection and correction. Internal or external refresh control.	SECS80/056	Titan/SESCO	
Eight RS-232/RS-423 serial ports	OB68K/OCTAL	Omnibyte		Dynamic RAM board, 128K-2Mb EDC.	CD21/2700	CentData	
Eight RS-232 serial ports	OB68K/MSIO	Omnibyte	5	ECC RAM board, up to 256 Kbytes	mSBC028A	Microlnlds	30
2 Channel 14 Bit resolver/inductosyn converter with 16 bit DAC.	NPT1602	Northern		ECC RAM board, up to 512 Kbytes	mSBC012C	Microlnlds	
16 channel intelligent serial I/O board. Achieves 9600 baud full duplex operation on all 16 channels.	CD21/3116	CentData		EPROM multimodule board, 28-pin sockets	mSBC341	Microlnlds	
48 lines of parallel I/O, print port, SASI interface, calendar clock with battery backup	OB68K/INT-P	Omnibyte		EPROM/RAM/EEPROM board with real-time clock/calendar.	CD21/2035	CentData	
72 Channel input/output board. Programmable monitor using 8741A.	ZX572	Zendex		EPROM/RAM module. RAM only capacities to 512 KB, EPROM to 1 MB. 24-bit addressing, maps into 16 MB address space.	SECS80/164A	Titan/SESCO	
72 Channel programmable parallel I/O board.	ZX560	Zendex	10	Expansion board, up to 128 Kbytes	mSBC056A	Microlnlds	35
72-Channel TTL I/O with Output Readback	MP830-72	Burr-Brown		Expansion board, up to 32 Kbytes	mSBC032	Microlnlds	
72-line parallel I/O. On-board interval timer and eight maskable interrupts.	SECS80/519	Titan/SESCO		Expansion board, up to 64 Kbytes	mSBC064	Microlnlds	
96 lines of parallel I/O	OB68K230	Omnibyte		Expansion board, 64-Kbyte EPROM	mSBC464	Microlnlds	
<b>Mathematics</b>				Expansion module: 256 Kb RAM which augments PM68K single board computer.	MXK	PacificM	
Array processor, capable of performing integer and floating-point math, 8 MOPS. Extensive software libraries available.	APB3024M	Marinco		Expansion module: 756K or 1, 3, 4 Mbytes, dual-ported RAM augments PM68D Single Board Computer.	MXD	PacificM	
Fixed point array processor, 12 MOPS, 50-kHz real-time bandwidth.	43-100	Anasco	15	Fast 200 ns read access, data protected by byte parity, Multibus compatible with 24 bit addressing & 8/16 bit data paths—1Mb RAM Bd w/parity.	ZBC010P ZBC012P ZBC020P	Zitel	40
High speed math unit; fixed point integer arithmetic, 16 and 32 bit format. Floating point arithmetic. Compare and test operation relative to floating point constant. Float to fix and fix to float conversions. Multimaster access.	mSBC310A	Microlnlds		For PDP 11/73, 11/83, and 11/84. Full PMI support, single-bit error correction, double-bit error detection, 4MB, battery back-up.	CIPMI-EDC	Chrislin	
Numeric data processor provides high speed fixed and floating point functions for iSBC86/88, and iAPX86/88 systems, supports seven data types including single and double precision integer and floating point.	iSBC337A	Intel		High performance LBX design, Fast 190ns maximum LBX read access, Byte parity error detection, 16M addressing ability, 1Mb dual port RAM bd w/parity.	ZBC010PX ZBC012PX ZBC020PX ZBC040PX	Zitel	45
Transformation Processor (Floating point processor for graphics applications)	WTE5300	Weitek		Interfaces up to four Sundstrand SETS-I or SETS-II tape recorders. 48K bps transfer rate using phase encoding.	SECS80/TC1	Titan/SESCO	
Twelve MOP array processor for Multibus I.	AP4	DSP-Systems		LBX 512K to 2 Mbyte parity-checking dynamic RAM board	CD21/2510	CentData	
<b>Memories</b>				Memory board with 256 KB of RAM and error checking capability.	ZX056N	Zendex	50
Bubble memory card, 128K to 256K, on-board processor with DMS to Multibus, power conditioning. Includes software to implement a complete file structure.	BM256	Morrow	20	Memory board with 512 KB RAM, parity checking.	ZX012QA	Zendex	
Bubble memory controller, interfaces to Miitope Militarized Bubble System (BMS1000) or Intel IBCK. On-board DMA controller (8089).	SECS80/BMC	Titan/SESCO		Memory Management Unit (MMU) for GPC68020.	MM86	Microbar	
CMOS RAM 4 Kbytes memory/battery backup board. Base address selectable to start on any 4K memory address boundary. On board rechargeable batteries and charging circuitry.	mSBC094	Microlnlds		Multibus Memory expansion with Error Detection and Correction—512Kbyte RAM board with ECC.	ZBC012E ZBC10E	Zitel	55
CMOS SRAM memory board. Battery backed-up, dynamically relocatable memory. Supplied with 0, 1, or 4 MB CMOS SRAM.	ZX091	Zendex		Multimodule, 4-Kbyte RAM	mSBC301	Microlnlds	
Detects and Corrects all Single-Bit data errors. Multibus Memory Expansion with Error Detection and Correction—2Mb RAM board with ECC.	ZBC0202	Zitel		Multimodule, 128-Kbytes ECC RAM	mSBC304C	Microlnlds	
				Multimodule, 512-Kbytes RAM	mSBC314	Microlnlds	
				Output features: 96 Discrete open collector outputs, resident diagnostics.	S80 OUTPUT	Babcock	
				Programmable RAM/EPROM and I/O board.	CD21/5232	CentData	

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\*Typical Value

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus</b>							
<b>Memories</b>				<b>(Cont'd)</b>			
PROM/ROM expansion board. 16K to 128K capacity, address assignable anywhere within 16M byte memory, switch selectable minimum access time from 35ns to 1435ns, operation in 8 or 16 bit mode.	mBLC464	MicroIncls	5	64 Kbyte dynamic RAM, 8 or 16 bit jumper selectable, on-board refresh.	rMEM64K-D	RELMS	35
RAM Memory Board, 32K.	mBLC032B	MicroIncls		64-Kbyte dynamic RAM expansion for 8- and 16-bit bus masters; odd/even parity checker.	rMEM64K-BE	RELMS	
RAM Memory Board, 64K.	mBLC064A mBLC064B	MicroIncls MicroIncls		64-Kbyte RAM	mBLC064 mBLC064A	MicroIncls MicroIncls	
RAM with ECC, 512 Kbytes to 2 Mbytes	DSB020EL	Den/Pas		96 Kbyte dynamic RAM, 350-ns access, hidden refresh, 4 K bank disable, parity, 8/16 bit operation, on-board 5V generation, 24-bit addressing.	MR85-096	Comark	
RAM with parity and iLBX/HSI interface	DSB020PL	Den/Pas		128 Kbyte dynamic RAM, hidden refresh, 16 K bank disable, parity, 8/16 bit operation, on-board 5V generation, 24-bit addressing.	MR86-128	Comark	40
RAM with parity, 512 Kbytes to 2 Mbytes	DSB020	Den/Pas	10	128 Kbyte dynamic RAM, hidden refresh, 4 K bank disable, parity, 8/16 bit operation, on-board 5V generation, 24-bit addressing.	MR85-128	Comark	
Universal byte-wide memory card, space for 32 memory devices including RAM, PROM, and EPROM in combination.	210A211	Amtelco		128-Kbyte EPROM, addresses between 2 and 128 Kbytes, 24-bit address decoding	CD21/2014	CentData	
Up to 256 Kbytes CMOS RAM, EPROM 16, 32, 64, 128 or 256K bit devices, maximum capacity 1 Mbyte, RAM/EPROM mix, battery backup, 8/16-bit data, 24-bit address, real-time clock.	PSM6663	Plessey		128-Kbyte RAM	mBLC0128A mSBC028CX	MicroIncls MicroIncls	
Dual Port Ram 256K-1MB global memory.	DBR50	Microbar		256 Kbyte dynamic RAM expansion for 8- and 16-bit bus masters, on-board transparent refresh or scheduled refresh.	rMEM256K-BE	RELMS	
1 Mbyte to 4 Mbyte dynamic RAM.	CD21/2110	CentData	15	256-Kbyte dynamic RAM, hidden refresh, 16 K bank disable, parity, 8/16 bit operation, on-board 5V generation, 24-bit addressing.	MR86-256	Comark	45
1, 2, 4, and 8 MB expansion memory modules for iSBC 386/2x, iSBC 386/3x, iSBC 386/116 and iSBC 386/120 series of Multibus I and II CPU boards.	iSBC MM01 iSBC MM02 iSBC MM04 iSBC MM08	Intel Intel Intel Intel		256-Kbyte dynamic RAM, transparent refresh or off-board control, parity error detection, 8/16-bit data, 20/24-bit addressing	44-102 44-112	Anasco Anasco	
2 Kbyte DRAM, single- and double-bit error detection, single-bit correction.	CI796-EDC-2MB	Chrislin		256-Kbyte RAM	mBLC0256B mSBC056CX	MicroIncls MicroIncls	
2 Mbyte DRAM, on-board parity generator/checker and error status register.	CI8086 + 2MB	Chrislin		384-Kbyte dynamic RAM, hidden refresh, 16 K bank disable, parity, 8/16 bit operation, on-board 5V generation, 24-bit addressing.	MR86-384	Comark	
2 Mbyte dynamic RAM, transparent refresh or off-board control, parity error detection, 8/16-bit data, 20/24-bit addressing	44-107 44-117	Anasco Anasco		384-Kbyte RAM	mBLC0384B	MicroIncls	50
4K bytes of battery-backed CMOS static RAM for storing critical system parameters during power failures, S/W drivers available, single-wide SBX module.	LSBXRAM4	CompModules	20	512-Kbyte DRAM, on-board parity generator/checker and error status register.	CI8086 +	Chrislin	
16 ROM/PROM expansion board jumper selectable address board.	mSBC416	MicroIncls		512-Kbyte DRAM, single- and double-bit error detection, single-bit correction.	CI796-EDC	Chrislin	
16-Kbyte RAM	mBLC016A	MicroIncls		512-Kbyte dynamic RAM, hidden refresh, 16 K bank disable, parity, 8/16 bit operation, on-board 5V generation, 24-bit addressing.	MR86-512	Comark	
32 Discrete optically coupled inputs - 5 mA @ 5V, 4 serial differential ports (transmits up to 5000 feet), 4K RAM, 8K PROM, resident diagnostics, battery back-up.	S80 I/M	Babcock		512-Kbyte dynamic RAM, transparent refresh or off-board control, parity error detection, 8/16-bit data, 20/24-bit addressing	44-105 44-115	Anasco Anasco	
32 Kbyte dynamic RAM, hidden refresh, 4 K bank disable, parity, 8/16 bit operation, on-board 5V generation 24-bit addressing.	MR85-032	Comark		512-Kbyte RAM	mBLC0512B	MicroIncls	55
32-Kbyte RAM	mBLC032 mBLC032A	MicroIncls MicroIncls	25	128K-2 Mbyte Parity checking dynamic RAM.	CD21/2140	CentData	
32-Kbyte ROM/PROM expansion	mBLC8432	MicroIncls		128K-512K Parity checking dynamic RAM.	CD21/2100	CentData	
32K or 64K RAM board expansion though direct interface. Address assignable anywhere within a 16 Mbyte address space. On-board parity generator checker and error status register.	mSBC032A/064A	MicroIncls		16-Kbyte RAM	mBLC8016	MicroIncls	
48-Kbyte RAM	mBLC048 mBLC048A	MicroIncls MicroIncls		16-Kbyte ROM/PROM	mBLC416	MicroIncls	
64 Kbyte dynamic RAM, hidden refresh, 4 K bank disable, parity, 8/16 bit operation, on-board 5V generation, 24-bit addressing.	MR85-064	Comark		16K of CMOS memory with one bus slot, battery back-up of 96 hours, and resident diagnostics.	S80 MEM	Babcock	60
			30	2 Mbyte DRAM, 24-bit addressing on Multibus and iLBXbus, 8/16 bit data, EDC correcting, two I/O ports, battery backup.	PSM2DA	Plessey	
				2 Mbyte DRAM, 8/16-bit data, 20/24-bit address, byte parity, optional 1 Mbyte.	PSM2P	Plessey	
				2 Mbyte DRAM, 8/16-bit data, 20/24-bit address, EDC correcting, optional 1 Mbyte.	PSM2A	Plessey	
				2 Mbyte RAM with 8 K cache, full error detection and correction, can support dedicated 32-bit memory bus.	MB2000	Matrox	

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line	
<b>Multibus</b>								
<b>Memories</b>				<b>(Cont'd)</b>				
32 sockets capable of accepting up to 2 Mbyte EPROM or 1 Mbyte RAM	CD21/2032	CentData	5	Fault detection/watchdog timer board. Resets Multibus system after failure, allows hardware reset from under software control, alarm output for unrecoverable failures, real-time interrupt. 24 user-defined LEDs and switches.	MT1004	Morrow	20	
512 Kbyte DRAM, 24-bit addressing on Multibus and iLBX bus, 8/16-bit data, EDC correcting, two I/O ports, battery backup.	PSM512DA	Plessey		General purpose slave board which measures absolute shaft position and provides a binary output corresponding to this shaft position based on a resolver input.	BMUT	Astro		
512 Kbyte DRAM, 8/16-bit data, 20/24-bit address, byte parity, optional 512 Kbyte, 128 Kbyte.	PSM512P	Plessey		High Speed Bus Coupler provides high speed DMA data transfers between Multibus and Unibus. Q-bus or other Multibus Systems. MAX G7K blocksize. Transfer rate up to 4Mbytes/sec. The Unibus link is DR11W compatible and supports inter-processor link mode.	8611	MTC		
512 Kbyte DRAM, 8/16-bit data, 20/24-bit address, EDC correcting, optional 256 Kbyte or 128 Kbyte.	PSM512A	Plessey		IEEE-488 (GPIB) host adaptor and cable with watchdog timer, supports 15 talkers/listeners.	LSBX488	CompModules		
64 Kbyte CMOS RAM, 8/16-bit data, 20-bit address, battery backup.	PSM6463	Plessey		Interface from Multibus to Network Systems Corporation A-400 HYPERchannel and B-400 HYBERbus Adapters.	10077NSC	IKON		
<b>Multifunction</b>								
MIL-STD-1553B bus controller, bus monitor, and remote terminal unit. Interfaces to Multibus I. Stores, responds to and transmits up to 119 messages depending on mode of operation selected. Operates on ± 12V.	BUS65508 BUS65509	ILC-DDC ILC-DDC	10	IRIG-B synchronizable reader/generator, event register, propagation delay correction, FIFO bus interface, AGC, auto-polarity, 1 microsecond accuracy, optional oven on-time rate and frequency outputs.	AITGMB1	KSystems	25	
Real Time Clock, memory expansion (RAM and EPROM) with opto I/O expansion.	NPX2000	Northern		ISBX-bus to PC-bus adaptor module, supports up to 3 ISBX modules, PC add-on card form factor.	LSBXMOTHER	CompModules		
SBX motherboard provides six 8/16-bit SBX connectors. 8237A-5 DMA controller supplies four channels of DMA. Two 8259A programmable interrupt controllers.	ZX564	Zendex		Multibus Display Monitor. Displays up to 24 Bit address values, and 16-bit data values. Monitors power, interrupt and status lines. Powerful design tool.	ZX906B	Zendex		
<b>Prototyping Boards</b>								
Board, Universal	mBLC905	MicroInds	15	Multibus PCB that interfaces Dataproducts Long Line Interface (DPI) printers to the SCSI bus.	ADP60	NCR	30	
Prototyping card with P1 and P2 connectors.	ZX905	Zendex		Multibus Tracer. Stores up to 1024 Bus Events. Displays events on CRT. Features an 8085A-2 which controls tracing, interpretation and displaying.	ZX907	Zendex		
Single width multimodule prototype board. All holes plated thru, holds up to 7-16 pin IC's or 1-40 pm, 2-14 pin and 4-16 pin IC's in combination 30 pm external connector.	BE00103	Bummer		Optical isolation/signal termination panel for MULTIBUS/ISBX bus digital I/O boards. Accepts up to 24 industry standard plug-in solid state input/output modules.	IRCX910 IRCX920	Intel Intel		
<b>Speech Circuits</b>								
Speech Encoder, voice output, digitized for high quality speech or sound, downloadable to RAM or speak from on-board EPROM, live & speaker outputs.	MV1500025	Microvoice	15	Real time calendar/clock and 8K bytes of CMOS static RAM, battery backed, watchdog timer and power-fail detection circuit on-board, S/W drivers available, single-wide SBX module.	LSBXSUPER	CompModules	35	
<b>Miscellaneous</b>				Real-time clock and SRAM SBX module. 1/100 sec to 99 years. Calendar/clock with 8 KB battery-backed CMOS, SRAM, watchdog timer and power-fail detection circuitry.	LSBX-SUPER	CompModules		
Bus analyzer, captures up to 8196 bus events, display and control via CRT, Trigger and trace conditions, bus master capabilities, direct readout of power supplies	MB110	SilControls		1/10 sec. to 99 yrs real time calendar/clock, H/W leap year counter, battery backed, S/W drivers available, single-wide SBX module.	LSBXCLOCK2	CompModules		
Bus display, display of 24 bit address, data, control, interrupts, and bus exchange signals, monitoring of bus clocks and power supplies	MB100	SilControls		1/1000 sec. to months real time calendar/clock, wake-up alarm & power fail sense circuit, battery-backed, S/W drivers available, single-wide SBX module.	LSBXCLOCK	CompModules		
Card extender with eight LEDs displaying buffered bus functions, system reset switch, on-board power switch for removal and insertion of boards without powering down system.	ZX611	Zendex		4 Port Connector Board for RETMA.	mBLC89581	MicroInds		
Development board with on-board NS32332 processor that enables evaluation of the NS32332 computer cluster and series 32000 family. 15 MHz operating frequency.	DB332-Plus	National	4 Port Connector Board for RMC.	mBLC8958	MicroInds			
Enhanced digitaltalker expansion module speech synthesis; 144 word vocabulary.	mBLX281A	MicroInds	80/05 System Monitor Firmware.	mBLC8908	MicroInds			
			80/216 System Monitor Firmware.	mBLC8930	MicroInds			

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus 2</b>							
<b>Communications</b>							
Communications. Bitbus communications controller supports message passing and interconnect space. Built-in self test. 512 KB DRAM 8044 Bitbus controller provides full Bitbus support. CDX 51 executive two IEEE P959 (SBX) sites.	MIBII 186/154	MicroInds		Intelligent color graphics subsystem with TMS34010 graphics processor. 40MHz clock, 2 MB frame buffer, up to 1280x1024 non-interlaced pixels, RS-343 video output standard. On-board 80186 CPU.	MIBII 386/171	MicroInds	
Communications. MIL-STD-1553 communications controller supports message passing and interconnect space. Built-in self test 512 KB DRAM bus controller or remote terminal mode. Bus analyzer feature. Dual 1553 bus processors.	MIBII 186/153	MicroInds		Serial I/O board. 4-Channel serial I/O controller, supports message passing and interconnect space. Built-in self test, 512 KB DRAM synchronous/asynchronous, full-duplex. RS-232 or RS-422. Two IEEE-P959 (SBX) sites.	MIBII 186/150	MicroInds	15
Communications. Dual modem controller supports message passing and interconnect space. Built-in self test. 512 KB DRAM. BELL 103 and 212A compatible modems. DAA. FCC part 68 certification. Pulse or DTMF dialing. 300 baud (FSK) or 1200 baud (PSK) call progress detect. Hook switch watchdog.	MIBII 186/155	MicroInds		<b>I/O</b>			
Connects eight RS-232 ports to any Multibus II system (two ports can be RS-422). On-board 80186 microprocessor, 512K RAM, 8530 Serial Communications Controller.	CD22/3800	CentData		Analog and digital I/O system with 32 digital I/O lines. A/D has 12- or 16-bit resolution, programmable gains to 500, up to 32 single-ended/16 differential channels.	DT2401	DataTrans	
Ethernet (IEEE 802.3) local area network controller.	iSBC186/530	Intel	5	Analog I/O. 64 channel analog input board supports message passing and interconnect space. Built-in self test. 512KB DRAM. 32 differential/64 single-ended inputs 20mV to 5V unipolar or bipolar ranges. 12-bit resolution. 50kHz sample rate. Two IEEE P959 (SBX) sites.	MIBII 186/141	MicroInds	
Four-channel asynchronous/synchronous full-duplex serial controller. Supports RS-232, RS-423, RS-485, or RS-449, up to 1.5 Mb/s data rate.	LSBX-SERIAL/4	CompModules		Analog input. 32 channel analog input board. Supports message passing and interconnect space. Built-in self test. 512KB DRAM. 16 differential/32 single-ended analog inputs. 20mV to 5V unipolar or bipolar ranges. 12-bit resolution. 20 kHz sample rate two IEEE P959 (SBX) sites.	MIBII 186/140	MicroInds	
4-channel multiprotocol serial comm. board, each channel can be independently configured to be RS232C, RS422, RS423, or RS485, S/W drivers available, double-wide SBX module.	LSBXSERIAL4	CompModules		Analog output. 16 channel analog output board. Supports message passing and interconnect space. Built-in self test. 512 KB DRAM 4-20 mA current loop 10V uni- or bipolar. 12-bit resolution. Two IEEE P959 (SBX) sites.	MIBII 186/145	MicroInds	
<b>Controllers</b>				BitBus board. 8044 BitBus interface with two iSBX connectors.	MIBII 186/154	MicroInds	20
IEEE-488 (GPIB) controller supporting up to 15 talkers/listeners, GPIB cable included, S/W drivers available, single-wide SBX module.	LSBX488	CompModules		Central Services Module, integrates Multibus II central systems functions on a single board.	iSBCCSM/001	Intel	
SCSI and floppy controller board. SCSI/ANSI and 3T9.2 compatible, WD33C93 buscontroller, 82258 DMA controller. Supports floppy transfer rates to 500K/sec and SCSI rates up to 3.2M/sec.	CD22/4500	CentData		Digital I/O. 48 channel digital I/O board supports message passing and interconnect space. Built-in self test. 512KB DRAM. Programmable. I/O lines with termination provisions. Two programmable timers. Two IEEE P959 (SBX) sites.	MIBII 186/112	MicroInds	
SCSI bus controller supporting up to 8 devices, S/W drivers available, single-wide SBX module.	LSBXSCSI	CompModules	10	Digital I/O. 96 channel digital I/O board supports message passing and interconnect space. Built-in self test. 512KB DRAM. Programmable I/O lines with termination provisions. Two programmable timers. Two IEEE P959 (SBX) sites.	MIBII 186/111	MicroInds	
<b>Digital Signal Processing</b>				Multibus II to Multibus I Link Board.	iSBCLNK/001	Intel	
Dual channel digital signal processor. Supports message passing and interconnect space. Built-in self test. 512 KB DRAM four TMS32020 digital signal processors. Cascaded or parallel processing. 4 KB high-speed dual-port RAM. 16 bit digital I/O. 16 bit analog output.	MIBII 32020	MicroInds		Parallel and serial I/O module for 386 and other high density SBC. Includes three 8-bit parallel ports and two high speed multi-protocol serial channels.	LSBX386I/O	CompModules	25
<b>Graphics</b>				Serial I/O. 16-channel serial I/O controller supports message passing and interconnect space. Built-in self test. 512KB DRAM. Asynchronous, full-duplex, 50-19, 200 baud flexible. Programmable interrupts. Two IEEE P959 (SBX) sites.	MIBII 186/155	MicroInds	
Color graphics board. Intelligent color graphics subsystem with 640x640x4or 512x512x4 resolution. 80186 CPU, interconnect controller for self-testand configuration, 82720 GDC, 512 KB display memory.	MIBII 186/170 MIBII 186/171	MicroInds MicroInds					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Multibus 2</b>							
<b>I/O</b>							
<b>(Cont'd)</b>							
Serial I/O board. Four independent RS-232 or RS-422A/449 synchronous/asynchronous channels, two SBX connectors.	MIBII 186/150	MicroInds		1/10 sec. to 99 yrs real time calendar/clock, H/W leap year counter, battery backed, S/W drivers available, single-wide SBX module.	LSBXCLOCK2	CompModules	20
Terminal I/O subsystem, supports up to 128 asynchronous RS-232C devices on multi-user host, diagnostic and system administration software for fault isolation and system tuning.	HPS	Systech		1/1000 sec. to months real time calendar/clock, wake-up alarm & power fail sense circuit, battery-backed, S/W drivers available, single-wide SBX module.	LSBXCLOCK	CompModules	
Six channel serial I/O port controller. Four ports are RS-232C, two ports are configurable for RS-232C or RS-422.	iSBC186/410	Intel		<b>Multimodule</b>			
8-Channel Serial I/O Controller supports message passing and interconnect space. Built-in self test 512 KB DRAM asynchronous, full duplex. RS-232C or RS-422. Two IEEE P959 (SBX) sites.	MIBII 186/152	MicroInds		<b>Controllers</b>			
<b>Memories</b>				GPIB controller interface—complete controller/talker/listener, device driver and example application software provided.			
Memory Management Unit (MMU) for MT68020.	MM86	Microbar			xSBX 20	Ziatech	
0.5-Mbyte dual-port memory board	iSBCMEM/312	Intel		<b>I/O</b>			
1 Mbyte dual-port memory board	iSBCMEM/310	Intel		Parallel I/O interface—48 programmable I/O lines; optional interrupt requests and handshaking, each connector provides 8 data lines $\pm 12V$ , + 5V and ground for user interfacing.			
2 Mbyte dual-port memory board	iSBCMEM/320	Intel			zSBX 30	Ziatech	
4 Mbyte dual-port memory board	iSBCMEM/340	Intel		<b>Proprietary</b>			
4, 16, or 64 MB dynamic RAM board. 8, 16, or 32-bit transfers, programmable wait-state operation.	MIBII IIX	MicroInds	10	<b>Controllers</b>			
4K bytes of battery-backed CMOS static RAM for storing critical system parameters during power failures, S/W drivers available, single-wide SBX module.	LSBXRAM4	CompModules		Floppy disk controller for four drives.			
16-site JEDEC byte wide memory device board.	iSBC MEM/601	Intel			MFC04	Wintek	(4913)
<b>Multifunction</b>				for memory or printer	SUP-9	Octagon	25
Performs all central control functions. Central services module required for all Multibus II systems utilizing multiple processors.	CSM-B	Microbar		<b>Converters</b>			
<b>Prototyping Boards</b>				Analog-to-digital, 12-bit, 16 channel			
Intelligent I/O development kit with 80186 CPU 8 MHz. 512 KB DRAM, interconnect controller for self-test and configuration. Serial port with two SBX connectors.	MIBII 186/110A	MicroInds			MAI04	Wintek	(4913)
Intelligent prototyping board. Includes iAPX186, 512K parity DRAM, sockets for 128K EPROM, 16 interrupts, one 16-bit SBX connector, and user definable P-2 connector.	CD22/6410	CentData	15	Digital-to-analog, 8-bit, 2 channel	MAI20	Wintek	(4913)
<b>Miscellaneous</b>				<b>Graphics</b>			
IEEE-488 (GPB) host adaptor and cable with watchdog timer, supports 15 talkers/listeners.	LSBX488	CompModules		Video expansion board, IBM compatible monochrome keyboard port, 16KB video RAM, up to 64 KB PROM			
ISBX-bus to PC-bus adaptor module, supports up to 3 ISBX modules, PC add-on card form factor.	LSBXMOTHER	CompModules			SLPCXAT	Slicer	
Real time calendar/clock and 8K bytes of CMOS static RAM, battery backed, watchdog timer and power-fail detection circuit on-board, S/W drivers available, single-wide SBX module.	LSBXSUPER	CompModules		<b>I/O</b>			
Real-time clock and SRAM SBX module. 1/100 sec. to 99 yrs. calendar/clock with 8KB battery-backed CMOS SRAM, watchdog timer and power fail detection circuitry.	LSBX-SUPER	CompModules		IEEE-488 Bus interface			
					MGP00	Wintek	(4913)
				Opto module rack driver peripheral card	SUP-7	Octagon	30
				8-Port RS-232 serial interface.	MSI08	Wintek	(4913)
				64-Line parallel.	MPI08	Wintek	(4913)
				<b>Memories</b>			
				Expansion module with memory mapping.			
					MRR49	Wintek	(4913)
				Expansion with sockets for 56K RAM/ROM.	MRR19	Wintek	(4913)
				Memory expansion module with sockets and memory mapping, battery backup included.	MRR59	Wintek	(4913)
				Memory expansion module with sockets for 56K RAM/ROM, battery backup included.	MRR29	Wintek	(4913)
				RAM expansion board, 1 Mbyte, 4 serial ports, real-time clock, Centronics printer port.	SEAT 1MEG	Slicer	35
				<b>Multifunction</b>			
				Peripheral card			
					SUP-6	Octagon	
					SUP-8	Octagon	
				<b>Miscellaneous</b>			
				Backplane, 4-slot.			
					ABP04	Wintek	(4913)
				Backplane, 7-slot.	ABP07	Wintek	(4913)
				Breadboard with parallel interface	MPB00	Wintek	(4913)
				Counter/timer module with battery	MCT10	Wintek	(4913)
				Driver/Sensor module with 4 optically isolated inputs and 8 open-collector drivers.	MDS44	Wintek	(4913)

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

\*Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Proprietary</b>							
<b>Miscellaneous</b>				<b>(Cont'd)</b>			
Driver/Sensor module with 8 optically isolated inputs.	<b>MDS08</b>	<b>Wintek</b>	<b>(4913)</b>	Storage module device, designed to interface LSI-11 or MicroVAX computers to a wide variety of storage module devices, blockmode DMA, can control two SMD drives in excess of 1 Gbyte each, supports up to 20 MHz transfer rates.	SMV22	GENROCO	20
Driver/Sensor module with 16 open-collector drivers.	<b>MDS80</b>	<b>Wintek</b>	<b>(4913)</b>	Streaming tape, for QIC-02 1/4 inch streaming tape drives, uses DMA.	STV11	GENROCO	
Expansion board, 256 Kbyte RAM, 4 serial ports, parallel printer port, real-time clock with battery backup.	SEAT 256	Slicer		Winchester disk, controls two ST-506 5-1/4 inch Winchester disk drives and supports blockmode DMA.	MWV22	GENROCO	
16-Button Keypad with 15 7-segment displays.	<b>MCI11</b>	<b>Wintek</b>	<b>(4913)</b>	Dual height MSCP ST506/ST412 Winchester disk controller. Features WOMBAT comprehensive on-board interactive formatting and diagnostic firmware, block mode DMA, command queueing, seek optimization and overlap, bad block replacement, ECC, supports two physical drives.	SRQD11B	Webster	
<b>Q-bus</b>				Quad height MSCP 1 MB Cached ESDI Winchester disk controller. WOMBAT comprehensive on-board interactive formatting and diagnostic firmware, programmable look-ahead, supports up to four physical drives, block mode DMA, drive shadowing, seek optimisation, command queueing, ECC, dynamic bad block replacement, on-board bootstrap.	WQESD	Webster	
<b>Communications</b>				Quad height MSCP 1 MB Cached SMD (standard, modified, enhanced, and extended) Winchester disk controller. WOMBAT comprehensive on-board interactive diagnostic and formatting firmware. Programmable look-ahead, supports two physical drives with seek optimization and overlap, ECC, dynamic bad block replacement, on-board bootstrap.	WQSMD	Webster	25
Intelligent Ethernet controller for Q-Bus systems. 80186 CPU, up to 512 KB RAM, supports TCP/IP Internet protocols.	EXOS203	Excelan	5	<b>Converters</b>			
Multiplexer channel expansion, specify (32 single-ended or 16 differential) or (64 single-ended or 32 differential) channels.	DT2772	DataTrans		Encoder to Computer Interface Module.	C1500	Buckminster	
Dual height RS-232 asynchronous 16-line multiplexer compatible with two DHV11's. Programmable features: split speed baud rates, character length, parity, stop bits, XON/XOFF. 4 character per line FIFO silo and 256 character common silo. Block mode DMA, console DL emulation, line time clock.	WQDHV	Webster		Three-channel resolver-to-digital converter that obtains positional information, as well as three independent channels of D/A conversion. Used for a servo axis-monitoring/positioning control subsystem.	DDC5525	ILC-DDC	10
Dual height RS-232 asynchronous 8-line multiplexer. Compatible with DZ11 or DZV11. Programmable features: baud rates, character length, parity, stop bits, and transmitter enable. Ring, carrier, and DTR modem controls. Distribution boards, cables and 19" rack panels available.	SDZV11	Webster		16 8-bit A/D channels with a 2 us conversion time, backplane temperature and voltage sensors, a programmable real-time clock and programmable non-volatile upper-lower thresholds for each channel. Operates on polling or interrupt modes and includes diagnostic software.	190	Codar	
<b>Controllers</b>				<b>Graphics</b>			
Controller for AC 8" floppy disk SA800- or SA850 compatible, on-board bootstrap, RX02 emulation.	D4140-05	Qualogy		Family of seven mix and match boards that allows users to perform advanced image processing operations in hardware, such as convolutions, histogram and equalization, and feature extraction.	IP512	Imaging	15
Controller for DC 8" floppy disk Y-E Data YD-180 compatible (SA850-type interface), on-board bootstrap, RX02 emulation.	D4140-05	Qualogy		Frame processor, 16-bit for accelerating arithmetic-intensive image processing.	DT2658	DataTrans	30
Controller for up to four ESDI 5 1/4" Winchester drives	QE2	Qualogy		Real-time image acquisition and signal processing. Contains complete alpha-numeric display as well as pan, zoom, and scroll features.	QVG123	Datacube	
Controller for up to two SDM 10 1/2" disk drives, features 1 MB cache memory, field-loadable microcode, 48-bit ECC, dual wide controller, LSI-11 and MicroVAX compatible.	QS4	Qualogy		Video inserter. IRIG reader, clock, reticle alphanumeric titling, time, crosswire/box reticle insertion into RS-170A, NTSC, CCIR video, optional A/D inputs and binary video data insertion.	VICCUR	KSystems	
Controller for 5 1/4" SA450-compatible floppy disk drive, on-board bootstrap, RX02 emulation, not RX4-50 compatible.	D4120	Qualogy		Video overlay. Dual module, synchronizes CRT controller to incoming RS-170A, supplies pixel clock to CRT controller. Inserts TTL video signals from CRT controller into video. Compatible with KTL100 and TFL100.	VO-Q	KSystems	
Double-density, double-sided eight-inch or 5-1/4 floppy disk controller, Shugart compatible.	RXV21	GENROCO					
Ethernet/IEEE 802.3 communications controller	NP200	Micom Int					
Ethernet/IEEE 802.3 data link communications controller	NI2010A	Micom Int					
Ethernet intelligent controller with 80186 microprocessor, DMA capability, TCP/IP transport protocols.	EXOS203	Excelan					
Intelligent networking, one or two Mb/s DMA transfer rate on fiber or coax in SDLC or token pass. Up to 99 other stations on LAN.	LQ-4	Computrol					
MicroVAX II or LSI-11 multifunction disk controller. Supports 5T506 Winchesters, 5 1/4- and 8-inch floppy disks. DEC MSCP compatible.	SMS0107	SMS					

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MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Q-bus</b>							
<b>Graphics</b>				<b>(Cont'd)</b>			
Single-board real-time image processor with 512x512x8 resolution. Holds four images, split-scan mode, drive software.	Series 100	Imaging		Q-bus compatible memory with 1M byte capacity. Quad board, 22-bit addressing, compatible with LSI-11 family and all Q-bus based minicomputers.	DR223	Dataram	
640x480 color display processor	QG640	Matrox		Q-bus compatible memory with 2M byte capacity. Dual board, 22-bit addressing, compatible with LSI-11 family and all Q-bus-based minicomputers.	DR216	Dataram	
<b>I/O</b>				Q-bus compatible memory with 256K byte capacity. Dual board, full-function parity, 22-bit addressing.	DR215	Dataram	
Analog input expansion.	DT2774	DataTrans		Dual height 1 MB MOS dynamic memory board. Automatic parity error detection, 160 ns access time, supports block mode DMA bus protocol for high speed DMA transfers in blocks of up to 16 words. 16 or 22-bit addressing, on-board parity, parity CSR, and refresh, parity CSR address and RAM bank select.	SMSV11-P6	Webster	30
Analog output system with four D/A converter outputs, four digital outputs, 8-bit resolution.	DT2767	DataTrans		Dual size 4MB board with Error Detection and Correction for 11/23, 11/73, or 11/83 (without PMI), runs diagnostics and uses 1MB chips.	CI-QBUS-EDC	Chrislin	
Analog output with four D/A converter outputs, four digital outputs, 12-bit resolution.	DT2766	DataTrans	5	Dual-port RAM and controller, 32 Kbytes standard, 128 Kbytes optional.	DT3369	DataTrans	
Analog with 16 single-ended or 8 differential channels, 11-bit analog A/D converter.	DT2781	DataTrans		Two Mbytes of Q-Bus compatible memory. Configurable with either 64K or 256K DRAMs, on-board parity, block-mode DMA support and 22-bit addressing.	CDM85/73R	Cyberchron	10
Digital to analog expander.	DT3376	DataTrans		Four Mbyte add-in expansion for the DEC LSI-11/73, LSI-11/23, LSI-11/23PLUS, and MicroVAX. On-board parity CSR, supports block-mode DMA.	CDM84/73R	Cyberchron	
DMA Analog input system for high-level inputs, 45 kHz throughput (single channel).	DT2782	DataTrans		Eight Mbytes of add-in memory for the MicroVAX using 256K DRAMs. Full error detection and correction of single-bit errors.	CVM630/8-EDC	Cyberchron	35
High-level A/D, DMA, 12-bit resolution, up to 64 single-ended or 32 differential inputs.	DT3382	DataTrans		8MB DRAM with Error Correction for MicroVAX II.	CI-MIV8-EDC	Chrislin	
High-level analog to digital, 16 single-ended or 8 differential inputs.	DT2762	DataTrans		16MB DRAM with parity for MicroVAX II.	CI-MIV16	Chrislin	
IEEE-488 Interface and handler for Microvax II-DMA I/O.	77611731	NationalInst		64K DRAM memory, 512KB capacity, battery back-up, CSR, parity, lifetime warranty.	QRAM11	Clearpoint	15
IEEE-488 Interface and handler GPIB 11-1 programmed I/O.	17801001	NationalInst		128 Kbyte to 2 Mbyte DRAM single- and double-bit error detection; single-bit correction.	CI1173-EDC	Chrislin	
IEEE ± 488 Interface and handler GPIB 11-2 DMA I/O.	77604501	NationalInst		128 Kbyte, 4 Mbyte DRAM, block-mode DMA, parity, CSR.	CI1173	Chrislin	40
Isolated analog input expansion.	DT2775	DataTrans		256 Kbyte-1 Mbyte DRAM on-board parity generator/checker and control status register.	CI1123 +	Chrislin	
Isolated low-level analog to digital, 4 differential channels.	DT2765	DataTrans		256K DRAM memory, Block Mode, battery back-up, 1, 2, and 4MB capacity, bank selectable up to 64MB on board EDC lifetime warranty.	QED1	Clearpoint	
Low-level analog to digital, 16 single-ended or 8 differential inputs.	DT2764	DataTrans		256K DRAM memory, 256KB, 512KB, 1MB, 2MB capacity, battery back-up, CSR, parity, block mode, DMA, lifetime warranty.	QRAM44B	Clearpoint	20
Low-level analog, 16 single-ended or 8 differential, 12-bit A/D, two-channel 12-bit D/A converters.	DT2785	DataTrans		256K DRAM memory, 512KB, 1, 2, 4, MB capacity battery back-up, CSR, parity, Block Mode, DMA, lifetime warranty.	QRAM88B	Clearpoint	
Multifunction interface with two serial ports. 22-bit addressing for EPROM access.	CM1783	Cyberchron		4 Mbyte DRAM, parity, runs under PMI on the Microvax II.	CI-MIV4	Chrislin	45
Parallel digital, 16 data inputs 16 latched outputs.	DT2768	DataTrans		8 Mbyte, DRAM, parity, runs under PMI on the Microvax II.	CI-MIV8	Chrislin	
Serial, 16-port available in DH11 or DHV11 emulation. Can be configured to support 16 to 64 ports on a single quad height controller in 16-port increments. Blockmode DMA, expansion chassis and panels available	DHV11	GENROCO		<b>Multifunction</b>			
Dual-port analog output system, DMA, 12-bit resolution.	DT3366	DataTrans		Allows system to monitor it's own internal voltages and temperature and to communicate status to a back-up system. Includes single channel DLV11J serial port, two-stage Watchdog Timer, calendar clock with battery back-up, temperature sensor, A/D converter, digital I/O port, plus alarm on dual-wide module with software support.	170	Codar	
Dual-ported high-level DMA Analog input system, 12-bit resolution.	DT3362	DataTrans		CMOS Calendar Clock with 2 lithium battery back-up, two stage watchdog timer with relay and logic outputs and a 50 Hz LTC on a dual with module, plus complete calendar clock software support.	181	Codar	
Eight port asynchronous multiplexer, emulates two DEC DZV11s in half the space.	MZV8-11	Mintronics					
16 8-bit A/D channels with a 2 µs conversion time, backplane temperature and voltage sensors, a programmable real-time clock and programmable non-volatile upper-lower thresholds for each channel. Operates on polling or interrupt modes and includes diagnostic software.	190	Codar					
<b>Memories</b>							
Expansion board for 32K/128K of CMOS RAM or 32K/256K of EPROM. Full 22-bit address decoding up to 4MB.	CSM83/22	Cyberchron					
Q-Bus compatible memory add-on board available in 1, 2, and 4MB versions.	DR283	Dataram					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line	
<b>Q-bus</b>								
<b>Multifunction (Cont'd)</b>								
CMOS Calendar Clock, 2Kx16-bit CMOS RAM with lithium battery back-up, single stage Watchdog Timer with logic alarm output, hardware boots diagnostics and interactive monitor in EPROM, 60 Hz LTC 8-bit I/O, dual-wide 22-bit.	102	Codar		Two-stage Watchdog Timer with relay and logic outputs, 50 Hz LTC on dual-wide modue. Boot and software delays are individually set using rotary switches.	180	Codar	15	
MSCP compatible, SCSI host adapter for support of magnetic, SCSI peripherals. The adapter is firmware optimized to include support of SCSI optical disk systems. "OPUS" software utility available for optical. Archival applications under RSX and VMS operating systems.	B08L00	USDesign		15 independent 16-bit Counter/timers with 19 different programmable interrupts on a dual-wide module with diagnostics.	140	Codar		
MSCP Compatible, SCSI host adapter for support of SCSI compatible hard disks and peripheral subsystems. TS-11 emulation of start/stop SCSI tape devices also available.	B08M00	USDesign		<b>RAMport</b>				
Plus firmware support for VOS (Virtual Optical Storage) for file structured optical applications. Full hard disk emulation for optical applications. Full hard disk emulation for optical disks is provided along with "OMAP" optical utilities.	B08V00	USDesign		<b>Converters</b>				
Universal board for use as disk, tape and communications controller. Supports 1 to 57 serial lines, for use with PDP-11 and MicroVax II.	Liberty	Trimarchi		Provides a way of interfacing SBX daughter boards to 28-pin JEDEC memory sites. For 8-bit, SBX boards. Does not support DMA or interrupts. Maps SBX I/O registers into memory address space.	RP080	HiTech		
15 independent 16-bit Counter/timers with 19 different programmable interrupts on a dual-wide module with diagnostics.	140	Codar	5	<b>Memories</b>				
<b>Miscellaneous</b>				Adds a RAMport I/O bus to any 24/28 pin JEDEC memory socket. Original memory fits on top, while RAMport bus is brought out to external memory mapped I/O modules. Software controls switching between memory and I/O bus access. Allows expansion of non-expandable systems. Compatible with RAMport I/Omodules for serial, parallel, A/D, D/A, etc.	RP001	HiTech		
Allows system to monitor it's own internal voltages and temperature and to communicate status to a back-up system. Includes single channel DLV11J serial port, two-stage Watchdog Timer, calendar clock with battery back-up, temperature sensor, A/D converter, digital I/O port, plus alarm on dual-wide module with software support.	170	Codar		1Kx8 100 ns dual-port static memory allows two computers with 28-pin memory sockets to access the same memory. High-speed/low power versions available. Full arbitration transparent in operation, includes additional arbitration and interprocessor interrupt capability.	RP040	HiTech		
Bus grant cards provide interrupt and DMA continuity for empty slots in backplane. Dual Quad and Knucklebuster sizes.	160	Codar		<b>RM-65</b>				
CMOS Calendar Clock on a dual-wide 22 bit module, with two lithium battery back-up and complete software support.	120	Codar		<b>Memories</b>				
CMOS Calendar Clock with 2 lithium battery back-up, two stage watchdog timer wth relay and logic outputs and a 50 Hz LTC on a dual with module, plus complete calendar clock software support.	181	Codar	10	Battery backup 12K CMOS RAM each of the 3-4K sections are individually addressable throughout the full address space.	GE65-12K	Golden	20	
CMOS Calendar Clock, 2Kx16-bit CMOS RAM with lithium battery back-up, single stage Watchdog Timer with logic alarm output, hardware boots diagnostics and interactive monitor in EPROM, 60 Hz LTC 8-bit I/O, dual-wide 22-bit.	102	Codar		<b>S-100</b>				
CRT emulator. Complete VT-100 emulation with 80/132 column, 24 row, smooth scroll, non-volatile setup memory, true 19200 baud speed, on-board Z80, keyboard, serial I/O ports, and composite or separate video outputs.	KTL100	KSystems		<b>Communications</b>				
IRIG-B synchronizable reader/generator, event register, propagation delay correction, FIFO bus interface. AGC, auto-polarity, Dual size module, 1 μs accuracy and on-time rate and frequency outputs.	AITG	KSystems		Intelligent communications controller for IEEE-696 bus computers. CSMA/CD protocols, on-board CPU and communications management firmware.	NIB100/01	Destek	25	
VT-100 emulation and DLV-11 interface. 80/132 column, 24 row, smooth scroll, non-volatile setup memory, true 75000 baud speed, on-board Z80, keyboard, Auxiliary I/O ports, Composite, separate video outputs.	TFL100	KSystems		Provides a simplified interface between the S100 (IEEE-696) Bus and the ARCNET modified token passing Local Area Network (LAN).	ARCNET-S100	SMC		
			<b>Controllers</b>					
			Floppy disk controller, controls both 5-1/4 and 8-inch floppy disk drives.	LDP72	Lomas	30		
			for both hard disk and cartridge tape.	HD/CTC	Teletek			
			Graphics, IBM-PC color graphics board compatible. Allows IBM-PC programs to run on S-100 bus computers.	LDPCOLOR 1	Lomas			
			SMD controls one or two drives at 10Mb/s	WDC-SMD	DUAL			
			Supports up to 4 ST-506 hard disks and up to 4 floppy disk drives, 8K on-board sector buffer, drivers for MS-DOS, CC-DOS and CPM-86.	Control-It-All	Lomas			
			9-Track tape controller with FIFO buffering on DMA transfers. Supports tape densities up to 6250 BPI.	TCON	DUAL			
				<b>Converters</b>				
				Analog to digital, 12-bit resolution and accuracy	AIM12	DUAL	30	
				Digital to analog, 12-bit accuracy.	AOM12	DUAL		
				Voltage to current, 12-bit accuracy.	VIC4-20	DUAL		

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MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>S-100</b>							
<b>Converters</b>				<b>(Cont'd)</b>			
64-input A/D converter, 8-bit resolution	A/D64-100	IndComp		Data Controller. Consecutive sector transfer (non-interleaved data)	OMTI3100	SMS	
64-output A/D converter, 8-bit resolution	D/A64-100	IndComp		Floppy disk controller for 3-1/2 or 5-1/4 inch drives. Based on the SCSI disk controller (SDC) chip and the drive interface (DIF) chip.	ADP47	NCR	25
<b>I/O</b>				General Purpose floppy disk controller for 3-1/2 or 5-1/4 inch drives. Provides a high level interface between the SCSI bus and the drives.	ADP20	NCR	
Digital, MIL-STD-1397 (NTDS) Type A (SLOW) or B (FAST), 16/2, Peripheral/Computer/Intercomputer Modules, non-DMA bus interface, single card.	810701	Syscon		High performance intelligent controller designed to control up to four disk drives that use the industry standard or extended SMD interface. Disk transfer rate from 10 Mb/s to 24 Mb/s.	ADP48	NCR	
Digital, MIL-STD-1397 (NTDS) Type A (SLOW), 16/32 bit, Intercomputer mode, DMA bus interface, single card.	841101	Syscon		Intelligent disk drive for up to four ST506 Winchester 5-1/4 inch drives or four flexible drives, 56-bit error-correction code, 1.5-Mb/s transfer rate to host.	ADP41	NCR	
Hard disk controller. Simultaneously controls 4 hard disks and does ECC and CRC generation on data fields.	HDC1001	AdvDigital	5	SCSI host interface.	OMTI5000	SMS	30
IEEE-488 Hardware interface GPIB-696 DMA I/O, handler available.	77607001	NationalInst		SCSI host interface (Revision 17 implementation)	OMTI7000	SMS	
IEEE-488 Hardware interface GPIB-696 P-1 program I/O handler available.	77607101	NationalInst		SCSI intelligent disk controller supports a variety of SMD-O disk drives, up to 1 Mb/s transfer rate, 10-MHz disk transfer rate, selectable-read recovery algorithm.	ADP44	NCR	
Eight serial ports for multiuser environment.	OCTAPORT	Lomas		SCSI to ST-506/412 (hard), and SA-400 (floppy) disk drive controller. For 3-1/2 or 5-1/4 inch drives.	ADP46	NCR	
<b>Memories</b>				ST506 hard disk controller.	DAVID1K	Davidge	
accepts 2716 EPROMs or 2732 EPROMs. 64 Kbyte RAMS may be mixed with 2716 EPROMs allowing use as a RAM/EPROM board.	EPROM	DUAL		Tape Controller, SCSI to QIC36	ADST100	Western	
Dynamic RAM, 256 Kbyte. Supports 8- and 16-bit data paths.	LDP256K	Lomas	10	Winchester controller. Half slot for PC/XT, and compatibles with radial connection.	WD1002-WXE	Western	35
Dynamic RAM, 256 Kbyte to 2 Mbytes.	MEGARAM	Lomas		Winchester Disk Controller, SCSI to Four ESDI Drives	ADSD200	Western	
high-density memory with 8 or 16 bit data paths. Parity error checking. 1Mbyte on board.	EMEM-1MB	DUAL		Winchester disk, supports ST506/412 and ESDI disk drives.	OMTI7100	SMS	
High-density memory with 8 or 16 data paths. Parity error checking.	DMEM-256KP	DUAL			OMTI7150	SMS	
Non-volatile memory. On-board lithium battery.	CMEM-32K	DUAL		Winchester disk, 3-1/2 inch form factor, disconnect/reconnect, CCS (common command set)	OMTI3500	SMS	40
Static RAM, up to 1 megabyte, 100 ns access, supports 8 and 16 bit processors.	MEGA-S-RAM	Lomas	15		OMTI3527	SMS	
Static RAM, 128 Kbyte, 130-ns board access time, for high performance 16-bit systems.	RAM67	Lomas		Winchester floppy and tape controller, QIC-02 tape drive, 3-1/2, 5-1/4, and 8-inch floppy disks	OMTI5400	SMS	
<b>Multifunction</b>				Single board interface between the 8-bit IBM PC/XT (or AT) I/O channel and the SCSI bus. It provides all SCSI options with many additional features. When used with the DMA and interrupt capabilities of the host PC, it can implement a fast and full function SCSI-I/O channel.	RT10-XT	RanchoTech	
SCSI adapter, supports hard disk and tape drives, 4 serial ports (38.4 baud max), battery protected clock calendar, 3 programmable interval timers with interrupts.	LDP-SCSI	Lomas		Three-in-one SCSI controller for IBM PC/XT, AT and compatibles. Provides a floppy disk controller, a hard disk controller and an SCSI host adapter on a half card format.	RT100XT	RanchoTech	
System support board, two serial ports, two parallel ports, real-time clock, battery protected clock calendar.	HAZITALL	Lomas		Four-layer, high performance SCSI bus interface controller for the IBM PC/AT. It allows the AT to communicate with multiple SCSI device-independent peripherals: optical disk drives, laser printers, hard disks, etc.	RT10-AT	RanchoTech	
<b>Miscellaneous</b>				<b>Converters</b>			
Calendar/Clock, alarm with tone generator	CCA-100	IndComp		SCSI single-ended to differential-ended converter board. Two RT-SDAs can be used to extend an SCSI cable length from 6 meters to 25 meters for applications where both the initiator and target are single-ended.	RT-SDA	RanchoTech	45
Calendar/clock/timer board, allows time, date, day of week, to be provided to CRT display, or used for logging. Provides 1/100th second timing increments, long-term battery backup.	CCT-100	IndComp	20				
clock/calendar module with on board lithium battery.	CLK-24C	DUAL					
<b>SCSI</b>							
<b>Controllers</b>							
Controls one 1/4 inch data cartridge tape drive. Can be connected to tape drives that use the QIC-36 interface.	ADP55	NCR					
Controls up to four streaming tape drives that use the industry standard PERTEC tape interface.	ADP53	NCR					

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

Bold face indicates additional data is provided on the page noted.



## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>SCSI (Cont'd)</b>				polynomial checking generator, 4 full duplex channels, error checking CRC-12, CRC-16, LRC-8			
<b>I/O</b>				RS-232 and 20 mA current loop serial communications card. Full or half-duplex operation.			
Flexible, multi-master I/O expansion using SCSI bus provides full SCSI (ANSC X3T9.2) and SASI compatible bus, 17 bi-directional I/O lines, 8-bit input port.				Serial communications board with RS-422 capability.			
1AX Ampro				Dual asynchronous and synchronous serial communications card. Full or half duplex operation.			
<b>Memories</b>				Dual programmable RS-232C or RS-422/485 serial interface. Direct plug-in replacement for Pro-Log 7304.			
Video RAM emulator, for use with LittleBoard/186. Simulates 6845 registers.				Four channel communications controller. Quad RS-422 (asynchronous operation), SDLC, HDLC protocols, and 8259A interrupt controller.			
2VR Ampro				<b>Controllers</b>			
<b>Multifunction</b>				Add on centronics style port, for parallel printers. Can also be used as a general purpose input and output parallel port incorporating an 8255 PIA.			
Centronics parallel printer interface. Allows CPU to output to a Centronics compatible (the industry standard) parallel printer. All output control and input status lines are supported.				Add on serial port compatible with JEDEC-28 pin RAM socket, allows addition of an RS-232 serial async port without losing access to RAM. Replaces RAM in socket on users pc board using piggyback RAM. Multiple I/O ports may be added using one RAM socket.			
SBSxCEN SingleBoard				Alphanumeric display and keyboard controller. Direct drive of 32-digit display. 32x8 display RAM with no external refresh required.			
Companion board for LittleBoard/186 with buffered I/O bus, two additional serial ports (RS-232/422), 512K bytes of battery-backed RAM.				ARCNET local area network (LAN) controller, on-board 2 Kbyte dual-ported buffer memory, up to 255 nodes, coax network interface			
EXPANSION/186 Ampro				ARCNET Network Interface Module links Multibus computers to ARCNET local area networks providing user-transparent network operation, control and protocol.			
SCSI interface. Standard SCSI bus interface module. Initiation or target CPU. DMA or pseudo-DMA modes. Uses 5380 chip, parity, arbitration, and reselection is supported, socketed terminators can be removed.				ARCNET Network Interface Module links PC-compatible computers to the ARCNET local area network.			
SBSxSCSI SingleBoard				ARCNET Network Interface Module links STD PC-compatible computers to the ARCNET local area network.			
<b>Prototyping Boards</b>				CMOS Dual Asynchronous SDLC RS232/RS422			
User-configurable general purpose I/O and memory expansion interface for LittleBoard/186. With breadboarded custom circuitry for data acquisition, process control, and test instrumentation.				Color terminal controller, on-board Z80 with software, up to 16 colors, NTSC, PAL or RGB video, 40x24 text or 256x192 graphics.			
PROTO/186 Ampro				Cross hair generator and digitizer.			
<b>Miscellaneous</b>				CRT controller with keyboard interface. 80x25 character display, 128 character display font. RS-170 composite video output.			
Battery-backed real-time clock for any system having an SCSI bus or SCSI host adaptor.				Disk drive subsystem with 3.5 inch microfloppy drive and Western Digital controller.			
SCSI/CLOCK Ampro				DMA (Z80).			
Full SCSI interface to disk and tape controllers. Single width, supports DMA.				Floppy disk controller. Controls up to four drives. Supports 5-1/4 inch and 8 inch formats, single or double density, single or double-sided. IBM3740 and System 34 compatible.			
SCSI SBE				Floppy Disk controller, companion to ForthCard and C-Board High Level Language single board computers with firmware supporting 40 or 80 cylinder single or double sided 5 1/4" diskette drives, double density.			
Host Adaptor. Four MB/s intelligent 5651 channel controller for PC/XT.				Floppy disk controller for 2S2D floppy disks.			
WDSCS-XTS Western WD7000-ASC Western				Floppy disk controller for 5 1/4' & 3 1/2' drives; utilizes WD1773 device.			
10				DSD2430 Davidge			
IBM PC Host Adapter. Designed for SCSI single host/multiple controllers configuration.							
OMTI510 SMS							
SCSI interface with real-time clock and Centronics interface. Double width, supports DMA. Full SCSI interface to disk and tape controllers. FIFO buffered Centronics interface.							
SCSI-CP SBE							
SCSI to 9-track 1/2 inch tape interface.							
IoSCSI902 IoInc							
<b>STDbus</b>							
<b>Communications</b>							
Available in three configurations, dual asynchronous RS-232, dual asynchronous RS-422, and dual asynchronous RS-232 and RS-422 ports.							
DSPXXX Matrix							
Bell 103 compatible modem.							
SB8630 MicroSys							
Coaxial Cable Modem with UART, Data Rates to 10.2K Baud.							
SB8601 MicroSys							
Communication controller, RS-422, 232, link and error recovery protocols supported.							
7413 Sensoray (4901)							
Parallel card with 32 I/O software selectable inputs or outputs.							
PIA Matrix							

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDBus</b>							
<b>Controllers (Cont'd)</b>							
Floppy disk controller supports 3 1/2", 5 1/4" and 8" drives including AT type drives; utilizes WD1793.	DSB2434	Davidge	5	Stepper motor controller. Intelligent stepper motor controller with optically isolated on-board uni-polar drivers. Powerful macro command set. Uses external power supplies for quiet bus operation.	STEP-2	CompDyn	25
Floppy disk with DMA (Z80).	05364	STDMicro		Stepper motor controller/driver, full, half, or user defined step sequence, 256 byte non-volatile memory, up to 65,536 steps per move command.	SM2	AdvMicroSys	
Floppy disk, 3-1/2, 5-1/4, or 8 inch drives, DMA, CMOS version	FLP380	CompDyn		Stepper motor controller with two-axis smart chopper driver.	sm4 SM4	AdvMicroSys AdvMicroSys	
GPIB Controller—controller/talker/listener; for use in GPIB controllers (master): includes driver software and cable.	ZT 7488/28	Ziatech		Stepper Motor Driver. L/nR type driver controls current through the windings of a four-phase stepper motor (3A/phase). Intended for use with models 4302, 4310, and 4316.	4313	Tech80	
Hard disk, interface 3-1/2, 5-1/4, 8 inch Winchester ST506, or SA1000	WIN358	CompDyn		Stepper motor, intelligent control of any 3, 4, or 5 phase stepper motors in full-step or half-step mode, SBX connectors permit expansion to 3 or 4 axis control using 4316 modules	4310	Tech80	30
High performance single axis intelligent motor controller.	SM2A	AdvMicroSys	10	Stepper motor, 3 axis, consists of one 4310 and an attached 4316 module	4317	Tech80	
IEEE-488 controller	CDI488	CompDyn		Stepper motor, 4 axis, consists of one 4310 module and two attached 4316 modules	4318	Tech80	
IEEE-488 (GPIB), TMS9914, Talker, Listener, Controller, 9511 Math Processor socket, software drivers in C source form for GPIB and Math functions. LED status on GPIB control lines, latches for Z interrupt vectors, 1 parallel port.	STD1003	Zapco		Synchronous data link control (SDLC), DMA compatible.	SB8451	MicroSys	
Intelligent four axis motor controller. Provides PC users with the ability to directly control up to four stepper motors.	PCMC	AdvMicroSys		Universal floppy disk controller with 16/20-bit DMA. 3 1/2", 5 1/4", 8" Floppies	SB8520	MicroSys	
Intelligent motor controller unit.	SMC22	AdvMicroSys	15	Video display card. Offers color or monochrome alphanumeric or graphics video with "snow-free" access, display. To 96 lines, to 128 columns, resolution 640 x 240.	10301	Enterprise	35
Latching relay card for power switching, 8 latching relays with 2 form A high-current contacts for control switching. Relays retain position with power off.	CE4503	Conway		Video display generator, 64 character x 28 lines with programmable character size.	VID64	VersaLogic	
Latching relay card for telephone switching, 8 latching relays with 2 form C contracts for telecommunications switching. Relays retain position with power off.	CE4502	Conway		Video display generator, 80 character x 28 lines with programmable character size.	VID80	VersaLogic	
Low cost floppy disk controller.	SB8500	MicroSys		Single channel stepper motor controller with full or half step operation. 13 to 10,000 pps step rate.	SSC10K SSC5K	Matrix Matrix	
Microfloppy disk drive controller card.	ipc-DISK-0	Vesta		Dual channel stepper motor controller with full or half step operation. 13 to 10,000 pps step rate.	DSC10K DSC5K	Matrix Matrix	40
Printer driver card, 2 parallel printer ports, CMOS version	PTR351	CompDyn	20	Dual independent axis intelligent motor controller.	SM3	AdvMicroSys	
Programmable controller. Supports 40 I/O signals.	7412	Sensoray (4901)		Dual multiprotocol communications controller for Z80.	SB8412 SB8422	MicroSys MicroSys	
Programmable cross-hair generator and digitizer unit.	PCHG4P	AdvMicroSys		Four channel DMA Controller, 16-bit memory address.	SB8341	MicroSys	
SASI host adaptor. Supports up to eight SASI controllers for up to 16 physical disk drives. Two 8-bit parallel ports, one for data and one for status.	STD603	Micro-Link		Four channel DMA Controller, 20-bit memory address.	SB8345	MicroSys	45
SASI/SCSI/DMA/FDC, supplies WD2793 FDC for 3-1/2, 5-1/4, or 8-inch drives, up to 4 in any combination, BIOS for CPM available	80-0019	MicroAide	20	Four-phase power switch, controls current through the windings of a four-phase stepper motor, intended for use with 4302	4306	Tech80	
Servo motor controller. For one or two axis. Provides intelligent position and velocity control for DC servo motors with programmable velocity profiling. Encoder and limit switch feedback, DAC output, and PWM pulse and direction outputs.	4322	Tech80		Four-phase stepper motor. Controls step rate, acceleration, number of steps, and direction of rotation	4302	Tech80	
servo motor controller for one axis. Provides position and velocity control for one DC servo motor, with programmable velocity profiling. Inputs are provided for encoder and limit switch feedback. motor control is through a DAC output and PWM pulse and direction signals.	4321	Tech80		Five amp power drive expander. Slave for SM1, SM2 or ST60	ST60S	AdvMicroSys	
Servo motor controller for one or two axis. Provides intelligent position and velocity control for DC servo motors with programmable velocity profiling. Encoder and limit switch inputs; on-board amplifiers provide up to 2A of PWM output.	4327	Tech80		Five channel system timing and counting.	SB8355	MicroSys	50
Servo valve controller: mostly CMOS; on-board 8-bit DAC and servo amplifier; full STDBus compatibility + 5V @ 65mA, +/- 12V @ 25mA.	STD-SVC1	Intelicom		16 Channel Z80 Mode 2 interrupt controller, 16 Channel Counter Timer, or Combination.	SB8303	MicroSys	
				16 Channel 8085, 8088 priority interrupt Controller.	SB8301	MicroSys	
				24x80 Alphanumeric CRT controller.	SB8320	MicroSys	

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\* Typical Value

° Macrocell

◇ Available in Surface Mount Package

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDbus</b>							
<b>Controllers (Cont'd)</b>							
6502 Single card computer controller with mixed RAM, ROM Sockets, 1 serial port, 2 parallel ports and 4 timers. Power fail, interrupt, and memory protection circuitry allow CMOS RAM to be battery backed.	10812	Enterprise		Eight channel user configurable 12-bit A/D converter. Each channel front end is multiplexed by relays, back end multiplexed by FET multiplexers. On-board microprocessor runs BASIC. 1000 volts isolation to bus.	MT11007	Miller	
6809 Single card computer controller with mixed RAM, ROM Sockets, 1 serial port, 2 parallel ports and 4 timers. Power fail, interrupt, and memory protection circuitry allow CMOS RAM to be battery backed.	10809	Enterprise		Eight Channel, 12 Bit 0–20ma D/A Plug-in.	SB8278	MicroSys	
<b>Converters</b>				Eight independent D/A converters with separate configurable output channels.	LPM-D/A8	WinSystems	
A/D converter. Provides conversions on eight single-ended channels, with 12-bit resolution. Input voltage ranges are $\pm 5$ volts or 0 to 10 volts. Features programmable gain and eight opto-isolated external input lines.	4328	Tech80		Eight-channel A/D, 14-bit resolution, conversion to engineering units	SMART A/D	CompDyn	
A/D Converter; CMOS 16-channel 12-bit A/D Converter card; 16 single-ended or 8 differential inputs; Input voltage –10V to +10V in four ranges; programmable amplifier.	ADC12	Intelicom		12-bit successive approximation A/D converter with 16 single-ended or 8 differential inputs.	LPM-A/D12	WinSystems	30
A/D converter. Intelligent data logger, performs waveform capture. Includes 12-bit A/D, 8/16 channel multiplexer.	7411	Sensoray (4901)	5	12-bit 32 channel analog input and 2 channel analog output. Processor independent.	MCM-A10	WinSystems	
A/D converter, 8-channel, 15-bit, $\pm 10$ V to $\pm 20$ mV in five ranges. Measures resistance, current, thermocouples, RTD's and thermistors. Has DC/DC converter, DSP function.	7408 7409	Sensoray (4901) Sensoray (4901)		120-bit successive approximation A/D converter with 16 single-ended or 8 differential inputs. On-board programmable gain instrumentation amplifier for 5 input ranges.	MCM-A/D12	WinSystems	
A/D, D/A, 4 12-bit analog outputs, eight 15–1/2 bit inputs	DAD48	CompDyn		12-bit A/D converter card. CPU-controlled conversion provides channel selection and free run. Conversion completion signalled by interrupt or status bit.	STD581	Micro-Link	
D/A, 12-bit resolution, drives a 2 A load over full output voltage range	4307	Tech80		12-bit analog input/output board. 32 input and 2 output channels. All CMOS, very low power, extended operating temperature range: –40°C to +85°C.	LPM-A10	WinSystems	
DC-DC converter board	DT2715	DataTrans	10	12-bit high-speed A/D converter. 25 microsecond conversion time, on-board DC/DC converter. Supplies $\pm 12$ volts to analog circuitry.	STD541	Micro-Link	35
Digital to analog, 8-bit, eight channels.	MCM-D/A8	WinSystems		12-bit high-speed D/A converter. One microsecond conversion time, bipolar outputs. On card precision voltage reference.	STD539	Micro-Link	
Encoder to Computer Interface Module.	C1510	Buckminster		16 channels of single-ended/8 differential expandable to 32 single-ended/16 differential. 12-bit resolution in 25 $\mu$ s settling time.	ADC12	Matrix	
four-channel, 8-bit digital to analog.	DT2727	DataTrans		<b>Data Acquisition Systems</b>			
four-channel, 12-bit digital to analog.	DT2726	DataTrans		High-speed data acquisition card. 8088 compatible with 32K dual-port RAM, block acquisition, sample & hold, 500K samples/sec., available in 8, 10, or 12-bit resolution.	ACQ	AdvMicroSys	
Frequency to digital, 2 channel, 8-bit dual port RAM data access, continuous conversion input frequencies to 10 KHz	750	Atec	15	Sensor-based 16-channel single-ended and 16-channel differential inputs, 12-bit resolution.	RTI1270	AD	
High speed data acquisition card.	ACQ16	AdvMicroSys		<b>Graphics</b>			
Synchro/resolver to digital, memory mapped onto STDbus address array, 16-bit address decoding	771-0	Atec		High-resolution color graphics board	STD800	Matrox	40
Triple 8-channel 8-bit analog to digital (Z80).	05340	STDMicro		Intelligent color graphics controller card. On-board MC6809 processor and TMS9118 video processor. 256x192 resolution with 16 colors and reverse video. On-board line, circle, and arc generation. Can be used for plotting charts.	STD602	Micro-Link	
One 16-bit synchro-to-digital or resolver-to-digital converter.	5405C	Transmag		Universal color video display	CRT-VDP	Datricon	
Four channel D/A	862	Octagon	20	Video Overlay. Synchronizes 1 or 2 CRT controllers to incoming RS170/CCIR/NTSC. Supplies pixel clock to CRT controller. Inserts TTL video signals from CRT controller into video. Compatible with STD–100 Video surround attribute.	VOSTD	KSystems	
Four independent analog voltage output channels convertible to four channels of 4 to 20 mA current loop. 12-bit resolution in 25 $\mu$ s settling time.	DAC12	Matrix		<b>I/O</b>			
Four independent double buffered 12-bit current (4 to 20 mA) channels, memory or I/O map with expansion	LD62DA-I	LupiData		A/D converter, 16 single-ended or 8 differential input channels, 10-bit resolution	RTI1226	AD	
Four independent double buffered 12-bit D/A voltage channels, memory or I/O map with expansion	LD62DA-v	LupiData		Analog I/O board, 12 bits (Z80).	MK78172-42 MK78172-56 MK78175-40	Thomson Thomson Thomson	45
Sixteen Channel, 12 Bit A/D Plug-in.	SB8277	MicroSys					
Eight channel D/A converter with 13-bit resolution. On-board microprocessor runs BASIC. Outputs are buffered and protected. 1000 volts isolation to bus.	MT11033	Miller	25				

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\* Typical Value

° Macrocell

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MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDBus (Cont'd)</b>							
<b>I/O</b>				Centronics w/Serial SBC (8088).	05822	STDMicro	
Analog I/O, 16 single-ended and 8 differential inputs, programmable gain, 8 analog outputs, 12 bit resolution	RSD7728	Robotrol		CMOS decoded I/O utility prototyping board. CMOS replacement for Pro-Log 7914 or 79C04.	VL79C14	VersaLogic	30
Analog I/O, 16 input channels, two output channels. Eight bit resolution. Input voltage ranges: 0-5 V, 0-10 V, $\pm 5$ V.	864	Octagon		CMOS Multimode Parallel Interface, Six Port	SB84C66	MicroSys	
Analog input board	DT2712	DataTrans		CMOS RS232 Interface, Three-Channel	SB84C23	MicroSys	
Analog input expander for additional 48 single-ended or 24 differential channels.	DT2734	DataTrans		CMOS version of VL-7304 serial I/O. Direct plug-in replacement for Pro-Log 7304.	VL73C04	VersaLogic	
Analog input has 16 single-ended or 8 differential inputs. 12 bit resolution with ranges of 0-5, $\pm 5$ , 0-10, $\pm 1$ -10, 0-20 ma. Expands to 64 channels with slaves.	S868	Contemporary	5	CMOS version of VL-7507 24-line I/O. Direct plug-in replacement for Pro-Log 75C07.	VL75C07	VersaLogic	
Analog input, 16 single-ended, 8 differential, 12-bit A/D, CMOS STDBus.	RTI1280	AD		CMOS version of VL-7508 48-line I/O. CMOS replacement for Pro-Log 7508.	VL75C08	VersaLogic	
Analog input 16/32 single-ended or 8/16 differential channels. 12-bit A/D.	860	Octagon		Communications, 212A modem with 1200/300 baud and optional touch-tone receiver, one serial RS-232 and one RS-422/488, may be memory or I/O mapped	80-0029	MicroAide	35
Analog input, 8 channels with 12 bit resolution and noise tolerant conversion.	AIN-1A AIN-1B	VersaLogic VersaLogic		Configurable parallel I/O	TTL64	Datricon	
Analog output, four 12 bit outputs provide 0-5, $\pm 5$ , 0-10, $\pm 1$ -10, or 4 to 20 ma output standard	S864	Contemporary	10	Counter/timer. Three 16-bit counter/timer channels with six operating modes each, on-card crystal oscillator and clock driver, 8-input count source multiplexer.	308	Octagon	
Analog output, 4 channels, 12-bit resolution, CMOS STDBus.	RTI1282	AD		D/A converter with four output channels. 12-bit resolution. output voltage ranges: 0-5V, 0-10V, $\pm 5$ V, $\pm 10$ V.	862	Octagon	
Analog output, 12 channels, 12-bit resolution	RSD7712	Robotrol		Decoded I/O utility prototyping board. Direct replacement for Pro-Log 7914.	VL7914	VersaLogic	
Analog output, 4 channels with 10 bit resolution. 0-10 volt output range.	AOUT-1	VersaLogic		Digital I/O, 24 signal channels, three 8-bit read/write ports for 24 bidirect lines, CMOS STDBus.	RTI1287	AD	40
Analog processor, 16 analog channels with 8-bit resolution, 24 TTL I/O channels, monitoring and data acquisition software package included	LD8038	LupiData		Digital-Input/Output Board.	MK77672	Thomson	
Analog subsystem combination, 16 single-ended, 8 differential analog inputs, two analog outputs, 10-bit resolution.	RTI1225 RTI1281	AD AD	15	Digital-Input/Output Panel.	MK77673	Thomson	
Analog subsystem, four analog output channels, 12-bit resolution, memory mapped or port I/O selectable.	RTI1262	AD		DMA with/RS-232/449 Serial SBC (8088).	05826	STDMicro	
Analog subsystem, 16 single-ended, 8 differential analog inputs, 10-bit resolution.	RTI	AD		FFT with/RS-232/449 Serial SBC (8088).	05825	STDMicro	
Analog subsystem 32 single-ended, 16 differential analog inputs, 12-bit resolution, memory mapped or port I/O selectable.	RTI1260	AD		Floppy-disk controller.	MK77677	Thomson	45
Analog to digital converter, 8-channel differential dc amplifier, multiplexer and controller	DA505	Validyne		Floppy-disk interface (Z80).	MK78146	Thomson	
Analog to digital input (Z80).	MK78177-26	Thomson	20	For use with LVDT, RVDT and variable reluctance transducers. 13-bit resolution, 8 channels	CD501	Validyne	
Bar code interface, stand alone or STDBus interface, prints and reads codes 39, UPC, EAN, ad 2/5.	7415	Sensoray (4901)		For use with strain gauge transducers, 13 bit resolution, 8 channels	SG502	Validyne	
Bell 212A modem card. Meets Bell 103/113 and 212A specifications. 300 or 1200 bps asynchronous operation. May be programmed for auto answer, auto originate and pulse dialing.	STD403	Micro-Link		Full STD bus 64-line TTL input/output interface board.	SB8464	MicroSys	
Bridge transducer interface, 2 channel, 8 bit resolution, complete signal conditioning and continuous A/D conversion, dual-port RAM	740	Atec		GPIO (IEEE-488) Listener/Talker utilizes TMS9914A device.	DSB2427	Davidge	50
Calendar clock with battery backup using the MM58167A for the Z80C, NSC800, 80C85, and 80C88 processors. Includes a watchdog timer.	LPM-CLK LPM-CLK-2	WinSystems WinSystems	25	GPIO Interface—talker/listener; for use in GPIO devices (slave); includes driver software and cable.	ZT 7488/08	Ziatech	
Camera interface card; mostly CMOS interface for Reticon LC600 line scan camera; Z80 compatibility: $\pm 5$ V @250 mA.	STDCAM1	Intelicom		GPIO Listener/talker/controller w/DMA (Z80).	05388	STDMicro	
				GPIO w/Serial SBC (8088).	05828	STDMicro	
				High-level analog input, 16 single-ended or 8 differential channels, 12-bit resolution.	DT2722 DT2742	DataTrans DataTrans	55
				High-speed opto-input provides 24 inputs from 5 Vdc to 110 Vac, address switch selectable for 8- or 16-bit memory or I/O mapping	80-0034	MicroAide	
				High-speed opto-output provides 24 opto-coupled outputs, address switch selectable for 8 or 16 bit memory or I/O mapping	800035	MicroAide	
				I/O module interface. Connects to industry standard Opto-22 type interface racks. Two independent control channels, up to 24 I/O modules per channel.	STD722	Micro-Link	
				I/O Rack module interface (Z80).	05382	STDMicro	
				IEEE-488 Controller and general purpose I/O Functions, DMA Compatible.	ZT8847 ZT8848	Ziatech Ziatech	60

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDbus</b>							
<b>I/O</b>				<b>(Cont'd)</b>			
IEEE-488 interface card. Utilizes TMS9914A GPIB controller, provides all functions including listener/talker, controller, and system controller.	STD401	Micro-Link		one asynchronous RS-232 serial port, two 8-bit parallel-input, and two 8-bit parallel output ports.	LPM-SPI0A	WinSystems	
Incremental shaft encoder interface, provides signal conditioning and angular data formatting for optical shaft encoders.	775	Atec		Opto input, eight channels, input voltage range from 70 Vrms to 140 Vrms ac.	506	Octagon	
Intelligent I/O board with 8751H processor. Links IBM PC to STD bus, EPROM programmer and printer, firmware and software available.	LM-1 Linker	Devtek		Opto input/output, 4 opto-isolated inputs, four solid state relay outputs. Zero crossing power switching. Built-in snubber network.	500	Octagon	
Intelligent 488 with Z80 on-board, Talker/listener/controller.	TBD	Thomson		Opto input, 24 opto-coupled inputs from 5 Vdc to 110 Vac, may be memory or I/O mapped by 8- or 16-bit address	80-0023	MicroAide	
Interface card to the OPTO-22 PB-8, PB-16, and PB-24 racks.	MCM-7507	WinSystems		OPTO 22/Gordos compatible I/O card with 48 lines terminated bidirectional TTL, four event sense software controllable interrupts; 8 or 16-bit I/O decoding	ZT8845	Ziatech	35
Interface, connects to 8, 16, or 24 channel opto-22 relay boards, protected filter inputs, may be memory or I/O mapped by 8- or 16-bit address	80-0022	MicroAide	5	Opto-isolated I/O card. Eight channels can be configured as input or output. AC/DC inputs up to 250 volts, DC output to 60 volts.	STD700	Micro-Link	
Interface for platinum RTDs, on-board linearization, 13-bit resolution, 8 channels	PT503	Validyne		Opto-output/relay, provides 24 opto-coupled outputs plus one latching relay (form C), may be memory or I/O mapped	80-0030	MicroAide	
Interface for thermocouples (E, J, K or T), on board linearization, 13-bit resolution, 7 channels plus 1 reference channel	TC504	Validyne		Opto-output, supplies 24 opto-coupled outputs, may be memory or I/O mapped by 8- or 16-bit address	80-0025	MicroAide	
Interface to opto-22 I/O module racks. 24 bi-directional buffered I/O lines.	507	Octagon		Opto-Triac output, supplies 24 MOC3011 opto-triac outputs, may be memory or I/O mapped by 8- or 16-bit address	80-0024	MicroAide	
Interface to Opto-22 I/O module racks. 48 bi-directional buffered I/O lines. Drives two module racks.	508	Octagon	10	Parallel and serial I/O card. Two 8-bit parallel ports, Centronics compatible. Two RS-232-C full-duplex ports, three 16-bit counter/timers.	STD701	Micro-Link	40
Interface to Opto-22, PB-8, PB-16 and PB-24 racks.	LPM-PI03	WinSystems		Parallel, four 8-bit input and four 8-bit output ports.	MCM-PI02	WinSystems	
Interface to Opto-22, 16 lines	PI/O-16	CompDyn		Parallel I/O board. High current, high voltage, open-collector output. Software and hardware programmable as input or output. ProLog 7605-0 compatible.	HPIO-64	CompDyn	
Interface to Opto-22, 48 lines	PI/O-48	CompDyn		Parallel I/O, CMOS industrial interface card; 24 bi-directional lines; drives industry standard I/O Module Racks; Precision interval clock.	CMOSP10	Intelicom	
Interface to Opto-22, 64 lines	PI/O-64	CompDyn		Parallel I/O with four buffered programmable 8-bit ports with handshake. Supports Z80 mode 2 interrupts.	LPM-PIO	WinSystems	
Interfaces with industry standard optical isolator module racks. 24 bidirectional I/O lines.	805	Octagon	15	Parallel industrial module (PIM) with 16 channels. Designed for use with opto-isolated I/O relay modules manufactured by OPTO-22, Gordos, and Crydom, etc.	PIM	Matrix	45
Isolated analog input expander for 8 additional differential-input channels.	DT2735	DataTrans		Parallel interface for the Opto-22 PB-8, PB-16, and PB-24 type modular racks.	MIO-24	VersaLogic	
Isolated input and relay output, 4 channels of each.	IPI-4	VersaLogic		Parallel, with 64 I/O lines total, 4MHz operation.	MCM-PI01	WinSystems	
Isolated input and solid state relay output, 4 channels of each.	IPI-5	VersaLogic		Parallel, 24 bidirectional lines.	MCM-7507	WinSystems	
Isolated input, 8 channels, up to 250 volts ac or dc with status indicators.	IPI-1	VersaLogic		Parallel, 56 lines, 3 connectors	UPIO	Sys Datar	
Isolated low-level analog inputs with four differential-input channels.	DT2725 DT2745	DataTrans DataTrans	20	Photosensor board with parallel input/output. Eight channel photosensor input with LED drive, high sensitivity, high-speed, and high noise rejection.	PC-108	ElecConServ	50
Isolated RS-422 Serial I/O.	MK77671	Thomson		PIO with Serial SBC (8088).	05823	STDMicro	
Low-level analog input, 16 single-ended or 8 differential channels, 12-bit resolution.	DT2724 DT2744	DataTrans DataTrans		Printed circuit board for prototyping I/O circuitry	STI-DIO STI-DIO-C	Solarcom Solarcom	
Medium power driver (MPD) is a 24 channel DC output power driver to control indicators, relays, or other current/voltage devices in control systems.	MPD	Matrix	25	Programmable I/O card. Up to 40 parallel I/O lines programmable as input, output, or bi-directional. One RS-232-C port with baud rates to 19.2K.	STD729	Micro-Link	
Medium power output driver card, 32 channels of four 8-bit write only ports. Switches up to 0.3A at up to 30 volts.	STD740	Micro-Link		ProLog 760x compatible parallel interface board. Includes watchdog timer with +5V supply monitoring. Solid ground connection which reduces RFI and noise problems.	PIO-760x	CompDyn	55
Multi-channel communications controller (Z80).	MK78192	Thomson		Relay, eight output channels, normally open or normally closed contacts, 2 A at 125 Vac/24 Vdc, resistive; 0.5 A at 125 Vac/24 Vdc, inductive.	502	Octagon	
Multi-Unit Winchester Floppy Disk Controller and SCSI/SASI Interface on Board.	ZT8850	Ziatech					
Multichannel serial board—four independent INS 8250 UARTs; programmable baud rates to 56K; wait state generator; on-board 8259 interrupt controller; loopback diagnostic capability.	ZT 8840	Ziatech					
Non-isolated RS-422 Serial I/O.	MK77676	Thomson	30				

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDbus (Cont'd)</b>							
<b>I/O</b>				STD-Z80 compatible I/O with four programmable 8-bit TTL I/O ports with handshake.	MCM-P10	WinSystems	
Relay output card—eight relays SPST (optional mercury wetted SPST or SPDT), LED display of relay status; CPU readable relay status.	ZT 7502/10/40/or 60	Ziatech		STD-Z80-BUS to SASI interface.	MK77678	Thomson	
Relay output card with eight SPDT relay channels.	RLC	Matrix		STD-Z80-BUS to SASI interface with DMA.	MK77679	Thomson	30
Relay output, eight 280Vac 2 amp solid state relay outputs. Zero crossing power switching. Built-in snubber network.	504	Octagon		Touch Tone Interface, connects STDbus to telephone line for encoding and decoding DTMF (touch tone) signals. Can be used with other cards to build remote alarm and control system.	CE4000-2	Conway	
Relay output with 24 channels N.O. or N.C. Used to switch low-level signals and in situations where leakage must be avoided.	RLY-24	CompDyn		TTL Compatibles I/O points.	G7507	Gordos	
Relay output, 8 channels N.O. or N.C. up to 1.25 A, CPU readback with status indicators.	IPI-2	VersaLogic		Universal TTL I/O board, provides 8 ports (64 lines) of TTL I/O with readback. May be populated for input or output with readback on a port basis.	10611	Enterprise	
RS-232 to RS-422 translator card.	VSCTR	Gordos		Up to 40 TTL input/output channels and 4/8 counter/timers	LD8040-IO	LupiData	
RS-232/449. Serial w/Centronics (Z80).	05374	STDMicro		Waveform capture and data logging A/D, expandable up to 128 channels of voltage or thermocouple input, 12-bit resolution.	7411	Sensoray (4901)	35
RTD interface for eight channels, 0.4 C/bit resolution.	7404	Sensoray (4901)		Winchester disk Controller Interface (SASI/SCSI).	SB8740	MicroSys	
SCSI Host adaptor w/DMA (Z80).	05386	STDMicro		Dual channel STD-Z80 multiprotocol synchronous or asynchronous serial I/O with RS-232 or 20mA opto-isolated current loop. Modem control signals, supports Z80 vectored interrupts.	MCM-S102	WinSystems	
SCSI host/target interface utilizes NCR5380 device.	DSB2428	Davidge		Dual PIO (Z80).	05380	STDMicro	
Serial I/O, dual RS232 ports	Z80S102	Datricon		Dual RS-232-449 Serial SBC (8088).	05824	STDMicro	
Serial I/O, dual RS232/422 with 20 mA current loop, 6809 only	SER02B	Datricon		Dual RS232 (DART) Serial Interface (Z80).	05370	STDMicro	40
Serial I/O, dual RS232/422 with 20 mA current loop	SER04	Datricon		Triple RS232/449 (DART) serial interface (Z80).	05373	STDMicro	
Serial I/O, fully CMOS Dual UART card; two full duplex RS-232-C channels provided (DTE or DCE); programmable 50-9600 baud rate; supports mode 2 interrupts.	CMOSSIO	Intelicom		Quad channel RS422 serial interface for Z80.	SB8414	MicroSys	
Serial I/O, quad RS232/422 ports	Z80S104	Datricon		Quad channel serial interface provides RS 232/422/485 protocol.	SER08	Datricon	
Serial input adapter with Sync Code Detector, iSBX module contains 128-bit digital correlator to detect any size sync code up to 128 bits, input is serial NRZI data up to 5Mb/sec, outputs are 8- or 16-bit data to iSBX interface	LMSBX108	LitMach		Quad RS-232 DART with interrupt controller and SBX connector, programmable baud rates on each channel	5101	Systek	
Serial interface, two channels, one each RS-232 and RS-422.	SIO-2B	VersaLogic		One asynchronous RS-232 serial port, one eight-bit TTL input and one eight-bit TTL output port; two combination 8-bit TTL I/O ports.	MCM-SP10	WinSystems	45
Serial interface, two RS-232 channels up to 19.2K baud.	SIO-2A	VersaLogic		Two asynchronous RS-232 or opto-isolated 20mA current loop serial channels with modem control.	MCM-DS10	WinSystems	
Serial, six independent sync/async RS-232C serial ports, 12 independent baud rate generators 50-38.4k, Parallel lines, 21 in/24 out (for modem control or misc), 3 counter/timers, Automatic RTS/CTS handshake.	STD1006	Zapco		Two asynchronous RS-232 serial or opto-isolated 20mA current loop ports, selectable baud rate 110-9600.	LPM-DSIO	WinSystems	
Serial, two full-duplex programmable serial I/O channels.	MCM-SIO2	WinSystems		Two channel USART card. Two RS-232-C ports with programmable baud rates to 19.2K, full or half-duplex operation.	STD435	Micro-Link	
Serial, two serial UART channels opto-isolated current loop, jumper selectable baud rate generator for 110 to 9600 baud.	MCM-DSI/O	WinSystems		Two RS-232 channels, 4/8 counter/timers, 16 multi-purpose I/O channels	LD8040-P	LupiData	
Serial UART board using two 8251 devices. Two RS-232 channels. Replaces Pro-Log 7304.	MCM7304	WinSystems		Two RS-422/485 serial channels, parity and stop bits, software-programmable baud rate (19.2K)	LD8040-C	LupiData	50
Serial, 2 channels of fully configurable RS-232C communications, synchronous or asynchronous	SI/O-2	CompDyn		Two 8251 UARTS for serial asynchronous communications. -40°C to +85°C operating temp. Replaces Pro-Log 7304.	LPM7304	WinSystems	
Serial, 4 channels of fully configurable RS-232C communications, asynchronous	SI/O-4	CompDyn		Two-channel programmable Serial I/O.	MK77670	Thomson	
Serial 4-port RS232, RS422, synchronous, asynchronous, to 19.2 Kbaud	SCC	Sys Datar		Two-Channel RS232C/20mA serial interface with 256 byte bootstrap PROM socket.	SB8420	MicroSys	
Serial-parallel, one serial UART channel, opto-isolated current loop, jumper-selectable baud rate generator for 50 to 19200 baud.	MCM-SPI/O	WinSystems		Four channel serial I/O card using 8251. Supports cascable interrupts with an 8259 PIC RS-232 or TTL output levels	MCM-S104 MCM-5104	WinSystems WinSystems	55
Solid state relay output, 8 channels, up to 250 Vac at 1 A. CPU readback and status indicators.	IPI-3	VersaLogic		Four channel serial I/O using 82C51. RS-232 or TTL output cascable interrupts supported with 82C59 PIC	LPM-SIO4	WinSystems	
				Four channel serial interface card. Z80 bus compatible (4 MHz). Two RS-232-C ports, two RS-422/485 ports, programmable baud rates to 19.2K baud.	STD402	Micro-Link	

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

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°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDbus (Cont'd)</b>							
<b>I/O</b>				32 TTL Compatible I/O points, interfaces G7507 card to industry standard PB-32 I/O module board.	PAM3	Gordos	
Four channel USART card. Four independent RS-232-C ports, programmable baud rates to 19.2K bps. Full or half-duplex operation.	STD436	Micro-Link		32 TTL Compatible I/O points, 8 quad I/O modules on board are drives by G7507 card.	PAM2	Gordos	30
Four independent async/sync RS-232 serial channels using the Z8530 scc. Replaces Pro-Log 7314.	MCM7314	WinSystems		32-bit parallel I/O	Z80PIO	Datricon	
Four independent async/sync serial channels using SCC chip. -40°C to +85°C operating temperature.	LPM7314	WinSystems		32-bit parallel I/O with counter/timers	VIA02B	Datricon	
Four to 20 mA loop controller, 4 channel, 8-bit resolution, external control loop excitation of 12 to 32 volts	730	Atec		32-bit programmable parallel I/O.	MK77650	Thomson	
Four 6522 VIAS for up to 64 I/O lines, may be memory or I/O mapped	80-0032	MicroAide	5	32-digit display driver 1 digit per memory location	701	Atec	35
Four 12-Bit output channels, Analog Devices replacement.	VL1262	VersaLogic		32-Line digital, Plug-in.	SB8276	MicroSys	
Four-channel 12-bit D/A.	MK77665	Thomson		48 line digital interface to Opto-22 Racks. -40°C to +85°C operating temperature range.	LPM7508	WinSystems	
Four-channel 8-bit D/A.	MK77666	Thomson		48 line digital interface to Opto-22 Racks. Replaces Pro-Log 7508.	MCM7508	WinSystems	
Six channel serial I/O card with two, four, or six RS-232-C ports. Baud rates programmable to 19.2K bps. Full or half-duplex operation.	STD460	Micro-Link		48-bit parallel I/O	VIA04 Z80P103	Datricon	
Six RS-232 serial ports, two interrupt timers, supports all Z80 interrupt modes	80-0021	MicroAide	10	48-line Opto 22 or general purpose parallel I/O interface. Direct plug-in replacement for Pro-Log 7508.	VL7508	VersaLogic	40
Six-port multi-mode parallel Interface.	SB8466	MicroSys		64 line digital interface. All CMOS, -40°C to +85°C operating temperature. Replaces Pro-Log 76C14.	LPM7614	WinSystems	
Eight optically isolated input channels for sensing the status of AC and DC control signals and interfacing them to the STDbus control systems.	ADI	Matrix		64 line digital interface. Replaces Pro-Log 7614.	MCM7614	WinSystems	
Eight-bit D/A converter with 8 independent input channels. Each channel has separate configurable output ranges.	MCM-D/A	WinSystems		64 parallel I/O lines; four 8-bit input, four 8-bit output ports.	LPM-PI02A	WinSystems	
Nine independent 16-bit counter timers using 82C54. Supports 8259 PIC for interrupts. All CMOS. -40°C to +85°C operating temperature.	LPM-CTC	WinSystems		64 parallel I/O lines; two 8-bit input, two 8-bit output, and four 8-bit combination ports.	LPM-PI01A	WinSystems	
Nine independent 16-bit counter/timers using 8254A. Onboard 8259 PIC for interrupts.	MCM-CTC	WinSystems	15	64 switch inputs, accomodates 64 independent static inputs, reads inputs from a variety of types of switches, and reads logic levels.	8304	Tech80	45
4 to 20 mA input, 7 channel, 8-bit resolution, open-loop detection of eighth channel	735	Atec		64-line TTL I/O interface. Direct plug-in replacement for Pro-Log 76C14.	VL76C14 VL7614	VersaLogic	
16 inputs with interrupts. Allows interrupt/status generation on state transitions of any or all of its 16 opto-isolated inputs	4314	Tech80		96 bidirectional TTL I/O lines grouped into 12 ports with eight channels each.	832	Octagon	
16 opto-sensor inputs, latched. Accomodates 16 directly connected opto-sensors, 4 inputs operate in a priority interrupt/status mode, selectable interrupt vectors	4304	Tech80		96 TTL channels, software programmable as input/output, memory or I/O map with expansion	LD96IO	LupiData	
16-channel high-level 12-bit A/D.	MK77655	Thomson		1200/300 Full Bell 212A/103 modem compatible with industry standard AT command set. Auto answer/Autodial.	MCM-MODEM	WinSystems	50
16-channel i-bit A/D.	MK77674	Thomson	20	16 opto-isolated inputs. Input voltages may range from 5 to 50 volts with not more than 10 mA of current required. Voltage level thresholds are adjustable.	4329	Tech80	
16-digit switch interface, provides memory mapped addressing for up to 16 digits of BCD data, without switches	710-0 710-1	Atec		16 opto-sensor inputs. Accomodates 16 directly connected opto-sensors, 4 inputs operate in a priority interrupt/status mode, selectable interrupt vectors	4305	Tech80	
20-channel counter frequency	CFIO-20	Datricon		16 single-ended/8 differential 10-bit input channels, two 8-bit output channels, Analog Devices replacement.	VL1225 VL1226	VersaLogic	
24 bi-directional parallel channels with darlington outputs, rated to 25V and connector compatible with industrial I/O module racks. Z80 Mode 2 interrupts supported.	Z501	Electrologic		16 single-ended/8 differential 12-bit input channels, optional 32 single-ended/16 differential 12-bit input channels. Analog Devices replacement.	VL1260	VersaLogic	55
24-channel analog I/O	ANA10	Datricon		32 TTL input lines and 32 output lines, Pro-Log replacement.	VL7601A	VersaLogic	
24-line Opto 22 or general purpose parallel I/O interface. Direct plug-in replacement for Pro-Log 7507.	VL7507	VersaLogic	25	64 channel TTL I/O card. Latched output with readback, non-inverting input ports.	STD734	Micro-Link	
32 line digital interface. CMOS STD BUS. -40°C to +85°C operating temperature.	LPM7605	WinSystems		64 CMOS/TTL input and/or output lines, Pro-Log replacement.	VL76C04A	VersaLogic	
32 line digital interface. Replaces Pro-Log 7605.	MCM7605	WinSystems		64 parallel I/O lines organized as four 8-bit input ports and four 8-bit output ports; direct TTL interface levels.	MCM-P102	WinSystems	

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MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDBus</b>							
<b>I/O</b>							
<b>(Cont'd)</b>							
64 parallel I/O lines organized as two 8-bit input, two 8-bit output, and four 8-bit combination I/O ports, direct TTL interface levels.	MCM-P101	WinSystems		I/O accessed byte-wide memory, up to 256K RAM or EPROM	80-0017	MicroAide	25
64 TTL input and/or 64 TTL output lines, Pro-Log replacement.	VL7604A	VersaLogic		Memory board with 32K bytes of static RAM or EPROM/EEPROM.	RPC-32	Matrix	
64 TTL input lines, Pro-Log replacement.	VL7603A	VersaLogic		Program development card, combines up to 32 K battery-backed RAM, an EPROM programmer, power fail circuit and a parallel printer port.	870	Octagon	
64 TTL output lines, Pro-Log replacement.	VL7602A	VersaLogic		PRM programming system for single supply EPROMS.	PS8200	MicroSys	
<b>Mathematics</b>				STD-Z80, 4-MHz 128K dynamic RAM card.	MCM-DRAM 128	WinSystems	
High-speed floating point math.	MK77852	Thomson	5	STD-Z80, 4-MHz 64K dynamic RAM card.	MCM-DRAM 64	WinSystems	30
<b>Memories</b>				STD-80188/8088/8085 compatibility; no wait states at 5 MHz; hidden memory refresh and parity with a non-maskable interrupt; supports MEMEX* bank-switching. Memory capacity also includes 512 Kbytes and 1 Mbyte.	ZY8823	Ziatech	
Add-on memory card. Bank switching, multiple board capabilities expands system to over 40MB. 2MB static RAM, 2MB EPROM, or 128KB EEPROM can be used.	MEGA-MEMORY	CompDyn		Universal battery-backed memory and calendar/clock. Supports up to 24-bit address, works with any processor on the STDBus	80-0031	MicroAide	
Bank-select ROM card	826	Octagon		Universal Memory Card.	MK77763	Thomson	
Battery RAM Card (2Kx8).	MK77762	Thomson		Universal memory card. One megabyte of RAM.	SB8122	MicroSys	
Battery RAM Card (4Kx8).	MK77760	Thomson		Universal memory module.	SB8120	MicroSys	35
Battery-backed memory card with 64K byte capacity.	RP64	Matrix	10	Universal non-volatile memory card mixes up to 64 Kbytes of CMOS RAM, EPROM and EEPROM. Two groups of 4 sockets each may be separately addressed allowing RAM and EPROM to be in different areas of the memory map.	10764	Enterprise	
Battery-backed RAM memory card and real time clock up to 16Kbytes with power-fail detect and write protect logic.	CRC	Matrix		Universal, supports 1 MByte 8088 addressing, bank switchable for 8085s and Z80s, 10-year memory retention, low-battery indicator, up to 256K RAM or 512K EPROM	6440	Systek	
Byte-wide memory board—unpopulated-socketed for byte-wide RAMs, PROMs, EPROMs, EEPROMs; addressable to 1Mbyte on STD Bus; works with 5 or 8 MHz 8088, battery backup.	ZT 8820	Ziatech		Up to 256-Kbyte battery-backed RAM/EPROM, 8 JEDEC sockets	MMC	Sys Datar	
Bytewise memory card. Eight 28-pin JEDEC memory sockets, power-fail protection for RAM. Supports up to 512K EPROM on a single card. 16 and 20-bit addressing.	STD301	Micro-Link		Winchester/Floppy Controller, RAM/ROM, eight byte-wide sockets, each independently configurable for any RAM/ROM type up to 8Kx8, sockets are deselectable, has host adaptor for WD1000, WD1002-05.	STD1002	Zapco	
Bytewise memory card with 512K EPROM, 256K RAM, or 16K EEPROM capacity. Supports 16,20, and 24-bit addressing with on-board battery back-up.	STD304	Micro-Link		Eight 28-pin sockets for 256K RAM or 512K EPROM or mixture. Direct address by 8088 or banking by 8-bit processors.	MEM256-8	Mitchell	40
CMOS Universal Memory Module	SB81C20	MicroSys	15	1M byte dynamic RAM	MS-1DR	Datricon	
CMOS Version of VL-7709 memory board. Direct plug-in replacement for Pro-Log 77C09.	VL77C09	VersaLogic		16 Kbyte RAM (Z80).	MK78109	Thomson	
CMOS 54 Kbyte EPROM card using 27C32 only; Z80, 8085, 6800 compatibility; bank select to 512 Kbyte; 450-ns access time.	CMOS-64K	Intelicom		16K Dynamic RAM.	MK77754-0	Thomson	
CMOS-STD BUS universal memory card with eight 28-pin JEDEC memory sockets for RAM, ROM, or EPROM's. Supports page mode or 1 Mbyte extended address decoding.	LPM-UMC	WinSystems		32K Dynamic RAM.	MK77761-0	Thomson	45
Dynamic RAM board with up to 1 Megabyte using 20 or 24 bit addressing and MEMEX control up to 16 Megabytes.	MS-DR	Datricon		64 Kbyte dynamic RAM module.	SB8130-64	MicroSys	
Dynamic RAM, 128 Kbytes supports 8 and 16-bit processors, transparent on board refresh.	RAM128	AdvMicroSys		64 Kbyte RAM, battery backed	UMEM-64	CompDyn	
Dynamic RAM, 256 Kbytes supports 8 and 16-bit processors, transparent on board refresh.	RAM256	AdvMicroSys		64 Kbyte static RAM or EPROM	SRAM-64	CompDyn	
EPROM and UART.	MK77753	Thomson	20	64/256K byte memory with 16 or 20-bit addressing and optional lithium battery backup. Direct plug-in replacement for Pro-Log 7709.	VL7709	VersaLogic	
Fully CMOS 32 Kbyte Static RAM/ROM card: Z80, 8085, 6800 compatibility; bank select to 512 Kbyte; 250-ns access time.	CMOS-32K	Intelicom		64-Kbyte RAM with two PIO channels (Z80).	MK78110	Thomson	50
High-speed Read/Write memory board with 128K, 256K, 512K, 768K, or 1Mbyte configurations, no wait states at 8 MHz, parity error detection and on-board hidden refresh.	ZT8824	Ziatech		64K byte-wide battery-backed RAM	MSB-64	Datricon	
				64K DRAM with bankswitch capability.	MK77764	Thomson	
				64K/256K byte memory card. Accepts 8K and 32K byte RAMs and EPROMs. Write protect switches, optional battery backup.	829	Octagon	
				128 Kbyte dynamic RAM module.	SB8130-128	MicroSys	
				128/256Kbyte Dynamic RAM board—5 and 8 MHz compatibility, no wait states; on-board memory refresh; parity with a nonmaskable interrupt.	ZT 8821	Ziatech	55

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDbus</b>							
<b>Memories (Cont'd)</b>							
128K byte-wide RAM	MS-128	Datricon		Data and address buffers, I/O decoding, eight separate input and output decoded strobes. 4.2 inch by 4.2 inch grid.	930	Octagon	
128K DRAM with bankswitch capability.	MK77765	Thomson		General utility card with 0.1" grid pattern.	STD897	Micro-Link	
128K static RAM card. Battery backed, write protect switch, clock rates up to 8 MHz. CMOS version available.	820	Octagon		STD bus prototyping module for analog or digital I/O. On-board microprocessor runs BASIC. 1000 volts isolation to bus.	MTI-10XX	Miller	
128K static RAM card. 16 and 20 bit addressing, clock rates up to 8 MHz. CMOS version available.	822	Octagon		Wire Wrap prototype board with address decoding and SBX interface.	WW-DCODE	CompDyn	
256 Kbyte dynamic RAM	DRAM-256	CompDyn		<b>Speech Circuits</b>			
256 Kbyte Dynamic RAM module (8088).	05809	STDMicro		Digital speech generator card, custom vocabularies available, 32 word FIFO buffer allows complete sentences to be loaded in one burst, reducing host processor overhead.	TLK-1	AdvMicroSys	
256-Kbyte non-volatile core memory, equal read and write times, data protect circuitry on board.	CM328	Controlex		Synthesizer Uses complete words instead of phonemes to achieve a natural sound, preprogrammed vocabulary. Comes with phrase demonstration ROM set. ROMs with custom words are also available	CE4510-2	Conway	
512 KB universal memory card. Supports RAM, ROM, EEPROM. Optional battery back-up. All CMOS. -40°C to +85°C operating temp.	LPM-UMC2	WinSystems		<b>Miscellaneous</b>			
512 KB universal memory card supports RAM, ROM, EEPROM. Optional battery for back-up RAM's.	MCM-UMC2	WinSystems		Bar code reader, printer, data buffering.	7415	Sensoray (4901)	
128 Kbyte DRAM, compatible with 8085, Z80, 6809, and 6502 CPUs	6210	Systek		Calendar clock, battery back-up.	MCM-CLK	WinSystems	
128 Kbyte DRAM with controller, 8088 compatible	6128	Systek		Calendar clock using the MM58167A, provides 24 hour clock with BCD format, on-board lithium battery for power-down operation.	MCM-CLK	WinSystems	
256K dynamic RAM with 4 MHz bus operation. Supports Z80 DMA and bi-directional DMA of 16- and 24-bit devices.	STD303	Micro-Link		Clock/Calendar, Industrial I/O, RS-232-C, 8-channel 12-bit analog to digital converter, 8 level interrupt.	STD7520	CAN-TRON	
64K dynamic RAM card compatible with 8080, 8085, and Z80, self-refresh and low power.	RAM64	AdvMicroSys		Clock/Calendar w/Serial SBC (8088).	05827	STDMicro	
<b>Miscellaneous</b>				Clock/calendar with APU (Z80).	05350	STDMicro	
General purpose slave board which uses resolver based input to measure absolute shaft position and provide a binary output corresponding to this shaft position.	BSTD	Astro		Counter/timer, three 16-bit channels. Eight input count source multiplexer, on-card crystal oscillator.	308	Octagon	
<b>Multifunction</b>				Counter/timer, 4-event pulse-width counter and 8 timers. Application software includes PID controller, SCR timing control and multiple N bit counters	LD8040-K	LupiData	
Accessory board; designed for real-time applications; includes AC/DC power-fail protection, real-time clock/calendar, timer, reset, indicator lights and switches.	ZT8882	Ziatech		CRT emulator, Complete VT100 with AVO emulation 80/132 column, 24 row, smooth scroll, non-volatile setup memory, true 19200 speed, on-board Z80, keyboard, serial I/O parts, composite or separate video outputs.	STD100	KSystems	
Battery-backed real-time clock, 6 memory sockets, 48 digital I/O lines	RSD-7758	Robotrol		Display/keypad driver card that features a display port, 16-key keypad interface and eight high current outputs.	850	Octagon	
CPU board. Sockets for 12-bit A/D, 8/16 channel multiplexer, master/slave modes, full Z80 interrupts.	7410	Sensoray (4901)		Encoder interface with 4 digits of UP/DN counter. Supports Quadrature inputs plus index and event inputs. Single-ended or differential inputs, binary or BCD counting.	S851	Contemporary	
EPROM and UART with 10K ROM-based firmware module.	MK77950	Thomson		EPROM programmer for 27256 and 27512 EPROMs. Parallel printer port. ZIF programming socket.	871	Octagon	
power supply, power fail, battery backed, real time clock, 8 parallel inputs, 8 outputs, remote LEDs and thumbwheels, edge or flat mounted LEDs	CDI-Combo	CompDyn		Extender card. DIP switch isolation on signal lines; ground plane shielding.	STD-SX3-A	Intelicom	
Provides listener, talker, controller capabilities on a single card. 16 buffered I/O channels, 48K bytes of RAM, supports high speed DMA.	GPIB-100	RLCEnterprise		Extender card. Includes test points for all STD bus power signals.	901	Octagon	
System controller/diagnostics card.	MK77963-0	Thomson		Hardware/Software Development Support for Z-80-based systems. Complete debugging functions from IBM & compatible PC's. Includes object file download from PC diskettes by RS-232 interface. Optional EPROM programmer available.	DS-Z80	Devtek	
V20 CPU board with 8087 socket, RAM, ROM, RS-232, dual PIO interrupt controller. PC DOS and ROMable C compiler available.	SB8082	MicroSys		Hardware/Software Development Support for 8085-based Systems. Complete debugging functions from IBM & compatible PC's. Includes object file download from PC diskettes by RS-232 interface. Optional EPROM programmer available.	DS-8085	Devtek	
<b>Prototyping Boards</b>							
Board	STI-STD-CK	Solarcom					
Board, Program development peripheral card	871	Octagon					
Buffered development decoded card. Prototype digital and/or discrete circuits. Flexible I/O or memory mapping.	STD-830	Micro-Link					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>STDbus</b>							
<b>Miscellaneous (Cont'd)</b>							
Hardware/Software Development Support for 8086/8088-based systems. Complete debugging functions from IBM & compatible PC's. Includes object file download from PC diskettes by RS-232 interface. Optional EPROM programmer available.	DS-8088	Devtek		Waveform generator processor, up to 2 Kbytes with waveform memory. Generates pulse, word or arbitrary waveforms from software-programmed parameters, software included.	LD8060	LupiData	
High power driver with stepper motor logic, full or half step, outputs may be paralleled for higher power.	ST60	AdvMicroSys		Wire-Wrap card; power and ground busing to every IC, bypass capacitors across each IC, accommodates from 14 to 40 pin ICs.	STD-WW3-A	Intelicom	
Interrupt expander module.	MK77967	Thomson		Quad CTC (Z80).	05352	STDMicro	
Interval timer has two 8253 counter timers, six 16 bit counter, six programmable modes and internal or external time base.	S853	Contemporary		Quadrature encoder input. Input and decoding for one TTL or CMOS-level incremental encoder. Two channels and index. 24-bit counter, 10 MHz max. sample clock rate, 333 kHz max. decode rate, 2 MHz max. count rate, programmable interrupt control.	4324	Tech80	
IRIG-B synchronizable reader/generator event register, propagation delay correction. FIFO bus interface, AGC, auto-polarity, 1 microsecond accuracy, optional oven on-time rate and frequency outputs.	ATTGSTD	KSystems		Quadrature encoding inputs. Inputs and decoding for three TTL or CMOS-level incremental encoders. Two channels and index each axis, 24-bit counters, 10 MHz max. sample clock rate, 333 kHz decoder max. decode rate. Programmable interrupt control, SBX connector. Expandable to four axis with SBX model 4324.	4312	Tech80	
IRIG-B Time Code Reader. Forward/reverse up to 10X speed. FIFO bus interface, AGC.	STDVTTRZ80	KSystems	5	Eight channel relay multiplexer. On-board microprocessor runs BASIC. 1000 volts isolation to bus. Cold junction sensing capability.	MTI-1091	Miller	25
Multisensor A/D interface for thermocouples, voltage, RTDs, thermistors, or current. Software programmable gains, eight channels. Full range sensor linearization using on-board microprocessor and 14-bit A/D.	7408	Sensoray (4901)		Z80/NSC800 Adapter Module: allows Z80 In-circuit Emulator (ICE) to operate Intelicom's CMOS-CPU processor card.	CMOS-Z80/800	Intelicom	
Parallel video display (Z80).	MK78199	Thomson		128 channel FET multiplexer. On-board microprocessor runs BASIC. High-speed operation with 1000 volts isolation to bus.	MTI-1092	Miller	
Processor with programmable pre/postamble, checksum, re-transmit, and character filtering. Also works as printer spooler and transmit receive buffer.	7413	Sensoray (4901)		8085/NSC800 Adapter module; allows 8085 In-circuit Emulators (ICE) to operate an NSC800 processor card.	CMOS-85/800	Intelicom	
Program development card has EPROM programmer, 32K battery backed RAM, parallel printer port. ZIF programming socket.	870	Octagon	10	<b>TM990</b>			
Programmable cross hair generator card, accepts composite video input then superimposes up to eight programmable indicator lines on the output video for pattern recognition or image processing applications.	PCHG-8	AdvMicroSys		<b>Controllers</b>			
Provides controlled outputs from up to 16 opto-isolated, PCB-mounted DC relays (opto 22 type). Suppression diodes may be mounted to provide selectable load connection. LED status indicators provided. Strappable addressing.	4303	Tech80		Floppy disk drive.	TM990/303B	TI	30
	4325	Tech80		IEEE-488.	TM990/314	TI	
Provides 32 independent latched outputs, each capable of directly driving an LED. Useful for driving independent LED status indicators on operators' panels of machine controls, and may also be used to drive segmented character LED displays.	8303	Tech80		<b>I/O</b>			
Real-time clock	RTX	Datricon	15	Analog output, 4 channel, 12-bit D/A resolution.	RT1242	AD	
Serial video display (Z80).	MK78198	Thomson		Analog output, 8 channel, 12-bit D/A resolution.	RT11243	AD	
Shielded extender card has all lines labeled and breakable. Fuses on all power lines. Test points.	DSB2409	Davidge		Analog, 32 single-ended, 16 differential inputs, 12-bit resolution.	RT11240	AD	
STD bus to IEEE-488 interface (GPIB). Complete talker/listener capability. Full function RS-232 serial ports	GPIB-961P	NationalInst		Combination Analog, 32 single ended, 16 differential inputs, two-channel output, 12 bit D/A resolution.	RT11241	AD	35
Terminator card. Active termination of all bus signals except PBRESET. Permits sink/source of 10 mA per line.	STD858	Micro-Link		High power ac and dc interface.	TM990/309	TI	
Video cross-hair generator/digitizer, superimposes up to four adjustable indicator lines on the output video.	CHG-4	AdvMicroSys	20	IEEE (ISBX) interface.	TM990/959	TI	
				48 TTL compatible, input/output lines with three programmable timers, six interrupts.	TM990/310	TI	
				48 TTL lines, 24 mA sink current, on-board voltage regulator.	TM990/311	TI	
				<b>Memories</b>			
				Bubble memory card, 128 Kbyte 4 FBM43DA devices, compatible with the TM990 board.	MBC404M3T	FujitsuA	40
				EPROM programmer.	TM990/304	TI	
				RAM/EPROM/CMOSRAM, sockets for up to 128 Kbyte EPROM, up to 32 Kbyte static RAM and CMOS RAM, battery back-up.	TM990/202	TI	
				RAM/EPROM, up to 8 Kbytes EPROM, up to 32 Kbytes static RAM.	TM990/201	TI	
				256 Kbyte DRAM maximum with error detection, up to 16 Kbytes EPROM.	TM990/203A	TI	

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>TM990</b>				<b>Low-level analog I/O system, up to 64 single-ended or 32 differential inputs.</b>			
				DT1715      DataTrans			
<b>(Cont'd)</b>				<b>Memories</b>			
<b>Miscellaneous</b>				Unibus compatible memory with 1M byte capacity. Hex width board, parity memory, on-board status indicators, compatible with DEC PDP-11 computers containing the Unibus, or EUB.			
Communication expansion, provides four RS232/RS422.	TM990/307	TI		DR214      Dataram			
Pulse timer/event counter.	TM990/317	TI		DR244      Dataram			
X.25/HDLC Communication, permits implementation of distributed industrial processing network.	TM990/308	TI		64K DRAM memory, 1MB capacity, battery back-up, parity, CSR, lifetime warranty.	UNIRAM	Clearpoint	
<b>UNIBUS</b>				<b>Multifunction</b>			
<b>Communications</b>				MIL-STD-1553 bus controller, bus monitor, and remote terminal unit. Interfaces the Unibus system to the MIL-STD-1553 data bus. $\pm 12$ VDC operation.			
Ethernet/IEEE 802.3 Front-End Processor memory.	NP100	Micom Int		BUS65505      ILC-DDC			25
Intelligent Ethernet controller for Unibus systems. 80186 CPU, up to 512 KB RAM, supports TCP/IP Internet protocols.	EXOS204	Excelan	5	BUS65506      ILC-DDC			
Intelligent Ethernet/IEEE 802.3 controller for Unibus systems. 80286 CPU, 512K RAM, 82586 LAN coprocessor, supports TCP/IP Internet protocols.	EXOS304	Excelan		MSCP Compatible, SCSI host adapter for support of SCSI compatible hard disks and peripheral subsystems. TS-11 emulation of start/stop SCSI tape devices also available.	B58M00	USDesign	
Link level controller, Ethernet/IEEE 802.3	NI1010A	Micom Int		MSCP Compatible, SCSI host adaptor for support of magnetic, SCSI peripherals. The adapter is firmware optimized to include support of SCSI optical disk system. "OPUS" software utility available for optical archival applications under RSX and VMS operating systems.	B58L00	USDesign	
<b>Controllers</b>				Plus firmware support for VOS (Virtual Optical Storage) for file structured optical applications full hard disk emulation for optical disks is provided along with "OMAP" optical utilities.	B58V00	USDesign	10
Ethernet intelligent controller with 80186 microprocessor, DMA capability, TCP/IP transport protocols.	EXOS204	Excelan		<b>Miscellaneous</b>			
Intelligent Ethernet/IEEE 802.3 controller for Unibus systems. 80286 CPU, 512K RAM, 82586 LAN coprocessor, supports TCP/IP Internet protocols.	EXOS304	Excelan		Bus grant cards provide interrupt and DMA continuity for empty slots in backplane. Dual Quad and Knucklebuster sizes.			
Intelligent networking, one or two Mb/s DMA transfer rate on fiber or coax in SDLC or token pass. Up to 99 other stations on LAN.	LU5	Computrol		160      Codar			30
Hex height MSCP 1 MB Cached ESDI Winchester disk controller. WOMBAT comprehensive on-board interactive formatting and diagnostic firmware, programmable look-ahead, supports up to four physical drives, drive shadowing, seek optimization and overlap, command queueing, ECC, dynamic bad block replacement, on-board bootstrap.	WUESD WUSMD	Webster Webster		IRIG-B synchronizable reader/generator, event register, propagation delay correction. FIFO bus interface, AGC, Auto-polarity, dual size module with 1 $\mu$ s accuracy and on-time rate and frequency outputs.	AITG-U	KSystems	
<b>I/O</b>				<b>VAX</b>			
Analog input system capable up to 64 single-ended or 32 differential inputs.	DT1712	DataTrans		<b>I/O</b>			
Analog output systems with up to 8 D/A converter outputs and up to 8 digital outputs, 12-bit resolution.	DT1716	DataTrans		IEEE-488 Interface and handler rainbow GPIB-PC.			
Analog, 4 differential input channels, 100 kHz throughput, 16 bit resolution, 4 channels of D/A output, on board pacer clock.	DT1777	DataTrans		18020101      NationalInst			
Analog, 4 single-ended channels, 100-kHz throughput, 12-bit resolution, 4 channels of D/A, 125 kHz throughput, on-board pacer clock.	DT1778	DataTrans		<b>Memories</b>			
Analog, 8 differential input channels, programmable gain, 12-bit resolution, 4 channels of D/A, on board pacer clock, 125 kHz throughput.	DT1771	DataTrans		Add-in memory available in 16-64MB capacities, all utilizing one double-wide slot. Uses surface mount 1 MB DRAMs, supports single-bit error correction and double-bit error detection. 16MB capacity uses 256K DRAMs, 64MB capacity uses 1MB DRAMs. For DEC VAX 85XX, 87XX, and 88XX.			
High level analog with 16 single-ended or 8 differential input channels, 12 bit D/A converter, two channel 12 bit D/A converters, up to 64 single-ended or 32 differential inputs.	DT1711	DataTrans		VXR8800      Clearpoint			15
IEEE-488 Interface and handler GPIB 11-1 programmed I/O.	17804101	NationalInst		Micro-VAX compatible memory with 2/4M byte capacity. On-board parity generation and checking.	DR222	Dataram	
IEEE-488 Interface and handler GPIB 11-2 DMA I/O.	17904001	NationalInst	20	Micro-VAX compatible memory with 8M bytes of capacity. On-board parity generation and checking.	DR224	Dataram	35
				VAX compatible memory with 1/4 Mbyte capacity and ECC. 39-bit data word with 32-Bits of data and 7-Bits of ECC.	DR278	Dataram	
				VAX compatible memory with 1M byte capacity and ECC. VAX 11/750, 11/730, and 11/725 compatible.	DR275	Dataram	

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VAX</b>							
<b>Memories (Cont'd)</b>							
VAX 8600/8650 compatible memory with 4/16M byte capacity. Hex size board, ECC memory, 39-bit data word with 32-bits of data and 7-bits of ECC.	DR286	Dataram	5	VME-to-VME link. High-speed parallel DMA controller network with multidrop capability. One master controller. Supports up to 16 slaves. Supports 8, 16, or 32-bit data transfers over long cable (up to 2000 ft.) utilizing differential long line drivers and receivers.	VMIVME-VMENet VME-Microsys		
One Mbyte add-in memory board with error correcting for the VAX 11/730 and 11/750.	CVM50/30	Cyberchron		4 channel intelligent serial communications controller, RS-232 personality module, 0-1 M bp/s baud rate.	451-48201F	Bicc-Vero	
1MB DRAM memory board. 4 and 16MB capacity, battery back-up, EDC, lifetime warranty.	VXR8600	Clearpoint		<b>Controllers</b>			
4MB DRAM with ECC for VAX 780/785.	CI-VAX4	Chrislin		Advanced graphics controller, 63484 ACRTC, 1MB display RAM, 1024x800x4 display, 16/64K colors, zoom, scroll, window support, RGB and sync outputs, s/w support under PDOS, UNIX, single board.	AGC2	Force	
16 MB memory card for DEC MicroVAX 2000 and VAXstation 2000. 100% hardware/software compatible; utilizes surface mount megabit DRAM technology.	MV2000	Clearpoint		Advanced system control unit.	ASCU-1	Force	25
32 MB memory card for Sun Microsystems 3/200 series and 4/200 series. Has 32, 16, and 8 MB capacities, EDC and on-board diagnostic hotline using communications port.	SNX2RAM	Clearpoint		BitBus controller module. Single-high module which provides full control of BitBus network from any VME bus system.	XVME402	Xycom	
64K DRAM memory, 1MB capacity, battery back-up, parity, CSR, lifetime warranty.	VXR750	Clearpoint		Character overlay board for AGC-1 64KB character RAM, 32K byte character generator, 4 serial I/O parts.	AGC1X	Force	
256K DRAM memory. 1, 2, 4, 8 MB capacity, battery backup, EDC, lifetime warranty.	VXR780	Clearpoint		Color graphics controller. RS-343 compatible, 256K video RAM, 1024x1024 pixels and four color planes.	VME643	Micro-Link	
256K DRAM Memory board allows 16MB addressing. 2-8MB capacity, parity, lifetime warranty.	MV2RAM	Clearpoint		Color graphics controller with 1024 x 1024 pixel resolution within 16 colors. Firmware control of industry standard graphics functions, including windowing, blanking, zoom, pseudo colors, inverse video and plot functions.	PME-GDC-1	Plessey	
1 Mbyte DRAM, ECC, runs with VAX 725, 730, and 750.	CI-V53	Chrislin		Controller, high performance asynchronous I/O controller, single dual height VME board with full 32 bit data path, supports 16 full duplex ports at 9600 baud or 8 ports at 19.2 K baud. Provides full UNIX TTY sysbsystem emulation directly on the board, reducing amount of character I/O processing the host CPU must perform, and provides flexible terminal interface to UNIX drivers are available.	780	Xylogics	30
256K ZIP DRAM memory board, to 128 MB capacity range. Memory controller separate from memory arrays, EDC.	VBIRAM	Clearpoint	Controller, high performance disk controller ESDI disk interface supports data rates greater than 1.2MB/sec., DMA up to 10MB/sec., full 32 bit supports, FIFO buffer, automatic ECC, software programmable. Capable of controlling four ESDI drives. UNIX drivers are available.	714	Xylogics		
<b>VMEbus Communications</b>				Controller, high performance disk controller, SMD disk interface supports data rates up to 2.4MB/sec., DMA up to 10MB/sec., full 32 bit support, FIFO buffer, automatic ECC, software programmable. UNIX drivers are available.	752	Xylogics	15
Ethernet/IEEE 802.3 Front-End Processor.	NP700	Micom Int	Controller, high performance tape controller, PERTEC formatted interface, supports tape speeds up to 200 ips, densities to 6250 bpi. DMA rate up to 10MB/sec., full 32 bit support, supports either streaming or start/stop tape drives. UNIX drivers are available.	772	Xylogics		
Ethernet node controller. High-speed Ethernet (IEEE 802.3) node controller specifically for cost-sensitive applications. Intelligent Ethernet controller chip (LANCE) and a 256 KB dual ported data buffer, provides high-speed 32-bit bus slave data access. Accomodates direct connection to both Ethernet and Cheapernet transceivers.	V/Ethernet 3207	Interphase	Controls up to two 5 1/4" Winchester hard disks (ST-506 compatible), controls up to four 5 1/4" floppy disks, SA400 compatible. Double high VME module.	MVME-321	Motorola		
Ethernet node processor with MC68000 running at 10 MHz, 128KB of no-wait state dual-port DRAM with parity.	IV1620	Ironics	CRT color controller with keyboard and printer ports.	IV1653	Ironics	35	
Intelligent Ethernet controller for VMEbus systems. 80186 CPU, up to 512 KB RAM, supports TCP/IP Internet protocols.	EXOS202	Excelan	Direct ST506/SA460 5 1/4" Winchester floppy controller.	WFC-1	Force		
Intelligent ethernet interface, 68010 CPU, 512KB SRAM, master interface, optional TCP/IP firmware.	ILANC1	Force	Disk controller. Supports 5 1/4" and 8" Winchester and floppy drives. Up to four drives per board. CRC and ECC supported, two connector styles available.	PG3101	MicroInds		
LAN controller. Frees VMEbus hosts from protocol processing burden. Interfaces with VMEbus and hosts in the Ethernet System. Features 10 MHz MC68000 or MC68010 MPU, 128K or 512K dynamic RAM with parity.	MVME330-1	Motorola					
LAN controller with MC68010.	MVME330-2	Motorola					
Manufacturing Automation Protocol (MAP) interface. A two board set comprising a controller board and a modem board. For operation on MAP 2.1 channel group 3'/4"/P/Q.	MVME372SET-1 Motorola MVME372SET-2 Motorola MVME372SET-3 Motorola						

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>							
<b>Controllers (Cont'd)</b>							
Disk Module, includes 48120 controller, 20 Mbyte Winchester, microfloppy drive, all connections via PI connector.	48680D	Bicc-Vero		Intelligent SCSI controller, 68010 CPU, 128/512KB dual-port SRAM, DMA for local memory-disk transfers, 4-floppy disk controller.	ISCSI1	Force	25
ESDI Disk and Tape Cartridge controller. Supports ESDI disk or tape drive with up to 15 MHz serial data rate. Soft or hard sectored disks. Fast DMA, non-interleaved transfers, overlapped seeks and command chaining.	MCT6700	MiniCompTech		Intelligent 68000 based controller which can be used to interface large amounts of analog and digital I/O channels to the VMEbus using expansion modules.	MPV960	Burr-Brown	
ESDI disk controller. Has the features of the V/ESDI 3201 in a four drive controller with the BUSpacket interface and a 128K caching buffer. VMEbus DMA data rates over 30 MB/s and multitask caching. Optional SCSI port available for control of other disk drives, tape backup, and optical disks.	V/ESDI 4201	Interphase		Low-cost serial controller with eight independent, full-duplex RS-232-C channels. High system throughput attained by providing four separate interrupts per channel. Software programmable baud rates from 50 to 19.2K baud.	V/SIO 3208	Interphase	
Ethernet intelligent controller with 80186 microprocessor, DMA capability, TCP/IP transport protocols.	EXOS-202	Excelan		Mass storage device controller with on-board FIFO. Simultaneously supports 2 Winchester (ST506) and 4 floppies (mixable 3-1/2, 5-1/4, and 8 inch) with one optional streaming tape.	VMSC	PEP-Modular	
Ethernet Node processor/LAN controller. Interface for 10-Mbps Ethernet implementation.	MVME330	Motorola		MIL-1553B dual-redundant data bus interface. Available in full MIL-SPEC or ruggedized.	PMV1553B	PlesseyMicro	
Floppy disk controller. Word DMA or programmed byte data transfer over VMEbus.	MK75803	Thomson		Multifunction peripheral controller. Combines Centronics printer port, an electrostatic plotter port, and a SCSI host adapter all on one VME bus card.	V/MIX 3210	Interphase	30
Floppy disk, programmable to control up to four single- or double-sided 5-1/4 or 8-inch disk drives of single or double capacity.	MK7803	Thomson		PAMUX controller module. A single height VME bus interface for the OPTO-22line of PAMUX-4 high density expandable power I/O systems.	XVME202	Xycom	5
Floppy disk/UIPC interface controls up to four 8-inch or 5-1/4-inch floppy disk drives, supports 4-channel DMAC and provides RS-232C serial function.	MVME315	Motorola		Power-fail monitor and system control. Complete system control and utility functions including single-level arbiter and power-fail monitor.	IV1073	Ironics	
Floppy/hard disk, DMA intelligent using Signetics 68454, supports 4 drives, up to 2 Winchester and 3 floppy disks	48120F	Bicc-Vero		QIC 2 tape controller.	VME-QIC2	IntSolutions	
GPIO controller with DMA.	MVME300	Motorola		QIC-02 1/2" AND 1/4" Streaming Tape Cartridge controller. Supports Winchester disk based systems in capacities of 60 up to 200 MGB, with high speed DMA and up to 128 lbyte transfers with on command.	MCT6010	MiniCompTech	
GPIO interface, DMA and dual-channel optional	48220A	Bicc-Vero		SCSI host adapter. Full SCSI interface with DMA. 512K dual-port dynamic RAM.	VME620	Micro-Link	35
GPIO, polled or interrupt driven, 50-kHz transfers	42-209	Anasco		SCSI interface	48230H	Bicc-Vero	
Graphics controller, 63484 ACRTC, 2MB dual-ported display RAM, 1280x1024x8 256/16M colors, RGB and sync outputs, zoom, scroll, window support, s/w under PDOS, UNLX.	AGC1	Force		SCSI interface with sustained data transfer rates up to 2.5 Mbytes/s, full32-bit addressing and data.	PME SCSI-1	PlesseyMicro	
Graphics display processor board with 7220, 512 Kbyte display RAM, up to 40 MHz pixel rate.	IV1651	Ironics		SCSI peripheral controller with on-board 68000 and RAM.	VCC-1	CharlesRiver	
Hard disk controller interface. DMA can transfer up to 64-Kbyte data blocks.	MK75802	Thomson		SMD Disk Controller/Formatter, supports up to two SMD disk drives, programmable 8, 16 or 32 bit wide data transfers.	IV3275	Ironics	
Hardcopy peripheral device controller for any Versatec-compatible or Centronics-compatible plotter/printer including laser printers and color copies. 60 (double-high) form factor.	10088	IKON		SMDE Disk Controller, For SMD disk drives with serial data rate up to 24 MHz, 3 MB/Sec. High speed DMA device and on-board 48-bit ECC, static RAM cache of 16 up to 128 KB.	MCT6600	MiniCompTech	40
High resolution pixel memory with screen refresh, flicker-free display	MVME390	Motorola		Supports 2 SMD or SMD-E drives, M68000 Virtual Buffer architecture, Disk data rates to 24 Mb/s, Intelligent Caching plus Zero Latency Operation, 32-bit DMA with throttle.	V/SMD3200	Interphase	
High-resolution color graphics module with 38 high-level commands, up to 4096 by 4096 pixels, includes interface to VCCD camera module.	VGPM	PEP-Modular		Supports 4 SMD or SMD-E drives, M68000 Virtual Buffer architecture, BUSpacket Interface—DMA rates over 30 MB/s, Intelligent Caching with Zero Latency Operation, 128K Cache buffer, Software Compatible to V/SMD 3200 and V/ESDI 3201.	VSMD4200	Interphase	
High-speed GPIO controller, on-board DMA, 500-kHz transfers	42-208	Anasco		System controller. Handles bus arbitration, power fail, cycle length monitoring, and system reset functions. Provides 16 MHz system clock and 4 MHzVMS clock.	PG2900	MicroInds	
Includes IEEE-488, programmable user/interprocessor interrupts.	ASCU-2	Force		System controller for use with MC68010-based MPU to provide system-level functions, on-board system clock and serial bus clock.	MVME025	Motorola	20
Intelligent monochrome controller, 512x512 resolution, on-board 6809 processor, provided with Firmware.	XVME310	Xycom					
Intelligent networking, one or two Mb/s DMA transfer rate or token pss. Up to 100 stations on LAN.	LV-6	Computrol					
Intelligent peripheral controller.	MVME310	Motorola					
Intelligent SCSI controller/host adapter.	XVME405	Xycom					

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\* Typical Value

° Macrocell

Bold face indicates additional data is provided on the page noted.



## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>							
<b>Controllers (Cont'd)</b>							
System controller module: parallel and round robin arbiters, system clock generator, system reset generator power fail monitor, centronics parallel printer port, SCSI bus interface with DMA data transfer, two full duplex ASYNC serial ports using 68681.	IV3273	Ironics		Analog input board, 16-channel 12-bit ADC.	IV1641	Ironics	
System controller module. Performs all of the VME system controller functions.	SCM	DUAL		Analog input, 8 channels with 32 Kbytes of on board RAM, 12-bit resolution	IV1648	Ironics	
Tape controller for 1/2 inch PERTEC interface. Tri-mode compatibility (800/1600/6250 bpi). Controls up to eight 9-track 1/2 inch drives.	IV3276	Ironics		Buffered voltage output (0–10 V or plus or minus 10 V 5 mA). 12-bit D/A per channel, 1 $\mu$ sec settling time, double buffered inputs. Supports built-in test loop-back for fault detection and isolation when coupled with VMIC's A/D converter board.	VMIVME4100	VME-Microsys	25
VME based intelligent SCSI controller with 16-bit DMA data path. MC68000 at 10 MHz with no-wait states, 64KB of EPROM.	VSCSI	DUAL		D/A converter. Eight channels, 12-bit resolution.	IV1640	Ironics	
VMEbus data communications processor, designed to provide serial interfaces with a wide range of standard and custom communications protocols, on-board 80186 processor, operation in asynchronous, bisynchronous, SDLC, HDLC, X.25, and SNA communications protocols.	DCP8820	Systech		Digital signal processor and A/D converter, on board TMS320 signal processor, 12-bit resolution	IV1646	Ironics	
Winchester/Floppy disk. Controls up to two 5–1/4-inch Winchester disk drives and up to four floppy disk drives, on-board DMA.	MVME320	Motorola		High speed buffered 8-channel A/D	MPV952	Burr-Brown	
Winchester floppy disk/floppy tape controller supports up to two Winchester controllers via a SASI/SCSI interface	MVME319	Motorola		Isolated for channel D/A board, 30 $\mu$ s settling time, 12-bit resolution. Choice of voltage outputs: 0 to 5 Vdc, 0 to 10 Vdc, plus or minus 2.5 Vdc, plus or minus 5 Vdc, and plus or minus 10 Vdc.	DVME624V2 DVME626V2	Datel	
Winchester (SCSI) and floppy controller	VDIO	PEP-Modular		Isolated four channel D/A board, 30 $\mu$ s settlin time, 12-Bit resolution. Choice of voltage outputs: 0 to 5 VDC, 0 to 10 VDC, plus or minus 2.5 VDC, plus or minus 5 VDC, and plus or minus 10 VDC.	DVME624VI	Datel	30
Single-axis stepper motor controller with full or half-step operation. Compatible with 3-, 4-, or 5-phase stepper motors.	MS-SSC	Matrix		Isolated four channel D/A board, 30 $\mu$ s settling time, 12-Bit resoluion with + 1/2 LSB differential nonlinearity. 4 to 20 mA industrial current loop output.	DVME624C1	Datel	
Dual-axis stepper motor controller with full or half-step operation. Compatible with 3-, 4-, or 5-phase stepper motors.	MS-DSC	Matrix		Isolated four channel D/A board, 6 us settling time, 12-bit resolution, 4 oto 20 mA current loop industrial output.	DVME624C2	Datel	
Four-channel DMA system controller with real-time clock.	VDMA	PEP-Modular		VME to SCSI intelligent host adaptor connects to a VME bus host processor to the SCSI bus.	ADP33	NCR	
Eight-channel asynchronous serial communications module with RS-232, RS-422.	XVME428	Xycom		Quad channel resolver-to-digital converter board. Pin programmable resolution (10, 12, 14, or 16-bit). Accuracy to plus or minus 2.3 ARC minutes. Reference frequency to 6 kHz, tracking rates up to 800 rps (45,000 rpm). 16-bit software programmable pitch converter per channel.	VMIVME4941	VME-Microsys	35
Nine track 1/2-inch tape controller, handles Pertec type interface. PE and GCR.	VMETC50	IntSolutions		Two 16-bit digital-to-synchro or digital-to-resolver converters.	5410C	Transmag	
Nine-Track tape controller optimized for use in multiuser systems.	V9TRK	DUAL		Four channel A/D board with high isolation for thermocouples and low-level inputs. On-board CPU for temperature calaculations, CJC, on-board linearization for J, K, T, S, B, E, and R type thermocouples, 13-Bit resolution.	DVME602T	Datel	
9-Track controller. For all cartridge and 9-track tape units with a PERTEC interface, supports tape data rate up to 1.25 MB/s, equal to 200 ips at 6250 BPI.	MCT6020	MiniCompTech		Twelve-bit analog-to-digital converter module with software programmable gain. Supports VMIVME-3200 series multiplexer modules.	VMIVME-3110	VME-Microsys	
9-Track Tape controller. For all cartridge and 9-track tape units with a PERTEC interface. D32 version of the MCT6020, with added features to allow disk controllers, such as MCT6600, to perform backup without using host memory or resources.	MCT6021	MiniCompTech		8 channel current source digital to analog, 12-bit resolution	IV1644	Ironics	40
802.3/802.3 LAN controller.	VNC-1	CharlesRiver		8-channel, 12-bit Multiplying DAC, with built-in-test, 2 or 4 quadrant multiplier option. Requires VMIVME-3100 for built-in-test.	VMIVME4105	VME-Microsys	
<b>Converters</b>				16 channel digital to analog, multiple address modifier capability	IV1643	Ironics	
A/D and D/A, features software-controlled analog-input signal selection and conditioning as well as 32 banks of look-up tables.	DIGIMAX	Datacube		16-bit A/D converter board. 37 $\mu$ sec settling/conversion time. Autocalibration option provides 16-bit accuracy, 16 channel single-ended or 8 channel differential front panel inputs. On-board built-in test logic for fault detection.	VMIVME3116	VME-Microsys	
A/D conversion module, 14 to 16 bit	GMSV04	GenMicro		16-channel A/D converter, 12-bit resolution, programmable sample rates, 16 single-ended or 8 differential inputs, 16 TTL compatible lines for parallel I/O and/or interrupt inputs	16A/D-A	Alcyon	
A/D converter. Eight channels, 20 $\mu$ second throughput, 16-bit resolution.	IV1639	Ironics		32-channel analog to digital, 2-channel digital to analog, 32 single-ended or 16 differential inputs, 12-bit resolution, 7-level interrupt selection	IV1642	Ironics	
A quad channel synchro/resolver-to-digital converter input board which utilizes one synchro/resolver-to-digital module and a quad multiplexer to convert synchro/resolver data to a 14-bit digital word.	VMIVME4911	VME-Microsys					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line	
<b>VMEbus</b>								
<b>Converters (Cont'd)</b>								
12-Bit 8 channel D/A board. 6 μ settling time, same voltage outputs available as DVME-628V plus 4 to 20 mA current loop available.	DVME628C	Datel	5	Graphics interface module. High resoluition for Bit-Mapped graphics (1024x1024 pixels). Optional GKS support for FORTRAN 77 and C applications in VERSAdos and SYSTEM V/68 operating system environments.	MVME390A	Motorola	25	
12-Bit 8 channel D/A board, 6 μs settling time, five voltage outputs available: 0 to 5Vdc, 0 to 10Vdc, plus or minus 2.5Vdc, 5Vdc, or 10Vdc.	DVME628V	Datel		Linear signal processing module, up to 144 MOPS.	VFIR	Datacube		
16-Bit, 6 channel D/A board. 15 μs settling time, plus or minus 10V dc output. Three input coding types: bipolar 2's complement, bipolar offset binary, and unipolar straight binary. On-board DC-to-DC converter supplies plus or minus 15V dc for internal logic circuits.	DVME626V1	Datel		Mixer, digital crosspoint switch for graphics.	MAX-MUX	Datacube		
16-channel analog to digital, 7-level priority interrupt selection, 12-bit resolution	IV1645	Ironics		Programmable histogram and feature list extraction module, triggers off of 64K unique events, counts up to 1 million occurences of these events.	FEATUREMAX	Datacube	30	
32 single-ended/16 differential A/D channels. Four levels of resolution; 12-bit 20 μs, 12-bit 4μs, 14-bit 35 μs, and 16-bit 400 ms. With eight stage programmable gain amplifier.	DVME611	Datel		Real-time non-linear pixel processing provides up to 129 million 8-bit comparisons per second.	SNAP	Datacube		
32 single-ended/16 differential A/D channels and two D/A channels available. Four levels of resolution; 12-bit/20 μs, 14-bit/35 μs, and 16-bit/400 ms. Eight stage programmable gain amplifier.	DVME612	Datel	RGB output, 512x1024x8 memory, scrolling, icons	RTI681	AD			
			Transformation, sub-pixel multi-rate sampler, first order wrap.	INTERPOLATOR	Datacube			
			Transposer, real-time 90 degree image rotation.	MAX XFS	Datacube			
				Video input and video output board. Accepts up to 4 camera and VCR inputs. 512x512 resolution. Features include programmable gain, offset, and look up tables. Compatible with the DS-401V digital storage unit and pX-401V pipeline pixel processor.	AS401V	Recognition	10	
				Video memory board. Accepts a 512x512 array of 8 bit image data and stores it as a 512x512x9 bit image. The 9th bit is used for extra features such as graphics overlay, pixel protection and conditional processing control. Scroll and pan is available on a per pixel basis. System is available memory mapped or register accessed from VMEbus and one with one or four fram stores per board. The DS-401V is compatible with the AS-401V I/O board and the PX-401V pipeline pixel processor.	DS401V	Recognition		
				Video pixeo processor board. Operates on 16 bit data at 10.08 MHZ. Enables real time operations such as frame integration and summation, background subtractions, convolutions and filtering. The processor can be programmed to perform 2 different operations in a single pass through the image data. Processor cascading is possible for higher performance systems. The PX-401V is compatible with the AS-401V I/O board and the DS-401V digital storage unit.	PX401V	Recognition		
				Single board real-time image processor with 512x512x8 resolution. Holds four images, split-scan mode, drive software.	Series 100	Imaging		35
				640x480 color display processor	VG640	Matrox		
				<b>I/O</b>				
				A analog input expansion multiplexer, 32 single-ended/16 differential inputs, expandable to 256 differential.	41-213	Anasco	15	
				A/D converter, analog input with 32 single-ended or 16 differential inputsin a single high VMEbus form factor, conversion rates up to 50 kHz, software selectable gains from 1 to 100.	XVME500	Xycom		
				AC input, monitors status of up to eight 120/240 Vac sources, opto-isolated.	MVME610	Motorola		20
				AC output module, 16-channel optically coupled AC output.	VMIVME-2010	VME-Microsys		
				AC output (zero crossover). Enables switching eight 120/240 Vac outputs, opto-isolated.	MVME615 MVME616	Motorola Motorola		
				Analog and digital I/O system with 16 digital I/O lines. A/D has 16-bit resoluition, D/A has 12-Bit resolution.	DT1401	DataTrans		

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>							
<b>I/O</b>							
<b>(Cont'd)</b>							
Analog and digital system on double-height board with 16 digital I/O line. 16-bit resolution A/D, 12-bit resolution D/A, support for seven-level interrupt.	DT1407	DataTrans		Combination A/D, D/A. 32 single-ended/16 differential inputs, 12 or 14-bit resolution, two 12-bit outputs.	41-212	Anasco	
Analog I/O, 32-input and 4 output, 50 kHz input conversion rate. DMA transfers, 16K or 64K of dual-port RAM, 12-bit resolution, programmable gains up to 500 on each channel.	452-48650E	Bicc-Vero		Communications module, 6 serial ports with DMA controller	MVME333	Motorola	25
Analog input board with digital I/O option. 32 single-ended/16 differential channels. Software selectable gains.	MPV907	Burr-Brown		Communications module, 6-channel serial transceiver for 6 RS-232C or RS-422C	MVME705	Motorola	
Analog input board with digital I/O option. 64 single-ended/32 differential channels. Software selected gains.	MPV906	Burr-Brown		DC input module, eight input channels for 10 to 60 Vdc signal monitoring, 2500 V isolation.	MVME620	Motorola	
Analog input/digital signal processor, 4 channels of analog input with simultaneous sampling, selectable input ranges, 12-bit resolution, optical isolation, TMS320 DSP with 200-ns instruction cycle, dual-port 8Kx16 data memory, 4Kx16 program memory.	MPV960	Burr-Brown		DC output module, eight 10 to 60 Vdc output pairs, 2500 V isolation.	MVME625	Motorola	
Analog input module with 64 single-ended or 32 differential analog inputs, programmable gains of 1, 2, 4, and 8.	XVME560	Xycom	5	Digital, high-voltage digital I/O module, 32-bit I/O. Built-in test logic includes on-line and off-line test features.	VMIVME-2532	VME-Microsys	
Analog input/output module with 32 single-ended or 16 differential inputs and four analog outputs.	XVME540	Xycom		Digital I/O module, 64-bit digital TTL megamodule with built in test and programmable port direction control, options include positive true or negative true I/O, open collector outputs.	VMIVME-2510	VME-Microsys	30
Analog input, 8 single-ended input channels and 8 additional input channels, single-ended or differential, 12-bit resolution, 3 $\mu$ s maximum throughput, selectable input ranges	MPV950D	Burr-Brown		Digital I/O, 48 lines, solid-state compatible.	41-214	Anasco	
Analog input, 16 differential 32 single-ended, 12-bit resolution, resistor programmable gain.	MPV901	Burr-Brown		Digital input module, 16-channel AC or DC high-voltage, optically coupled input.	VMIVME-1000	VME-Microsys	
analog input, 16 single-ended input channels, 12 bit resolution, 3 $\mu$ s maximum throughput, selectable input ranges	MPV950S	Burr-Brown	10		VMIVME-1001	VME-Microsys	
Analog input, 32 single-ended/16 differential, 12 or 14-bit resolution, up to 50K samples/s throughput.	41-210	Anasco		Digital input module, 32-bit high-voltage digital input with change-of-state interrupts, current sinking and voltage sourcing, input signal conditioning options.	VMIVME-1180	VME-Microsys	
Analog output, eight channels, 12-bit resolution.	41-211	Anasco		Digital input module, 32-bit optically coupled with change-of-state interrupts, voltage sourcing and current sinking input signal conditioning options.	VMIVME-1160	VME-Microsys	35
Analog output module with eight 12-bit output channels, outputs can be either voltage or current.	XVME530	Xycom		Digital input module 32-bit TTL input with change-of-state interrupt.	VMIVME-1101	VME-Microsys	
Analog output module with four 12-bit output channels, selectable voltage ranges of -10V to +10V in four ranges.	XVME505	Xycom		Digital input module, 64-bit high voltage digital input megamodule with built in test and front panel fail LED, supports up to 32-bit transfers, voltage sourcing and current sinking input signal conditioning options available.	VMIVME-1110	VME-Microsys	
Analog output system with up to 8 D/A converters on double height board. On-board isolated dc/dc converter for noise reduction.	DT1406	DataTrans	15	Digital input module, 64-bit optically coupled, input voltage sourcing and current sinking signal conditioning options.	VMIVME-1150	VME-Microsys	
Analog output, 8 channels, 12-bit resolution, current source outputs with selectable range for each individual channel	MPV905	Burr-Brown		Digital output module, 32-bit optically isolated digital output, supports up to 16-bit data transfers.	VMIVME-2170	VME-Microsys	
Analog output, 16 channels, 12-bit resolution, unipolar or bipolar output	MPV904	Burr-Brown		Digital output module, 64-bit high voltage, built in test and front panel fail LED, supports up to 32-bit data transfers, open collector outputs with built in suppressor diodes.	VMIVME-2120	VME-Microsys	40
Analog subsystem, four analog-output channels.	RTI602	AD		Digital output module, 64-bit high voltage, current sinking, digital output with built in test and front panel fail LED, high surge current protection.	VMIVME-2130	VME-Microsys	
Analog subsystem, 32 single-ended, 16 differential analog-input channels, 12-bit resolution.	RTI600	AD			VMIVME-2131	VME-Microsys	
Analog, 16 differential 32 single-ended inputs, 2-channel analog output, 12-bit resolution, resistor programmable gain.	MPV901A	Burr-Brown	20	Digital output module, 64-bit telecommunications relay driver for negative high voltage applications.	VMIVME-2132	VME-Microsys	
	MPV901P	Burr-Brown		Digital, programmable I/O module, 48-bits of parallel I/O with handshake and two 24-bit timers. Interrupt capabilities include timer interrupts and I/O port interrupts.	VMIVME-2511	VME-Microsys	
Analog, 16-channel single-ended 12-bit analog to digital converter with built in test logic. Supports VMIC analog multiplexer product line.	VMIVME-3100	VME-Microsys		Digital, 128-bit turbomodule with jumper-selectable individual-port direction control, options include negative or positive true I/O.	VMIVME-2528	VME-Microsys	45
Anti-aliasing filter, 4-channels with independent filter circuits, selectable cutoff frequencies	IV1649	Ironics		DMA link, VME to VME link supports high speed 8-16- and 32-bit transfers between two VME busses.	VMIVME-DMAL	VME-Microsys	
				Emulation of DEC DR11-W high-speed parallel DMA interface for use as interprocessor link or general purpose peripheral device interface. 2M byte/second transfer rate, 6U form factor.	10084	IKON	
				Enables the IBM PC to become a master on the VMEbus. This allows the PC to communicate with any slave on the VMEbus.	PC/VME-STD	AjidaTech	

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◊ Available in Surface Mount Package

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>							
<b>I/O</b>				<b>(Cont'd)</b>			
Enhanced graphics card. Supports EGA, CGA, and monochrome graphics. Plugs onto VME0286AT board.	VAT0864P/EGA	LogicalDes		Interface/controller for up to three Winchester drives (ST506 interface) and up to four IBM 3740 format single or double sided floppy drives with Shugart compatible interface.	PME-WFC-1	Plessey	25
Fast analog input module with 32 single-ended or 16 differential analog inputs, conversion times up to 100 kHz throughput.	XVME566	Xycom		Interface for SASI controller to handle Winchester disk, floppy disk and tape drives, with 4-channel programmable DMA controller and local RS232C SIO channel for diagnostic access.	PME-SASI-1	Plessey	
General-purpose I/O module, eight serial channels, twenty-four parallel lines	GMSV01	GenMicro		Interface from VMEbus to Network Systems Corporation A-400 HYPERchannel and B-400 HYBERbus Adapters. 6U (double-high) form factor.	10090	IKON	
Global interrupter and interrupt expansion module, eight independent global-interrupt channels, eight external input interrupt channels.	VMIVME-5010	VME-Microsys		Isolated A/D expansion multiplexer, 32 single-ended/16 differential, expandable to 120 DI, compatible with 41-220.	41-223	Anasco	
Hard and floppy controller card with 20 Mbyte hard disk drive and 720K 1/2" floppy disk drive for VME0286AT system.	VAT622HFC20	LogicalDes		Isolated analog output and digital I/O, two 4 to 20 mA outputs, 12-bit resolution, 8 isolated digital inputs, 8 digital outputs, 1 kV isolation	41-221	Anasco	
Hard and floppy disk controller card, supports two hard/two floppy drives. For VME0286AT system.	VAT622S	LogicalDes		5 Long line (RS-485), DMA link supports parallel data transfers over long cable (up to 2000 ft.) utilizing differential long-line drivers and receivers. Lateral parity is provided.	VMIVME-DMAL/485	VME-Microsys	
High resolution analog input board, Eight channels with 16Kx16 words of RAM.	MPV911	Burr-Brown		Long line (RS-485), DMA link supports parallel 16-bit data transfers over long cable (up to 2000 ft.) utilizing differential long line drivers and receivers, lateral parity is provided.	VMIVME-DR11W/485	VME-Microsys	30
High speed analog output board, eight output channels, on-board RAM expandable to 16Kx12 words, 12-Bit resolution	MPV954	Burr-Brown		Magnetic tape interface adapter-buffer 1/2-inch 9-track, 4K bit FIFO buffer.	MVME435	Motorola	
High-density 12-bit analog I/O board. Capable of A/D conversions on 16 analog inputs and 16 analog (D/A) outputs. Built-in test logic allows for each of the 16 analog outputs to be selected and multiplexed to the A/D converter for accuracy verification.	VMIVME4512	VME-Microsys		Master/Master capabilities, interface to Gould-Sel 32 series, provides a 32-bit DMA link between the VMEbus and the Gould-Sel HSD model 9132.	VMIVME-HSD	VME-Microsys	
High-speed data movement. Up to 40Mbyte/s VME-to-VME or VME-to/from user I/O Data transfers with digital signal processing capability.	IV3272	Ironics		10 Medium and high power dc output card. Switches 0.5 A with 1.5 W dissipation or 5 A with 20 W dissipation.	VME701	Micro-Link	
High-speed fiber optic serial VME to VME link, up to 10 Mbits/s.	VMIVME-6010	VME-Microsys		Miscellaneous, Dual channel RS232C communications module. Two I/O channel compatible, full duplex serial I/O ports, enables synchronous/asynchronous baud rates of 50 to 19.2 kb/s as a terminal or modem.	MVME400	Motorola	
Host computer interface. General purpose DMA controller that supports 8, 16, or 32-bit transfers. Supports up to 6.25 M bytes/s.	VMIVME-DMA	VME-Microsys		MK68000 CPU (8-MHz), one RS232 serial I/O channel.	MK75601	Thomson	35
I/O transition module. Compatible with Motorola MVME 708-1, for serial and parallel interfaces.	TVME 1641	TLIndustries		Module with six RS-232 serial ports and two Centronics parallel ports. Baud rates are individually software selectable on each serial channel, 3 bytes of FIFO buffer for every input channel.	IOSP	DUAL	
IEEE-488 GPIB interface that converts a VME system into a controller that manages groups of remotely programmable test and measurement devices within a GPIB instrumentation system.	IV1621	Ironics		15 Multibus-I to VME bus adaptor.	422	Bit3Comp	
IEEE-488 Hardware interface GPIB-DP dual port, handler available.	77609301	NationalInst		Multiplexer expansion module for the VMIVME-31XX series of A/D modules. Requires VMIC's AMXbus P2 analog backplane that supports up to 16 expansion multiplexers on a single bus utilizing a single ADC. Has 64 single-ended channels or 32 differential channels.	VMIVME3210	VME-Microsys	
IEEE-488 Hardware interface GPIB-1014-1 DMA I/O, handler available.	77605901	NationalInst		Parallel I/O board. 64-line medium power parallel I/O with 10 high-performance counter/timer channels.	MV4500	MicroSys	
IEEE-488 Hardware Interface GPIB-1014P-1 programmed I/O, handler available.	77606201	NationalInst		Parallel I/O board with direct interface to OPTO-22 motherboard. Provides two sets of three 8-bit ports giving 48-bits of bi-directional I/O.	IV1623	Ironics	40
Intelligent asynchronous serial controller module with RS-232C, RS-422A or TTL interface.	XVME420	Xycom		20 Parallel I/O with opto-isolator. Micro/Sys' MV4500 with opto-isolator on 16 input lines.	MV4500-1	MicroSys	
Intelligent high-isolation A/D, four differential, 12-bit plus sign resolution.	41-225	Anasco		Parallel interface module with 32-bits of I/O for industrial control applications. Two independent 24-bit timers.	MS-PIM	Matrix	
Intelligent isolated analog input, 8 differential channels, 14-bit resolution, on-board linearization and CJC, RS-422, 1 kV isolation	41-220	Anasco		Piggyback module for RS-232C serial interface for use with VMPM68KB, VSIO, and MPM68008 CPU boards.	RS232-PB	PEP-Modular	
Intelligent multifunction I/O controller, 8 serial ports, 2 printer ports, one 16-bit parallel port.	VME-IMIO	IntSolutions					
Intelligent serial interface. Z80 processor, capacity for 32K EPROM and 32K dual-port static RAM. Four RS-232 ports.	VME409	Micro-Link					
Intelligent 8-channel serial I/O interface, 68010 CPU, 128/512 dual ported SRAM, RS-232/RS422, multiprotocol.	ISIO1/2	Force					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>							
<b>I/O</b>							
<b>(Cont'd)</b>							
Piggyback module for RS-422 serial interface for use with VMPM68KB, VSIO, and MPM68008 CPU boards.	RS422-PB	PEP-Modular		VME SASI compatible interface, DMA can transfer up to 64 Kbyte data blocks, enables up to eight SASI disk controllers (hard or floppy) to interface to VMEbus.	MK75802	Thomson	
Pulse-rate-input module, supports 8- or 16-bit data transfers, four channels.	VMIVME-1140	VME-Microsys		VME to VME transfers under program control, supports 8- 16- and 32-bit data transfers over long cable (up to 2000 ft.) utilizing differential long line drivers and receivers.	VMIVME-5510	VME-Microsys	
P2 to PC cable interface card set. Allows off the shelf AT peripheral boards to be used with VME-0286AT.	VAT596	LogicalDes		VMEbus to I/O channel interface.	VMVME316	Motorola	
Relay module, 32-channel mercury wetted relay module, supports 8 or 16-bit data transfers.	VMIVME-2200	VME-Microsys		Dual 16-bit parallel I/O. Four independent 8-bit ports with two handshake lines per port, centronics type parallel interface outputs for two printers.	VMVME410	Motorola	30
SASI bus peripheral interface adapter. Single host non-arbitrating SA400 disk controller interface for I/O channel.	VMVME420	Motorola		Quad parallel port, 8 configurable handshake lines	48210E	Bicc-Vero	
SBIO, Complementary I/O board for Centronics interface applications with VME-9100D.	SBIO201	LogicalDes	5	Quad serial port, sync/async operation	48200J	Bicc-Vero	
SBIO, Complementary use interface wirewrap through VME-9100D.	SBIO501	LogicalDes		Two RS-232 ports and two RS-422 ports with baud rates up to 38.4 Kb/s.	VME404	Micro-Link	
SBIO, Complementary 48 channel TTL interface buffer card to two 8, 16, or 24 Channel Opto-22 motherboards with VME-9100D.	SBIO248	LogicalDes		Two serial ports optionally support RS-232, RS-422, RS-485, 20mA current loop, fiber optics of X.25. 16 parallel I/O lines and 4 control lines.	VSIO	PEP-Modular	
SBX I/O board with eight interrupts. Quad SBX carrier supporting eight VME bus interrupts.	MV4400-1	MicroSys		Two VMIVME-DR11W's operate back-to-back to support data transfers up to 2.25 Mbytes/s. Cable lengths up to 50 ft.	VMIVME-DR11W	VME-Microsys	35
SBX I/O card with four interrupts. Quad SBX carrier supporting four VME bus interrupts.	MV4400	MicroSys	10	Four channels of RS-422/485 with baud rates up to 38.4 Kb/s.	VME401	Micro-Link	
SCSI Host adapter.	VME-SCSI	IntSolutions		Four RS-232 ports. Baud rates up to 38.4 Kb/s.	VME403	Micro-Link	
SCSI host card. For VME0286AT system.	VAT670	LogicalDes		Four serial I/O channels, asynchronous operation to 19.2 kilobaud, synchronous operation to 307.2 kilobaud.	DSIO	Thomson	
Serial and parallel I/O on a double EUROcard board. Contains four RS-232C asynchronous serial ports and one Centronics parallel port. Also included is a 24-bit timer for single or periodic interrupts.	VMVME335	Motorola		Four serial I/O channels, two fixed RS232 and two selectable RS232 or RS422.	MK75801	Thomson	
Serial I/O board. Intelligent eight channel board with one Centronics compatible channel. Optimized for UNIX; reduces processor and bus load caused by terminal handling to a minimum.	PME SIO-3	PlesseyMicro		Four serial ports and two parallel lines; 2-inch by 8-inch socket area for memory and real-time clock. On-board lithium battery backup; 512 Kbytes of CMOS static RAM.	VME9100D	LogicalDes	40
Serial I/O board. Intelligent 68020 based 16 channel with two multi-protocol synchronous ports, 1 Mbyte dual-ported RAM.	PME SIO-4	PlesseyMicro	15	Four sites for IEEE-P959 (SBX) I/O modules. 8 or 16-bit transfers, single or double wide modules. Programmable interrupt vector, bus error assertion for non-existent modules.	PG3900	MicroInds	
Serial interface board with four channels of RS-232C or RS-422A communications.	XVME400	Xycom		Four-channel analog output	48240D	Bicc-Vero	
Serial interface board with four channels of RS-422.	XVME401	Xycom		Four-port serial I/O board; four full duplex multiprotocol serial I/O ports, VMEbus interrupter, complete VMEbus slave interface (A16, D8) with interrupter.	IV1625	Ironics	
Similar to the PC/VME-STD, except that it supports the double-high VME bus with full 32-bit data and address capability.	PC/VME-EXT	AjidaTech		Six-channel SIO board with freely selectable RS232C or RS422 interface. Programmable asynchronous or synchronous operation using IBM bisync BSC, DDCMP, X3, 28, X21, SDLC, HDLC, X25 or other protocols. Software programmable rate from 110 to 38400 baud.	PME-SIO-1	Plessey	
Supports 8 and 16-bit data transfers over long cables (up to 2000 ft.) utilizing differential long line drivers and receivers. Software transparent. All seven interrupt levels supported. Provides low cost VME bus expansion to support large slave I/O subsystems.	VMIVME-RepeatL/485	VME-Microsys		Six-port asynchronous/synchronous serial I/O.	VMVME331	Motorola	45
System I/O, 144 buffered digital I/O lines	GMSV04	GenMicro	20	Sixteen serial ports, DMA, parallel printer port, RTC option.	VME-ICP16	IntSolutions	
Terminal I/O subsystem, supports up to 128 asynchronous RS-232C devices on multi-user host, diagnostic and system administration software for fault isolation and system tuning.	HPS	Systech		Sixty-four bit contact-bounce eliminator.	VMIVME-1130	VME-Microsys	
TTL I/O. 32 TTL lines, four real-time input lines, four interrupt input lines.	VME702	Micro-Link		Eight channel 16-bit D/A converter that offers fast settling of analog output of 10 microseconds maximum to 0.003% of full scale range. Buffered voltage output. Supports VMIC's analog expansion and built-in test bus (AMXbus).	VMIVME4116	VME-Microsys	
Universal I/O board with all I/O on daughter boards. Accepts 0-8 serial ports, 0-80 lines of parallel I/O.	OB68K/VIO	Omnibyte		Eight port intelligent I/O board: Eight Full Duplex Multiprotocol Serial I/O Ports, on-board 68000 processor, on-board 4Kx32 bit dual-port RAM, on-board 128 Kbyte private dynamic RAM VMEbus interrupter, VMEbus master and slave interface, functions as a CPU board in multiprocessor systems.	IV1624	Ironics	
Up to eight hard disk controllers, SASI interface, byte or word DMA data transfer.	VME-NOCI	Thomson	25				
Up to isolated input.	PIO-1	Force					
Up to 250Kb, synchronous.	SIO-1	Force					

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>							
<b>I/O</b>							
<b>(Cont'd)</b>							
Eight port serial I/O board.	IOS8	DUAL		64 parallel lines, three 24-bit timers, one 32-bit and one 16-bit data channel	MVME340	Motorola	25
Eight serial ports, DMA, parallel printer port, RTC option.	VM-ICP8	IntSolutions		80 TTL-level channels. Can be programmed for 64 inputs or outputs. Eight channels are for interrupt inputs and eight are for flag outputs.	XVME240	Xycom	
Eight-channel asynchronous multiplexer, dedicated 68000, full duplex at 19.2 Kbaud, programmable, all channels may run simultaneously	8-ASYMUX-A	Alcyon		32 single ended, 16 differential analog input, 2 analog output lines 12-bit resolution.	ADDA-1	Force	
4-Channel serial Module 1M bits/s max data rate. RS232C, RS422, RS423, RS485 compatibility RS485 Local Area Network capability.	VMIVME6015	VME-Microsys		48-line digital I/O board. Software programmable inputs and outputs. Compatible with Gordos and Opto-22 I/O module systems.	DVME-660	Datel	
6 channel serial I/O interface, RS-232/RS-422, multiprotocol, optional fiberoptic interface.	S102	Force		68450 DMAC, 68153 Bus interrupt modules for flexible interrupt handling DPTO insulation on input and output.	OPIO-1	Force	
8-Channel, Isolated Thermocouple inputs with on-board Cold junction compensation. Compensated for Thermocouple types. J,K,T,E,R,S,B wide input ranges. $\pm 5\text{mV}$ to $\pm 100\text{mV}$ or $\pm 50\text{mV}$ to $\pm 5\text{V}$ . Each input channel is complete, providing input protection, isolation, common mode rejection, multiplexing filtering and amplification. Input signals may be multiplexed to any of the VMIVME-3100 series of A/D Converter modules.	VMIVME3230	VME-Microsys	5	<b>Mathematics</b>			
8-Channel 12-bit Analog Output Module with voltage or 4-20mA current output option. Selectable voltage or current output ranges.	VMIVME4110	VME-Microsys		Fixed-point array processor, 10 MOPS, 50-kHz real-time bandwidth, 32 Kbyte dual-port RAM	43-200	Anasco	30
16 channel I/O channel interface. Up to 16 ac or dc solid-state relay or output signals.	M68RIO1-1	Motorola		8 MIP Array Processor, with ADSO-2100 DSP processor	RTI680	AD	
16-Channel Analog Output (S/H per channel) and 16 single ended high level analog input multiplexer module. The module supports on-line and off-line fault detection and isolation. The low cost AIO module supports analog input expansion by utilizing up to 16 model 4500's connected to any of VMIC'S ADC series modules. VMIC'S analog multiplexer backplanes are required.	VMIVME4500	VME-Microsys		<b>Memories</b>			
16-channel analog output, 32 optional	48250L	Bicc-Vero	10	Add-on Memory board for the VMEbus. 4, 8, 12, and 16 Mbyte configurations. Uses 1MB chips with 180 ns access times.	CI-VMEemory	Chrislin	
16-channel asynchronous multiplexer, dedicated 68000, full duplex at 19.2 Kbaud, all channels may run simultaneously	16-ASYMUX-A	Alcyon		Battery back-up, mixable 512K bytes of RAM, or 2M bytes of EPROM.	VMEM-S1	PEP-Modular	
20 Mbyte hard disk drive with hard/floppy controllers for VME0286AT system.	VAT622MC20	LogicalDes		Bubble memory module, 512K or 1 MB.	XVME164	Xycom	
32 bi-directional TTL I/O channels with interrupts.	XVME200	Xycom		Cache Accelerator Module for VME based systems, 16Kb cache, zero-wait-state operation	MVMEXTCAC-1	Motorola	35
32 channels of optically isolated digital inputs.	XVME210	Xycom			MVMEXTCAC-2	Motorola	
	XVME212	Xycom		CMOS RAM/ROM provides sixteen 28-pin sockets for combinations of user-supplied RAM, ROM and CMOS RAM. 1 Mbyte maximum capacity.	MVME211	Motorola	
32 channels of relay outputs which are software readable.	XVME260	Xycom		Combination SRAM/ROM/EPROM memory board with 16 x 28 pin sockets to support 24 or 28 pin JEDEC-compatible devices for a maximum capacity of 512 Kbyte EPROM or ROM or 128 Kbyte SRAM.	PMECRR-1	Plessey	
32 optically isolated digital outputs.	XVME220	Xycom		Control-status register, parity separate 256 banks.	DRAM-1	Force	
32-channel isolated digital input, contact closure	MPV910	Burr-Brown		Dynamic RAM module, 2 Mbyte with VME subsystem bus (VSB). Enhanced performance over the MVME204-2. Dual ported 32-bit address/data VSB interface.	MVME204-2F	Motorola	40
32-channel isolated digital input, high voltage	MPV910-NS	Burr-Brown		Dynamic RAM module, 256 Kbytes.	MVME201	Motorola	
32-channel isolated digital input, low-voltage	MPV910-LV	Burr-Brown		Dynamic RAM module, 512 Kbytes.	MVME202	Motorola	
32-channel relay output board	MPV902	Burr-Brown	20	Dynamic RAM module, 512KB/1MB with 200-ns access time.	VMEM-D	PEP-Modular	
32-Channel SE/16-Channel Differential High-Level $\pm 10\text{V}$ low cost Analog Expansion module with field isolation switches and analog input test buses to support fault isolation to card level. The analog input test signal is supplied by VMIC'S analog output module. Up to 16 analog input multiplexers may be connected to one VMIC ADC for economical analog input expansion. Analog multiplexer backplanes are required.	VMIVME3200	VME-Microsys		Error detection and correction (EDAC) memory board. Standard 4MB/2MB DRAM. Uses ZIP DRAMs for high density. Corrects all single-bit errors and detects all double-bit errors.	IV3214	Ironics	
48-channel TTL I/O	MPV930-48	Burr-Brown		Fast SRAM, separate 256 K banks, on-board battery back-up.	SRAM-2	Force	45
64 Channel Optically coupled I/O, 32 inputs (5-12V) plus 32 high current drivers (1.5A)-Power transition output protection, 24 volt option.	VME2232D	LogicalDes		Fast SRAM, separate 64 K banks. Active battery back-up on board.	SRAM-1	Force	
				Management CPU. MK68000 processor and MK68451 memory management unit.	MK75602	Thomson	
				Master-slave to 28 MB, parity, supervisor/user access.	DRAM-E4	Force	
				Mix up to 2 Mbytes of static RAM or EPROM on this full MIL-SPEC or ruggedized board. Dual-ported RAM.	PMV SME-1	PlesseyMicro	
				Multi-purpose memory board with 32-bit addressing and battery backup. Supports RAM, ROM, EPROM, and EEROM.	PME CRR-2	PlesseyMicro	50

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>							
<b>Memories (Cont'd)</b>							
Parity. 65 ns write access, expandable to 13 MB.	DRAM-E3	Force		1 Mbyte dynamic RAM module. Dual ported for use with VMEbus and multiplexed MVMx32bus (Motorola Proprietary Expansion Bus). Parity error checking.	MVME204-1	Motorola	
Programmable parity response	DRAM-2	Force		1 Mbyte expansion, dynamic RAM with error checking on byte boundaries, P2 connector	VMEMEM-1	Alcyon	
PROM/RAM/EEPROM board.	CD23/2200	CentData		1 Mbyte RAM board set (2 VME boards) byte parity, 8, 16 and 32-bit transfer supported.	VEM1024	CharlesRiver	
RAM (dual ported) 512 Kbyte, 1 Mbyte, 2 Mbyte versions.	VME-HSMEM	IntSolutions		1-Mbyte dynamic RAM, transparent refresh, parity error detection, 8/16/32-bit data, 24-bit addressing	44-310	Anasco	30
RAM/PROM module, 8 byte wide memory sockets, time of day clock/calendar, on-board battery back-up.	XVME100	Xycom	5	1Mb DRAM memory, 1, 2, 4, 6, 16 mB capacity, IBM system 9000-compatible, CSR, on-board EDC, battery back-up, lifetime warranty.	VERSARAM	Clearpoint	
RAM 512 Kbyte, 1 Mbyte 2 Mbyte versions.	VME-MEMI	IntSolutions		1Mb DRAM memory, 2, 4, 8 mB capacity, CSR, EDC, BMT, UAT, lifetime warranty.	VSBRAM	Clearpoint	
Static RAM and EPROM module, 128 Kbytes of RAM or 256 Kbytes of EPROM, battery backup is available.	VMEM-S	PEP-Modular		2 MB dynamic RAM with byte parity. VME/VMX bus compatible, dual-ported 8, 16, 32-bit transfers, 24- and 32-bit addressing with memory protect, uses 256K devices.	PG2222	MicroInds	
Static RAM/ROM with VSB (VMEbus subsystem bus). Storage capacity up to 1 Mbyte, supports 24- or 32-bit addressing on VMEbus, 32-bit addressing on VSB. 100 to 400 ns access times.	MVME214	Motorola		2 Mbyte dynamic RAM.	48606G	Bicc-Vero	
static RAM/ROM, 16 unpopulated sockets for 28-pin and 24-pin memory devices, memory size up to 128 Kbytes per module.	MVME210	Motorola		2 Mbyte dynamic RAM module. Dual ported for use with VMEbus and multiplexed MVMx32bus (Motorola Proprietary Expansion Bus). Parity error checking.	MVME204-2	Motorola	35
Universal Board. Twenty-four universal 28-pin memory sockets for EPROM, EEPROM, ROM/RAM. Two independent memory banks, 8, 16, 32 bit data transfers, 16 Kbyte to 256 Kbyte memory chips.	IV-3212-01	Ironics	10	2 Mbyte dynamic RAM with parity, 4 way word/2 way longword interleaving. With odd-even board pairs interleaving, the effective cycle time is reduced below 333 ns.	IV-3211-2MB	Ironics	
Up to 17 Mbytes of non-volatile bubble memory, insensitive to rugged environments.	PME BB1	PlesseyMicro		2 Mbyte expansion, dynamic RAM with error checking on byte boundaries, P2 connector	VMEMEM-2	Alcyon	
Up to 512K bytes of static RAM.	PME512S	PlesseyMicro		2 Mbyte Expansion module for PME1EA.	PME DB2EA	PlesseyMicro	
Up to 8 Mbytes of DRAM, supports block move and unaligned transfers, dual-ported to VME and VSB with parity generation and checking.	PME 2SB	PlesseyMicro		2 Mbyte Expansion module for PME2EP.	PME DB2EP	PlesseyMicro	
Up to 8 Mbytes of DRAM, supports unaligned transfers and block move, sustained data transfer rates in excess of 30 Mbytes.	PME 8EP	PlesseyMicro		2 Mbyte RAM board set (2 VME boards) byte parity, 8, 16 and 32-bit transfer supported.	VEM2048	CharlesRiver	40
Up to 8 Mbytes of DRAM with data read-ahead and block move capability, supports unaligned transfers and performs parity generation and checking.	PME 8SE	PlesseyMicro	15	2 megabyte dynamic RAM, 64-bit prefetch cache provides 85 ns sequential reads, 16 and 32-bit data transfers, A32, D32	VME4226D	LogicalDes	
User installable EPROM, PROM, SRAM to 16MB, 32-bit wide accesses, VMKbus interface.	RR2	Force		2-Mbyte dynamic RAM daughter board	44-213-DB	Anasco	
User installable EPROM, PROM, SRAM to 16MB, 32-bitwide accesses.	RR3	Force		2-Mbyte dynamic RAM, transparent refresh, parity error detection, 8/16/32-bit data, 24-bit addressing	44-312	Anasco	
Wait-less VMEbus memory. 2M byte DRAM board for older and slower VMEbus systems, increases performance by up to 40%. Access time: 40 ns for memory write and 125 ns for memory read.	WLM-2	Alcyon		3 MB dynamic RAM with byte parity. VME/VMX bus compatible, dual-ported 8, 16, and 32-bit transfers. 24- and 32-bit addressing with memory protect. Uses 256K devices.	PG2223	MicroInds	
One megabit ZIP DRAM memory, 8 and 16 MByte capacity, on-board EDC.	VMERAM	Clearpoint		4 MB dynamic RAM with byte parity. VME/VMX bus compatible, dual-ported 8, 16, and 32-bit transfers. 24- and 32-bit addressing with memory protect. Uses 256K devices.	PG2224 PG2225	MicroInds MicroInds	45
Two or four Mbyte, error detection/correction, status LEDs, UAT, RMW.	DRAM5	Force	20	4 Mbyte RAM board set (2 VME boards) byte parity, 8, 16 and 32-byte transfer supported.	VEM4096	CharlesRiver	
1 Mb Byte parity memory board.	VCM1024	CharlesRiver		4 megabyte dynamic RAM, 64-bit prefetch cache provides 85 ns sequential reads, 16 and 32-bit data transfers, A32, D32	VME4246D	LogicalDes	
1 MB dynamic RAM. Automatic refresh, unaligned and block transfers.	VME300	Micro-Link		4-Mbyte dynamic RAM	48607D	Bicc-Vero	
1 MB dynamic RAM module with parity.	XVME102	Xycom		8 MB dynamic RAM with byte parity. VME/VMX bus compatible, dual-ported 8, 16, and 32-bit transfers. 24- and 32-bit addressing with memory protect. Uses 1 MB devices.	PG2226	MicroInds	50
1 MB dynamic RAM with byte parity. VME/VMX bus compatible, dual-ported, 8, 16, 32-bit transfers, 24- and 32-bit addressing with protect. Uses 256K devices.	PG2221	MicroInds		8-Kbyte CMOS RAM, 32 Kbytes optional, battery-backed with clock	48070B	Bicc-Vero	
1 Mbyte CMOS RAM module. On-board battery for power down backup.	MVME215-3	Motorola	25	8MB DRAM with Error Correction for VME.	CI-VME8	Chrislin	
1 Mbyte dynamic RAM.	48055F	Bicc-Vero					

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line	
<b>VMEbus</b>								
<b>Memories (Cont'd)</b>								
12 MB dynamic RAM with byte parity. VME/VMX bus compatible, dual-ported 8, 16, and 32-bit transfers. 24- and 32-bit addressing with memory protect. Uses 1 MB devices.	PG2227	MicroInds	5	1024 KB dynamic RAM with parity. 8, 16 or 32-bit transfers with two-way interleaving supported, memory protection supported.	PG2205	MicroInds	30	
16 MB dynamic RAM. Automatic refresh, unaligned and block transfers.	VME356	Micro-Link		1024 Kbyte DRAM with EDAC circuitry, 16 or 32 bit data word operation	M68KVM11-3	Motorola		
16 MB dynamic RAM with byte parity. VME/VMX bus compatible, dual-ported 8, 16, and 32-bit transfers. 24- and 32-bit addressing with memory protect. Uses 1 MB devices.	PG2228	MicroInds		2048 Kbyte DRAM with EDAC circuitry, 16 or 32 bit data word operation	M68KVM11-4	Motorola		
20 JEDEC-compatible sockets in two banks: 4 sockets and 16 sockets. 32-bit address and data. Accommodates SRAM, ROM, PROM, EPROM, and EEPROM. VMXbus interface with battery back-up facilities.	PG2260	MicroInds		1 Mbyte DRAM memory board with EDC, 8/16/32-bit data, 24-bit address, 150 ns write and 300 ns read access.	PME1EA	Plessey		
32 Kbyte cache memory and a 50 Hz frame store.	VAP-FS	DSP-Systems		128 Kbyte SRAM memory board, 8/16-bit data, 24-bit address and 140 ns read/write access. On-board lithium battery back-up provides up to 1000 hours data retention.	PME128S	Plessey		
32 Kbyte memory for the VAP-AP board.	VAP-32K	DSP-Systems	10	16 28-Pin JEDEC sockets, 8 individually addressable banks.	RR-1	Force	35	
64-Kbyte CMOS RAM with 256 Kbyte optional, battery maintained	48640J	Bicc-Vero		2 MB improved speed thru write cache; parity UAT, RMW.	DRAM6	Force		
128-Kbyte static RAM	44-320	Anasco		2 Mbyte DRAM daughter board for PME 1EA, with 150 ns write access and 300 ns read access. Mounts onto mother board within VMEbus card profile, increasing capacity of PME 1EA to 3 Mbyte.	PMEDB2EA	Plessey		
256 KB dynamic RAM with ECC. VME/VMX compatible, dual-ported 24- and 32-bit addressing, error logging, memory protection supported.	PG2210	MicroInds		2 Mbyte DRAM memory board with byte parity, 8/16-bit data, 24 bit address, 190-ns write access and 300 ns read access.	PME048D	Plessey		
256 KB dynamic RAM with parity. 8, 16, or 32-bit transfers. Two-way interleaving supported, memory protection supported.	PG2200	MicroInds		2 Mbyte high-performance DRAM daughter board for PME 2EP, with 150-ns write access and 270-ns read access. Mounts onto mother board within VMEbus card profile, increasing capacity of PME 2EP to 4 Mbyte.	PMEDB2EP	Plessey		
256 KB, 512 KB, 1MB CMOS SRAM, on-board battery backup, UAT, RMW.	SRAM4	Force	15	2 Mbyte high-performance DRAM memory with byte parity, 8/16/32-bit data, 24-bit address, 150ns write access and 270ns read access.	PME2EP	Plessey	40	
256 Kbyte CMOS RAM module. on-board battery for power down backup.	MVME215-1	Motorola		2MB high-speed CMOS SRAM, on-board battery backup.	SRAM6	Force		
256 Kbyte dynamic RAM card, automatic refresh.	MK75701	Thomson		256 Kbyte DRAM memory board with EDC, 8/16/32 bit data, 24 bit address, 150 ns write access and 300 ns read access.	PME256EA	Plessey		
256-Kbyte dynamic RAM, transparent refresh, parity error detection, 8/16/32-bit data, 24-bit addressing	44-302	Anasco		512 KB Byte parity memory board.	VCM512	CharlesRiver		
512 KB high-speed CMOS SRAM, on-board battery-backup.	SRAM5	Force		512 Kbyte DRAM daughter board for PME-256EA with 150 ns write access and 300 ns read access. Mounts onto mother board within VMEbus card profile, increasing capacity of PME-256EA to 768 Kbyte.	PMEDB512EA	Plessey		
512 KB or 1 MB CMOS SRAM, on-board battery backup, VMX interface.	SRAM3	Force	20	512 Kbyte DRAM memory board with byte parity, 8/16-bit data, 24 bit address, 190-ns write access and 300-ns read access.	PME012D	Plessey	45	
512 Kbyte CMOS RAM module. On-board battery for power down backup.	MVME215-2	Motorola		512 Kbyte high performance DRAM memory board with byte parity, 8/16/32 bit data, 24-bit address, 150-ns write access and 270-ns read access.	PME512EP	Plessey		
512 Kbyte dynamic RAM with parity, 4 way word/2 way longword interleaving. With odd-even board pairs interleaving, the effective cycle time is reduced below 333 ns.	IV-3211-512K	Ironics		512 Kbyte high-performance DRAM daughter board for PME 512EP, with 150-ns write access and 270-ns read access. Mounts onto mother board within VMEbus card profile, increasing capacity of PME 512EP to 1 Mbyte.	PMEDB512EP	Plessey		
512 Kbyte Expansion module for PME 256EA.	PME DB512EA	PlesseyMicro		<b>Multifunction</b>				
512 Kbyte expansion module for PME512EP.	PME DB512EP	PlesseyMicro		Array processor, 10 MOPS, performs fixed point array processing, digital filtering, A/D conversion, complex Fast Fourier transforms, and frame storage.	VAP-AP	DSP-Systems		
512 Kbyte RAM board set (2 VME boards) byte parity, 8, 16 and 32-bit transfer supported.	VEM512	CharlesRiver	25	Complete single-high VME bus processor board with either 68000 or 68010 processor.	XVME601	Xycom	45	
512 MByte dynamic memory, 350 ns read /300 ns write, parity, 32-bit data transfers, 24 or 32-bit addresses.	loVME201	loInc						
512-Kbyte dynamic RAM	48051G	Bicc-Vero						
512-Kbyte dynamic RAM, transparent refresh, parity error detection, 8/16/32-bit data, 24-bit addressing	44-305	Anasco						
512K SRAM, 256K PROM, battery option.	VME4324D	LogicalDes						
1024 KB dynamic RAM with ECC. VME/VMX compatible, dual-ported 24- and 32-bit addressing, error logging, memory protection supported.	PG2211	MicroInds						

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>				<b>Prototyping Boards</b>			
<b>Multifunction (Cont'd)</b>				Board with interface logic, address decoding, logic select for blocks of 16/32 addresses, seven-level interrupter.			
Digital-to-synchro/resolver converter which utilizes either one or two digital -to-synchro/resolver converters depending on option chosen. 14-bit converter with an overall accuracy of $\pm 4$ ARC-minutes.	VMIVME4905	VME-Microsys			VME5100D	LogicalDes	
Implements full SCSI functions. Full compliance with ANSI SCSI X3T9.2 and VME bus revision C.1 specifications, 512 Kbytes of dual-port RAM, DMA transfers.	451-48231E	Bicc-Vero		Buffered development card with 2.75" x 3.75" user area.	VME902	Micro-Link	
MIL-STD-1553 bus controller, bus monitor, and remote terminal unit. Interfaces the VMEbus system to the MIL-STD-1553 data bus. $\pm 12$ VDC operation.	BUS65502 BUS65503	ILC-DDC ILC-DDC		Buffered development card with 3.5" x 5.5" user area, access to P2 connector.	VME951	Micro-Link	
MPCI compatible parallel DMA interface provides interface from VMEbus to Gould/Sel MPC1 board. VMEbus compatible. Fully programmable operation.	VMIVME-MPCI	VME-Microsys	5	Complete VME bus interface with 68172 bus controller, single-level bus arbiter, ROR or RWD, 7-level interrupt handler, standard size.	PG2750 PG2751	MicroInds MicroInds	20
Provides various VMEbus system resources suitable for multiprocessor systems.	XVME010	Xycom		Prototyping board, blank Wire-Wrap module which includes VMEbus and MAXbus interface.	PROTOMAX	Datacube	
VMEbus processor module. Works on Motorola I/O channel bus. MC68010 CPU at 10 MHz, 512 Kbytes dual access RAM (dynamic), two EPROM sockets for up to 128 Kbytes of zero-wait state EPROM. Four timers, 24-bit timer with 125 ns resolution, Local and VMEbus timeout, and Watchdog timers.	MVME104	Motorola		Prototyping board, wire wrap, with VME bus interface.	6159L	Bicc-Vero	
VMEbus processor module (same as MVME104 but connects to 5 1/4 floppy disk)	MVME106	Motorola		Provides a single height prototyping grid and all signals required for VME hardware development.	XVME087	Xycom	
VMEbus processor module (same as MVME104 but designed for embedded controller and small real-time system applications)	MVME105	Motorola		Selectable address decod., full VME interface-A16/D16, 7 level interrupt control, .1X.1 grid component area, 80% of board free for designer circ.	VME5100S	LogicalDes	
VMEbus processor module (same as MVME104 but has SCSI bus interface)	MVME107	Motorola	10	<b>Speech Circuits</b>			
VMEmodule 32-bit Monoboard microcomputer. MC68020 microprocessor with 32-bit address and data at 16.67 MHz. MC68851 Paged Memory Management Unit, 4Mbytes of local DRAM accessible from the VMEbus, 2 Kbytes of battery backup RAM.	MVME134	Motorola		Encoder, Voice output, digitized for high-quality speech or sound, download from disk to RAM or speak from on-board EPROM, line and speaker outputs.	MV1500	Microvoice	25
Dual SCSI host adapter. Two full-function SCSI ports (sync/async) that can both operate simultaneously. Exclusive BUSpacket interface boosts DMA data rates up to 30 MB/s.	V/SCSI 4210	Interphase		<b>Miscellaneous</b>			
Two board set is fully compatible with PC/AT, complete with video graphicscontroller, disk controller, and keyboard interface.	XVME682	Xycom		A full A32/D32, FIFO-buffered version of the IKON model 10084. High-performance DR11-W Emulator. Can achieve data transfer rates in excess of 4Mbytes/s.	10089	IKON	
8-Channel RTD or Strain Gauge Conditioners. A multipurpose Multiplexer Module is designed with input protection while multiplexing and amplifying of low-level signals ( $\pm 30$ mV to $\pm 100$ mV) such as those provided by RTD and strain gauge sensors. $\pm 10$ volt excitation current output is available for strain gauge sensors. Input signals may be multiplexed to any of the VMIVME 3100 series of A/D Converter Modules.	VMIVME3220	VME-Microsys		Allows any VME bus module to be connected to VME bus backplane signals while both surfaces of the module are exposed for testing.	XVME090	Xycom	
80286 based PC/AT compatible CPU board. Dual high eurocard format, MS/DOS compatible. Serial RS-232 and parallel printer interface, keyboard port. 1 MB dual-ported RAM, P2 implemented P2/AT bus.	VME0286AT	LogicalDes	15	Anti-Aliasing filter, low-pass, 4-channel analog filter	MPV990	Burr-Brown	
				Battery backup module, data retention control for VME systems.	VBAT	PEP-Modular	
				Bus monitor. Monitors and displays VME bus cycles. Address or data-valuetriggering. Read, write, or read/write triggers.	PG2800	MicroInds	30
				Counter module. 10 16-bit counting channels with measurement, control and utility functions.	XVME203	Xycom	
				CRT emulator. Complete VT-100 with AVO emulation. 80/132 column, 24 row, smooth scroll, non-volatile setup memory, true 19200 speed, on-board Z80, serial I/O ports, composite or separate video outputs.	VME100	KSystems	
				DMA interface to 9-track 1/2 inch magnetic tape and SASI interface. Also has two asynchronous serial ports.	IoVME402 IoVME403	IoInc IoInc	
				DUAL-CHANNEL Synchro/Resolver-to-Digital Converter Module. Option includes a wide variety of reference voltages and frequencies with 10, 12, or 14 bit accuracy.	VMIVME4920	VME-Microsys	35
				General-purpose slave board that measures absolute shaft position and provides a binary output corresponding to this shaft position based on a resolver input.	BVME	Astro	

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

**Bold face indicates additional data is provided on the page noted.**



## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>VMEbus</b>				<b>VERSAbus</b>			
<b>Miscellaneous (Cont'd)</b>				<b>Controllers</b>			
IRIG-B synchronizable reader/generator, 6U format, event register, propagation delay correction, FIFO bus interface AGC, auto-polarity, 1 microsecond accuracy. Optional oven on-time rate and frequency outputs.	ATTGVME	KSystems		8-channel isolated input VMEbus expansion board. On-board CJC channel and signal conditioning.	DVME634T DVME643H	Datel Datel	15
IRIG-B time code reader. Stripper with AGC, on-board event time measurement, day through milliseconds. VME bus interface, high-speed forward/reverse read, start/stop match option.	VTTR-VMT	KSystems		<b>VERSAbus</b>			
Multipurpose programmable Counter Module allows up to 12 separate 16-bit counter outputs with selectable on-board clock rates up to 8MHz. Up to 6 counter channels may be used to determine TTL Pulse Rate Inputs. Counters may be programmed to implement Real Time Clock, Event Counter, Digital One-Shot, Programmable Rate Generator, Square Wave Generator, Binary Rate Multiplexer, Complex Waveform Generator, and Complex Motor Controller. I/O is jumper selectable for front panel or P2.	VMIVME2910	VME-Microsys		<b>Controllers</b>			
P2/AT short card adapter for use with VME-9286AT.	VAT510	LogicalDes		Floppy disk controller. Controls two daisy-chained 1 Mbyte EXORdisk III disk systems (four drives).	M68KVM20	Motorola	
Uses memory mapping to interconnect two VMEbus systems together.	411	Bit3Comp	5	SASI/SCSI, Peripheral Controller (DMA).	CC-1	CharlesRiver	
Video bandwidth harmonic analyzer board. Designed to compute three arbitrary spectral components using quadrature FIR structures at a rate of 40 MOPS. Up to 8K points transfer length.	Analyzer	Interactive		Universal disk controller for up to two SMD interface-compatible hard-disk drives and up to 4 floppy disk drives.	M68KVM21	Motorola	
VME bus analyzer. Captures 96 bus signals in its 2K trace buffer, including 32-bit address/data, handshaking, interrupt and arbitration lines. Synchronous/asynchronous sampling to 20 MHz, four trigger/trace conditions.	Analyzer	SilControls		<b>I/O</b>			
Single-Channel Synchro/Resolver-to-Digital converter with built-in-test bus to support fault isolation to the card level. Front panel LED is provided. Supports fault isolation of VMIVME-4900 modules.	VMIVME4910	VME-Microsys		Four serial ports, 1 parallel port.	TP304	CharlesRiver	20
Dual-Channel Digital-to-Synchro/Resolver with built-in-test. The VMIC module supports fault isolation to the card level by isolating field outputs and switching the synchro/resolver outputs to a test bus for conversion by VMIC'S synchro/resolver-to-digital converter. A variety of options are available to support a wide range of reference voltages and frequencies. Both 1.5VA, 4.5VA and 5.0VA options are available. Requires VMIVME-4910 for fault-isolation.	VMIVME4900	VME-Microsys		Eight serial ports, with modem control signals and 24 bit parallel port.	TP308	CharlesRiver	
Quad Channel Pulse Rate input with interrupt overflow and auto recycle. 5V to 240V AC or DC or TTL input. Also optically coupled input options.	VMIVME1140	VME-Microsys		802.2/802.3 LAN interface.	NC-1	CharlesRiver	
Quad-Channel Resolver-to-Digital converter with Built-in-Test and front panel fail LED. Each channel contains an independent 16-bit pitch counter. Options include 10,12,14, or 16 bit resolution and 3 frequency rates.	VMIVME4940	VME-Microsys		<b>Memories</b>			
800/1600 or 6250 bpi, PERTEC Interface, Start/Stop and streaming—over 200 ips, Exclusive CacheFlow operation/command queuing, M68000, 8Kor 128K Cache Buffer, DMA rates over 20 MB/s with throttle.	VTAPE3209	Interphase		1 Mbyte dynamic RAM, byte-parity checking, 8-16 bit addressing, separate addressable blocks of 32 Kbytes.	M68KVM12	Motorola	
16-channel simultaneous S/H VMEbus expansion board. 16 SE/8 DI channels, expansion for DVME-611/612 A/D boards.	DVME645	Datel		1 Mbyte, memory board with ECC error correction.	DM1024	CharlesRiver	
32 channel high level VMEbus expansion board. 32 SE/16 DI channels. Interfaces to Datel's DVME 611/612 A/D boards.	DVME641	Datel		1 Mbyte RAM board; 8, 16 and 32-bit transfer supported.	CM1024	CharlesRiver	25
				2 Mbyte, Byte parity memory board	CM2MB	CharlesRiver	
				2 Mbyte RAM board; 8, 16 and 32-bit transfer supported.	CM2048	CharlesRiver	
				4 Mb, Byte parity memory board.	CM4MB	CharlesRiver	
				4 Mbyte RAM board; 8, 16 and 32-bit transfer supported.	CM4096	CharlesRiver	
				512 Kbyte dynamic RAM with ECC, byte-parity checking, 8-16 bit addressing, separate addressable blocks of 32 Kbytes.	M68KVM11-2	Motorola	30
				512 Kbyte RAM board; 8, 16 and 32-bit transfer supported.	CM512	CharlesRiver	
				1 Mbyte DRAM, 8/16 or 32-bit data, 24/32-bit address, byte parity, optional 512Kbyte or 256Kbyte.	PSM-1VP PSM1VA	Plessey Plessey	
				4 Mbyte DRAM, 8/16 or 32-bit data, 24/32-bit address.	PSM-4VA PSM-4VP	Plessey Plessey	35
				<b>Miscellaneous</b>			
				Emulation of the DEC DR11-W high-speed parallel DMA interface for use as interprocessor link or for general purpose peripheral device interface. Bus efficiency of an 8.6Mbyte/s device; data transfer rates of 2Mbytes/s for input and 4-6Mbytes/s for output.	10083	IKON	
				Multi-channel communications module. Four asynchronous RS232C serial ports, 50 to 9600 bps baud rate, one parallel printer port and on-board intelligent peripheral controller.	M68KVM30	Motorola	

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°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Special</b>							
<b>Communications</b>							
Multifrequency receiver provides detection of multi-tone trunk address signalling. Detects multifrequency tone signals containing frequencies: 700, 900, 1100, 1300, 1500, and 1700 Hz. Compatible with CCITT R1 MF recommendations.	M985 M987 M989	Teltone Teltone Teltone		16-bit D/A converter for the MOCEE bus.	S-D/A16	Magnum	30
				32 channel A/D converter. 324 channels, 16-Bit A/D with signal conditioning.	60A/D16-32	Digitronics	
				12-Bit Eurocard A/D converter. 2 MHz word rate, TTL compatible. Used for radar digitizing, medical instrumentation, and transient analysis.	CAV1202	AD	
				12-Bit Video A/D converter. 20 MHz word rates, ECL compatible. Used for radar digitizing, medical instrumentation, digital signal processing, and spectrum analysis.	CAV1220	AD	
<b>Controllers</b>				<b>Digital Signal Processing</b>			
Microcontroller board for industrial applications. Utilizes 8031 microcontroller, 8-bit bidirectional output port, RS 422/485 serial port for external access to the controller.	CCB9	AdvControl		Application development system for designing, debugging, and evaluating DSP56001 target system equipment.	DSP56000ADS	Motorola (2893, 4754)	
Controller, includes A/N display keyboard, 40 column printer. Can be OEM custom-programmed for industrial control applications.	CNT1XXX	CAN-TRON	5	<b>Graphics</b>			
Winchester and floppy disk controller, supports 3-1/2, 5-1/4, and 8-inch floppy disks	OMTI5200	SMS		Video terminal board. Includes on-board NVRAM that retains set-up parameters such as baud rate, parity and full/half duplex operation.	CARDINAL-01	SMC	35
Winchester and QIC-02 tape controller, supports 3-1/2, 5-1/4, and 8-inch drives	OMTI5300	SMS		Video terminal board. Same as Cardinal-01 with additional DB25 RS-232 communications and printer port connectors.	CARDINAL-03	SMC	
Winchester disk controller, supports any 3-1/2, or 5-1/4 inch ST506/412 drive	OMTI3100	SMS		<b>I/O</b>			
Winchester disk controller, supports up to two ST506/412 disk drives. Drives can be fixed, removable, hard or soft sectored. 32-bit ECC and consecutive sector transfer	OMTI5100	SMS		Digital input board with 64-channel TTL compatible inputs.	1041	Basicon	
Winchester Disk Controller with SASI Interface	WD1002S-SHD	Western	10	Digital output board with 32 channels at 200 mA each.	1042	Basicon	
<b>Converters</b>				Edge-triggered latching input module. Eight optoisolated inputs.	AOELI-8	IndComp	
A/D converter, 8-channel, 15-bit, $\pm 10V$ to $\pm 20$ mV in five ranges. Measures resistance, current, thermocouples, RTD's and thermistors. Has DC/DC converter, DSP function.	6408	Sensoray (4901)		I/O expansion board. Expands the IOMUX channel to 512 points.	60-6MT	Digitronics	40
Analog to digital converter, 8-Bit.	RP050	HiTech		IEEE-488 Intelligent interface hardware and software.	77612201	NationalInst	
Analog to digital converter, 12-Bit.	RP051	HiTech		IEEE-488 Interface and handler GPIB-PC IIA + AEGIS Handler.	77612101	NationalInst	
Analog to digital converter, 16/32 input 8-Bit A/D converter. Works on MOCEEbus.	S-A/D	Magnum		IEEE-488 Interface and handler GPIB-PC2000.	77611201	NationalInst	
Analog-to-digital evaluation board, high speed, 8-bit, 50 MSPS.	TDC1025E1C	TRW-LSI	15	Interface to industry standard optical isolated module racks. 24 I/O lines.	Sup7	Octagon	
Analog-to-digital evaluation board, 7-bit, 20MSPS.	TDC1047E1C	TRW-LSI		Level-triggered latching input module, eight optoisolated inputs.	AOLLI-8	IndComp	45
Analog-to-digital evaluation board, 8-bit, 20MSPS.	TDC1048E1C	TRW-LSI		Opto-22 I/O interface. TTL level parallel I/O using 8255 PPI for connection to Opto-22 style isolated I/O module racks.	RP031	HiTech	
Analog-to-digital evaluation board, 9-bit, 15MSPS.	TDC1019E1C	TRW-LSI		Parallel I/O and timer/counter. 32 I/O lines plus four timer/counters.	S-PAR	Magnum	
Digital to analog converter, four D/A voltage outputs.	60D/A12B-4	Digitronics		Parallel I/O module. TTL level signals from an 825 PPI for printer interface or 24-bit general purpose parallel I/O lines.	RP030	HiTech	
Digital to analog converter, two D/A voltage outputs.	60D/A12B-2	Digitronics	20	Plug into ICD models 1018-PC and A/D12B32-PC. 32-channel input opto-isolator module for incoming ac or dc signals.	AOISO-32 AOISO-320	IndComp IndComp	50
Digital to analog converter, two 4 to 20 mA outputs.	60D/A12A-2	Digitronics		Plug into ICD models 1018-PC and A/D12B32-PC. 8 A/D inputs and two current loop outputs, 7 digital input lines.	AOAD-82864	IndComp	
Digital to analog converter, 8-Bit.	RP060	HiTech		RAMport I/O module. Async. serial interface using 8250 with rate generator and voltage conversion on card. RS-232 serial port.	RP010	HiTech	
Digital to analog converter, 12-Bit.	RP061	HiTech		RAMport I/O module. RS-422 serial interface using 8250 with rate generator and voltage conversion on card.	RP011	HiTech	
High resolution programmable integrating A/D converter (modular). Used for data acquisition systems, medical instruments, and automatic test equipment.	AD1170	AD					
Six bit 25 MSPS analog to digital converter evaluation board.	1014PIC	TRW-LSI	25				
Eight bit D/A converter for the MOCEE bus.	S-D/A8	Magnum					
Eight bit 20 MSPS analog to digital converter evaluation board.	1007PIC	TRW-LSI					
Eight channel 12-Bit bipolar A/D converter.	1020	Basicon					
16-Bit A/D integrating converter, has four channels and signal conditioning. Uses the Sixnet IOMUXbus.	60A/D14-4	Digitronics					

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line	Supported System Function	Part Number	Source	Line
<b>Special</b>							
<b>I/O (Cont'd)</b>							
Relay output, eight relay outputs and opto-isolated inputs.	1027	Basicon		Memory expansion board available in 2, 4, and 8 Mbyte capacities. On-board enable/disable switch, works with Data Generals' MV/7800.	DR-7800	Dataram	
Serial port expansion to the IOMUX channel.	60-6MT-232	Digitronics		256K DRAM memory, 4, 8, 12 MB capacity parity, lifetime warranty.	SNXRAM	Clearpoint	
Dual serial port RS-232C with control signals, works on MOCEbus.	S-SER	Magnum		16K RAM, parallel printer port, optional battery backup.	Sup-9	Octagon	
12-Bit A/D and D/A, filters, prototype area, direct interface to all TMS320 EVMs and XDS <sup>†</sup> .	RTC/EVM320C-06 TI			256K ZIP DRAM memory board for Apollo DN 3000, 1.2 MB capacity.	DNXRAM	Clearpoint	
<b>Memories</b>				<b>Multifunction</b>			
Bubble memory card, 32 Kbyte, 1 FBM43DA device.	FBC401M3	FujitsuA	5	Bare board. You add chips to get the function you desire, floppy disk controller, EPROM programmer, more RAM or all three. When used in conjunction with the TINY188, the system will boot from MS/DOS and program EPROMs.	DDS188	Vesta	35
Bubble memory card, 64 Kbyte, 2 FBM43DA device.	FBC402M3	FujitsuA		RAMport socket, allows use of standard JEDEC 28-pin and 24-pin memory sockets for I/O modules in this family. Software controls switch between memory and memory mapped I/O devices.	RP000	HiTech	
Bubble memory card, 128 Kbyte, 1 FBM54DB device.	FBC501M4	FujitsuA		Real-time clock. Three 16-bit counter/timers. 16 TTL inputs, 16 TTL or high current outputs.	Sup-6	Octagon	
Bubble memory card, 128 Kbyte, 4 FBM43DA devices. Also available with 8 to 64 devices for memory expansion from 256 Kbyte to 2 Mbyte.	FBC404M3	FujitsuA		Real-time clock. 20-key keypad interface, display interface. 28 TTL I/O lines. Optional battery backup.	Sup-8	Octagon	
Bubble memory card, 128 Kbyte, 8-bit parallel interface, 1 FBM54DB device.	FBC501M4	FujitsuA	10	Remote sensing unit; 8 differential analog input channels; 4 voltage analog output channels, 8 digital input/output lines; fully CMOS design; programmable from any CPU via ASCII commands.	RSU	Intelicom	
Bubble memory card, 256 Kbyte, 8-bit parallel interface, 2 FBM54DB devices.	FBC502M4	FujitsuA		6502 or 65C02 with crystal oscillator 1 or 2 MHz, also available with 65SC802. Works on MOCEbus.	S-CPU	Magnum	40
Bubble memory card, 384 Kbyte 8-bit parallel interface, 3 FBM54DB devices.	FBC503M4	FujitsuA		<b>Prototyping Boards</b>			
Bubble memory card, 32 Kbyte, four 74 Kbit serial loop organized FBM31DB, Typical access time, 370 ms.	FBC304M1A	FujitsuA		Development board for 32008, 32016, and 32032 processors.	DB32000	National	
Bubble memory card, 32 Kbyte, typical access time, 4.5 ms.	FBC304D2A	FujitsuA		Development system for PEEL devices. Contains editor, logic assembler, translator programmer, and tester all in one system.	PDS-1PEEL	ICT	
Bubble memory cassette system for FBM43CA cassette, 273,745 bits (total), 32 Kbyte user area.	FBM-u404 FBM4404P	FujitsuA FujitsuA	15	RAMport bus interface suitable for solder, Wire Wrap, or IDC construction of custom RAMport compatible interfaces.	RP020	HiTech	
Bubble memory cassette system, 1 Mbyte.	FBM-C128GA	FujitsuA		<b>Miscellaneous</b>			
Bubble memory cassette, 273,745 bits (1033 bits x 265 loops, major-minor loop (block replication transfer)).	FBM43CA	FujitsuA		Active signal conditioners. Adjustable gain, transducer excitation. Fully compatible with the PCI-20000 personal computer instrumentation system.	PCI20044T-1 PCI20045T-1	Burr-Brown Burr-Brown	45
Bubble memory cassette, 74,032 bits (total), 65,536 bits (effective), serial loop.	FBM31CA	FujitsuA		Active signal conditioners. Provides complete analog isolation to 750V, four channels. Used in pairs to provide eight channels.	PCI20042T-1 PCI20043T-1	Burr-Brown Burr-Brown	
Bubble memory control card for FBM31CA cassette.	FBC308C1A	FujitsuA		Demonstration board for 16G040 clock and data recovery circuit used in analog and fiber communications.	90GCDR	GigaBit	
Bubble memory control card for FBM43CA cassette, RS232C interface.	FBC404C3S	FujitsuA	20	Digital Direct Frequency Synthesizer (130 MHz)	STEL9272	STI	(3208)
Bubble memory control card for FBM43CA cassette, 8-bit parallel interface.	FBC404C3A	FujitsuA		EPROM programmer, programs 2716, 2732, 2764, 27128, 27256, and 27512 devices.	RP070	HiTech	50
Bubble memory expansion card for 8 FBM43DA devices, 256 Kbyte.	FBC408D3	FujitsuA		EPROM programmer for MC-1Z board.	1026	Basicon	
Bubble memory expansion card, 4 FBM43DA devices, 128 Kbyte.	MDC404D3	FujitsuA		EPROM programmer for MC-11 board.	1025	Basicon	
Bubble memory expansion card, 512 Kbyte 4 FBM54DB devices.	FBC504D4	FujitsuA		EPROM programmer for MC-2i board.	1039	Basicon	
Bubble memory interface adapter for 1 Mbyte bubble memory, RS232C interface.	FBMA002 FBMA003	FujitsuA FujitsuA	25	Evaluation board for Datel's ADC-300 A/C flash converter. Can also serve as self-supporting high speed A/D board.	ADC-B300E	Datel	(2575)
Memory board with 32K bytes of RAM available for use on MOCEbus.	S-MEM2	Magnum					
Memory board with 32K bytes of ROM available for the MOCEbus system.	S-MEM3	Magnum					
Memory board with 8K of RAM or 8K of ROM, works with MOCEbus.	S-MEM	Magnum					
Memory expansion board available in 2, 4, and 8 Mbyte capacities. On-board enable/disable switch, works with Data Generals' MV/10000, MV/4000, and S/280.	DR-280	Dataram	30				

† Military Temperature Range (-55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

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## MICROCOMPUTER—SUPPORT BOARDS (Cont'd)

Supported System Function	Part Number	Source	Line
<b>Special</b>			
<b>Miscellaneous (Cont'd)</b>			
Evaluation board for Datel's ADC-301 flash converter. Can also serve as a self-supporting high speed A/D converter board.	<b>ADC-B301E</b>	<b>Datel</b>	<b>(2575)</b>
Evaluation board for Datel's ADC-302 flash converter. Can also serve as a self-supporting, high speed A/D converter board.	<b>ADC-B302E</b>	<b>Datel</b>	<b>(2575)</b>
Evaluation Module. Supports code development for the MC68HC05CX, BX and LX MCU's, programs code into the MC68HC805C4/C8 EEPROM/MCUs.	M68HC05EVM <b>M68HC11EVM</b> M68HC99EVM	Motorola <b>Motorola</b> Motorola	<b>(2899)</b>
Evaluation PCB Assembly. Provides economical means of debugging, assemble/disassemble of user assembly code. Evaluation target system using the MC68HC11AX.	<b>M68HC11EVB</b>	<b>Motorola</b>	<b>(2899)</b>
FSK Radio Receiver	SM450	Siltronics	
Modular signal conditioners. Analog input/output modules for direct interface to sensors such as thermocouples, RTDs, millivolt, and voltage sources.	5B SERIES	AD	
Motor driver, quad stepper motor driver.	1043	Basicon	
MPU 6805 evaluation board. Designed to be a basic hardware and software development tool. Enables the designer to construct and debug a hardware model of a proposed device that incorporates the MPU 6805 standard cell microprocessor core.	SXP38999XX05	Motorola	
Multisensor A/D interface for thermocouples, voltage, RTDs, thermistors, or current. Software programmable gains, eight channels. Full range sensor linearization using on-board microprocessor and 14-bit A/D.	<b>6408</b>	<b>Sensaray</b>	<b>(4901)</b>
Numerically controlled oscillator (NCO) evaluation board. For the ST1172A NCO. Resolution from 1 Hz to 10 MHz, sine wave or TTL square wave output.	<b>STEL9172</b>	<b>STI</b>	<b>(3207)</b>
Power module, 5 volt system supply.	1017	Basicon	
Programmable power supply, provides output proportional to digital control word.	RP062	HiTech	
Serial Viterbi Decoder	<b>STEL9268</b>	<b>STI</b>	<b>(3211)</b>
Supports code development for the MC146870SE2/3, MC146805F2/G2/H2. Also programs code into MC146870SG2 and MC146870SF2, UV-EEPROM/MCUs.	M1468705EVM	Motorola	
Supports code development for the MC6805P2/P3/J2/J1, MC68HC04P2/P3, and MC68704P2. Also programs code into the MC68704P2, EPROM/MCU.	M68HC04EVM	Motorola	
System Performance Analyzer (SPA) analyzes program execution activities on the target MPU/MCU bus. For HDS-300 and MC68020 systems.	M68HDS300SPA	Motorola	
Eight channel solid-state relay module. Switch up to 24V dc at 1 A.	AOSSR-8	IndComp	
4 Digit .3" Display Module. Can be extended to 8, 12, 16, etc.	LN4	CAN-TRON	
8-Bit, 20 MHz sampling A/D board. Designed around the Datel ADC304 flash converter which is TTL compatible. Contains a buffer amplifier as well as filtering and timing circuitry.	ADC-B304E	Datel	

† Military Temperature Range (–55° to 125°C)

‡ High Radiation Resistance

\*Typical Value

°Macrocell

◊ Available in Surface Mount Package

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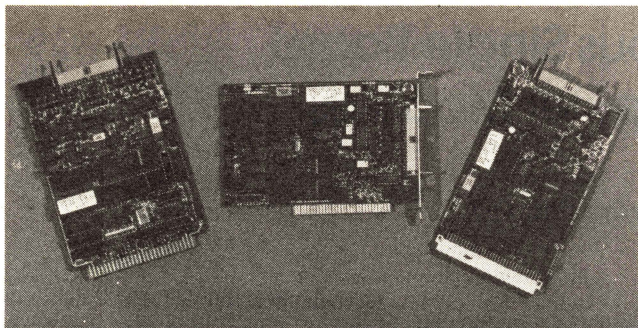
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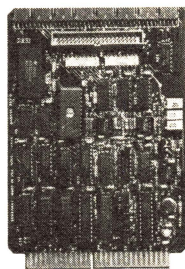
## MULTISENSOR INTERFACES PC BUS, STD BUS, G64 BUS



### MODELS 409, 7408, 7409, 6408

- Sensors connect to 40-pin ribbon cable connector, 7409TA, or directly to card depending on model selected
- EEPROM stores calibration data
- Supports any combination of RTD's thermocouples, strain/pressure gauges, thermistors, or voltage inputs
- Open-sensor detection
- Full range sensor linearization using on-board microprocessor and 14-bit A/D
- Pulsed excitation reduces self-heating in resistive sensors
- Software programmable limit values, digital filter, strain gauge factors
- Common mode voltage protection to 95 VAC

## RTD TEMPERATURE INTERFACE



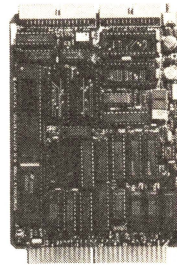
### MODEL 7404 - STD BUS

- Eight RTD's connect directly to board or 7404T terminator
- Linearizes 385 and 392 type RTD's using on-board ROM lookup table
- 12-bit A/D provides 0.3906C temperature resolution
- Supports two-, three-, and four-wire sensors
- Open-sensor detection
- Pulsed excitation reduces RTD self-heating

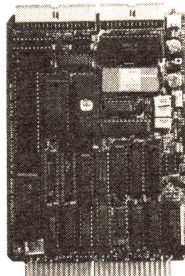
## CMOS PROCESSOR

### MODEL 7410 - STD BUS

- Z80 code-compatible CMOS processor (NSC800)
- 64K address space. JEDEC sockets for 8K/16K EPROM and 8K/32K RAM
- RS-422/232 serial port plus strobed parallel port
- Five programmable counter/timers
- Reset switch
- Sockets for 12-bit A/D, 16-channel multiplexer and incremental encoder interface



## 12-BIT A/D PROCESSOR



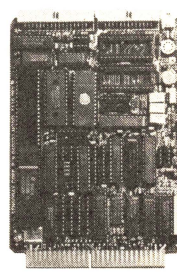
### MODEL 7411 - STD BUS

- 16-channel S.E. or 8-channel D.I. expandable to 256 S.E./128 D.I.
- Programmable limits, sample rate, buffer size, low pass filter, time-of-day clock
- Waveform capture mode with programmable pretrigger/posttrigger
- 25us, 12-bit A/D converter
- $\pm 5V$ ,  $\pm 10V$ , 0-10V ranges
- Linearization for J,K,T,S thermocouples

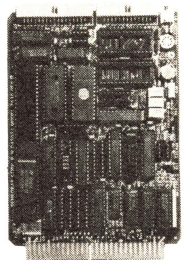
## PROGRAMMABLE CONTROLLER

### MODEL 7412 - STD BUS

- Supports up to 256 digital I/O signals when used with 7412T series termination boards
- 16-bit event counter per channel
- Outputs may be boolean function of other outputs, inputs, time-of-day clock
- Performs switch debouncing of inputs
- Programmable output sequencing, input change detection, time delays, output pulse rate



## COMMUNICATION PROCESSOR



### MODEL 7413 - STD BUS

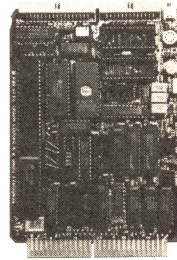
- Spooler for serial/parallel data communication using 28K buffer
- Compatible with RS-485 and RS-232
- Centronics printer output port
- On-board CMOS computer executes high-level commands from master CPU
- Programmable BAUD rate, buffer sizes, character filtering, checksum, and link and error-recovery protocols.

## BAR CODE PROCESSOR

### MODEL 7415

#### STAND-ALONE OR STD BUS

- Interfaces to Hewlett-Packard HEDS-3250 or equivalent wand
- Converts CODE-39, UPC, EAN, CODEABAR, 2/5 to ASCII
- RS-422/232 serial data link to external computer
- Centronics printer port for print-on-demand label generation
- Functions as slave processor on system bus



# SENSORAY

44106 OLD WARM SPRINGS BLVD.  
FREMONT, CA 94538 415-657-9331

Sensoray

μC BOARDS



## PG2004 / PG2009 VMEbus Single Board Computer Modules

### Standard Products

#### DESCRIPTION

The VMEbus Single Board Computer modules is one of the high performance building blocks in our Modular Board product family. It embodies, in a single module, a 68000 based computing function capable of supporting high speed data processing and control environments. This module is ideally suited for a wide range of applications. As a ROM based, single board computer, it is usable in a stand-alone application requiring no card cage or supporting modules. This provides the user with a compact computing nucleus for dedicated applications. The flexibility extends upward to include memory management for use in more general purpose, disc based, applications requiring multiprogramming/multi-tasking solution. All local I/O devices employ interrupt protocols for programming ease and fast response. This module is designed utilizing multilayer printed circuit techniques with internal power and ground planes in order to minimize noise and provide a reliable, industrial grade product. The Module is easily configured to support a wide variety of applications.

### Preliminary Specification

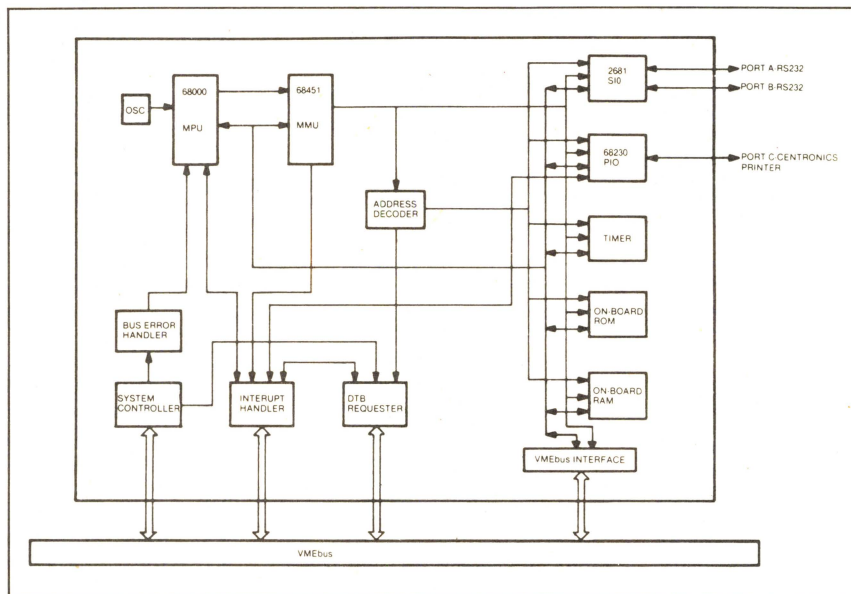
#### FEATURES

- 8 MHz (10 MHz optional) 68000 (68010 optional) 16-bit CPU
- Memory management unit 68451
- On-board memory up to 128kB ROM / PROM / EPROM and 16kB RAM
- Peripheral I/O ports: two RS-232 serial (2681) one parallel (68230)
- Programmable real-time clock (24-bit timer)
- Seven levels of interrupt
- System controller functions
- Selectable address mapper
- Bus control, arbitration, time out, and error handling functions
- VMEbus compatible

#### ORDERING INFORMATION

DESC.	PART NO.	ORDER CODE
68000 8 MHz	PG2004	9464 020 04001
68000 +MMU/ 8 MHz	PG2005	9464 020 05001
68000 10 MHz	PG2006	9464 020 06001
68000 +MMU/ 10 MHz	PG2007	9464 020 07001
68010 10 MHz	PG2008	9464 020 08001
68010 +MMU/ 10 MHz	PG2009	9464 020 09001

#### BLOCK DIAGRAM





Standard Products

Preliminary Specification

DESCRIPTION

Philips' PG2020 Family of Central Processor Modules offers a choice of 10 modules, allowing systems designers to choose precisely the functions they need. The modules are based on 68000 or 68010 microprocessors running at either 8 or 10 MHz. There is an optional 68451 MMU. On-board memory comprises sockets for up to 128 kB of ROM/ EPROM and a choice of 128 kB or 512 kB dual-ported dynamic RAM memory. An optional floating-point-processor unit (PG1990), based on the NS16081 FPP, can be added to any CPU in the family.

This flexibility allows the user to choose the right module for a particular application, including memory management in general purpose, disc-based applications that require multiprogramming/

multi-tasking systems. Full interrupt handler and requester and dual access dynamic RAM enables all members of the family to operate effectively in multi-processor applications. For ease of programming and fast response all local I/O devices employ interrupts to initiate communication.

Designed primarily for multi-processor applications, the modules contain no system controller functions which must be added in the VMEbus system.

The PG2020 Family are reliable, industrial standard products on multilayer printed circuit boards with internal power and ground planes to minimize noise.

FEATURES

- Choice of 10 modules
- 68000 or 68010 microprocessors
- 8 or 10 MHz
- Optional 68451 MPU
- On-board memory:
  - ROM/EPROM up to 128 kB
  - Dual-ported RAM 128 or 512 kB
- Peripheral I/O: two RS-232C ports
- Programmable real-time clock and 24-bit timer
- Full interrupt handler and requester
- IPL vector
- VMEbus compatible

ORDERING INFORMATION

PART NO.	ORDER CODE	MPU	MMU	SPEED	DRAM CAPACITY
PG2020	9464 020 20001	68000	None	8 MHz	128 kB
PG2021	9464 020 21001	68000	68451	8 MHz	128 kB
PG2022	9464 020 22001	68000	None	10 MHz	128 kB
PG2023	9464 020 23001	68000	68451	10 MHz	128 kB
PG2024	9646 020 24001	68000	None	8 MHz	512 kB
PG2025	9646 020 25001	68000	68451	8 MHz	512 kB
PG2026	9646 020 26001	68000	None	10 MHz	512 kB
PG2027	9646 020 27001	68000	68451	10 MHz	512 kB
PG2028	9646 020 28001	68010	None	10 MHz	512 kB
PG2029	9646 020 29001	68010	68451	10 MHz	512 kB

### Standard Products

### Preliminary Specification

#### DESCRIPTION

Philips' PG2030/2031/2032 68010 based Processor Modules are for multi-processor applications and provide VMXbus sub-system design capability plus off-loading of VMEbus for improved system performance.

Memory management is optionally available. Two RS-232C channels are provided with industry standard baud rates using a 68681 communication controller together with a 16-bit timer. Two 8-bit or one 16-bit parallel I/O ports and a 24-bit resident timer are also available.

The 68172 VMEbus controller is used for VMEbus master/slave interface.

PG2030/2031/2035 are reliable, industrial standard products on Double Euro-card multilayer printed circuit boards with internal power and ground planes to minimize noise.

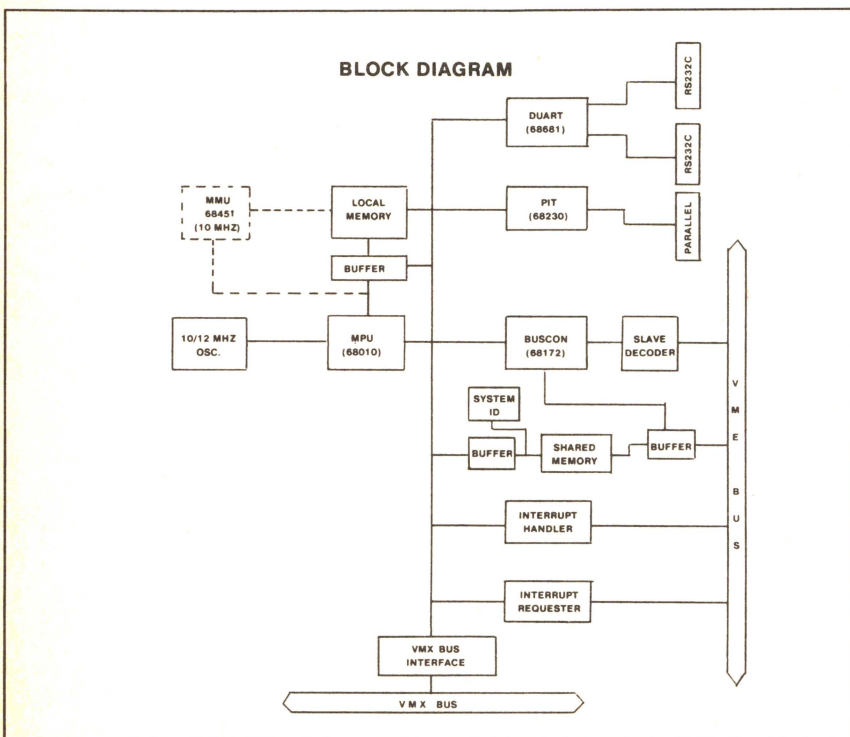
#### FEATURES

- 68010 virtual memory processor at 10-12.5 MHz
- Optional 68451 for memory management
- Four 28-pin sockets for up to 256 kB of ROM/EPROM (128 kB SRAM) local memory
- Two 28-pin sockets for up to 128 kB of ROM/EPROM or (64 kB SRAM) shared, dual ported memory
- 68172 VMEbus controller
- Two RS-232C communication ports (68681)
- 68230: dual 8-bit I/O ports with 24-bit timer (68230)
- Interrupt handler/requestor for seven on/off-board levels
- Two timers: 24-bit and 16-bit
- Memory map changes by reprogramming 82S153/82S157/82S159

#### ORDERING INFORMATION

DESCRIPTION	TYPE NO.
VME/VMX CPU, 10 MHz	PG2030
VME/VME CPU with MMU, 10 MHz	PG2031
VME/VMX CPU, 12 MHz	PG2035

#### BLOCK DIAGRAM





## PG8000 VMEbus Single Board Computer

### Standard Products

### Preliminary Specification

#### DESCRIPTION

Philips' PG8000 single board computer is intended for monoprocessor or multiprocessor systems in VMEbus environments or in stand-alone applications. The module is based on a 68008 MPU. In stand-alone mode the module can operate independently from the VMEbus, thus making it ideal for evaluation, education and small automation systems.

In a VMEbus environment the module can be used in a range of applications extending from simple monocomputer systems to more demanding high performance systems.

The PG8000 is a reliable, industrial standard product on a multi-layer printed circuit board with internal power and ground planes to minimize noise.

#### FEATURES

- Single Eurocard
- Single board computer
- 68008 MPU at 8 MHz
- D8 data bus
- A24 address bus
- Two 28-pin JEDEC memory sockets for ROM/RAM
- Slot one functions
- Arbiter one option
- 2 × RS-232C serial port
- 16-bit timer
- RESET and ABORT pushbuttons
- HALT LED indicator
- VMEbus compatible

#### ORDERING INFORMATION

DESC.	PART NO.	ORDER CODE
SECPU8-8	PG8000	9464 080 00001

PG3101/PG3102  
VMEbus Disk  
Controller Module

Standard Products

Preliminary Specification

DESCRIPTION

The VMEbus Disk Controller Module is another addition to the high performance building blocks in the Signetics Module Board product family. It contains in a single module, a high speed microprocessor supervised disk controller which interfaces to the industry's most popular hard and floppy disk drives. The Disk Controller Module provides a high performance data channel between multiple disk drives and the VMEbus system main memory. Intended as an intelligent peripheral interface, the Disk Controller includes a straight forward, high level interface to the system software by utilizing device control block (DCB) and direct memory access (DMA) protocols. Designed utilizing multi-layer printed circuit techniques with internal power and ground planes to minimize noise, the Signetics Disk Controller Module provides a reliable, industrial grade product.

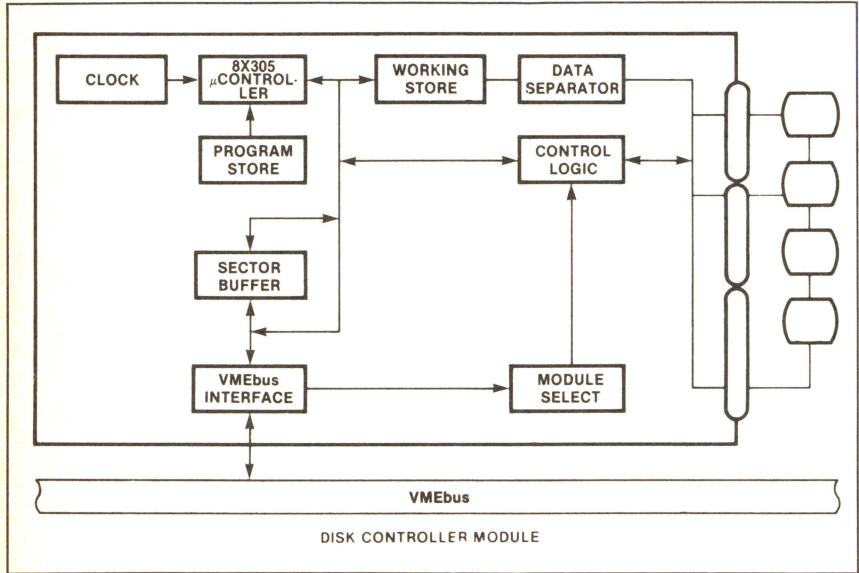
FEATURES

- **Mixed media mass storage control**  
— Supports up to four 5¼" and 8" Winchester and floppy disk drives per module
- **Bus master**  
— DMA between main memory and disk drives controlled by an on-board Signetics 8X305 bipolar microprocessor
- **Flexible formats**  
— IBM standard or user defined
- **Error recovery mechanisms**  
— Error correction and detection built-in
- **VMEbus compatible**

ORDERING INFORMATION

DESCRIPTION	TYPE NO.
VMEbus Disk Controller Module	SMVME4300
VMEbus Disk Controller Module User Manual	SMMAN3040

BLOCK DIAGRAM



Signetics

μC BOARDS



Preliminary Specification

Standard Products

DESCRIPTION

The System 9000 is a powerful and highly versatile system created by the integration of standard VMEbus board level products, the associated standard mechanical hardware, and base target software. The System 9000 is fully integrated and tested as a system. The optional software described in this document will support the specific hardware configurations.

The two configurations of the System 9000 can be used in target evaluation or for software development with the appropriate software options. It provides a complete VMEbus based system. The option UNIFIVE (UNIX SYSTEM V, Release 2) operating system features include optimized C compiler, Fortran-77 compiler, IEEE floating point capability, record/file level locking, text loitering, text sharing, and bad block handling. Furthermore the OEM is able to develop his application on the very same hardware that he can use as his target system, eliminating problems of different development and target environments. The System 9000 is a versatile target system. Since it is based on our standard VMEbus boards and has four spare expansion slots, the customer may tailor the system to his specific needs using the wide range of VMEbus based products. At a minimum it provides a complete prototype development environment. No need to worry about ground loops, shielding, FCC regulations, EMI, cabling and other system integration problems.

FEATURES

- Integrated system serves in development and target environments
- FCC class A equipment certification
- PG9001 basic system with 7 VMEbus slots, power supply and fans with PG9010 cabinet
- PG2009 10MHz 68010 single board computer with 68451 MMU
- PG2205 1MB DRAM board with parity
- PG3102 intelligent multiple disk controller
- PG4200 pSOS-68K™ real-time kernel, its companion debugger pROBE-68K and SIGFILE file system
- 3.3MB floppy disk drive
- 53.33MB Winchester disk drive

OPTIONS

- PG3301 four channel serial I/O board
- PG5400 UNIFIVE Unix™ System V release 2 with berkeley enhancements, optional
- PG5600 CP/M-68K™ disk operating system

pSOS-68K and pROBE-68K are trademarks of Software Component Corporation.

Unix is a trademark of AT&T Corporation.

\*CP/M-68K is a trademark of Digital Research Corporation.

ORDERING INFORMATION

PART NO.	RAM SIZE	HARD DISK	FLOPPY DISK	SERIAL PORTS
PG9105	1 MB	—	3.3MB	2
PG9106	1 MB	53.33MB	3.3MB	2

Note that all hard and floppy disk capacities are unformatted.

## PG4100 Embedded Real-Time Monitor System

### Standard Products

### Preliminary Specification

#### DESCRIPTION

The ERM System is a compact operating system with a File Management System which together provide an environment for user-written application programs. ERM System may be used with the full range of PHILIPS' VMEbus 68000 CPUs.

An important feature of the ERM System is the PMON-68k Stand-Alone Monitor Debugger which is included with all versions of ERM System.

As ERM System is downwardly compatible with the DRM and SRM Systems, programs developed to run on ERM System will run on DRM System and SRM System with no alteration.

ERM System is offered to the user in four versions.

#### FEATURES

- **Compact real-time operating system with file management system**
- **Development system and language independent**
- **Optional run-time support for: CP/M-68K™, VAX/VMS™ and UNIFIVE™**
- **Includes PMON-68K stand-alone monitor debugger**
- **Compatible with DRM System™ and SRM System™**
- **Easy to use interface through user traps**
- **No sysgen required**
- **Hardware configuration independent**

#### ORDERING INFORMATION

- See VMEbus/68000 Product Catalog
- A signed Software Licence Agreement is required before shipment

CP/M-68K is a trademark of Digital Research Inc.  
VAX/VMS is a trademark of Digital Equipment Corporation.

UNIFIVE has been derived from UNIPUS +, a trademark of Unisoft.

DRM System: Distributed Real-Time Multiprocessor System.

SRM System: Small Real-Time Monitor System.



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## WDLAN-H 10 Port Stand-Alone StarLAN HUB

### FEATURES

- COMPLIES WITH IEEE 802.3 1BASE5 STARLAN STANDARD
- TEN LOWER-LEVEL PORT INPUTS
- SUPPORTS NETWORKS WITH UP TO TEN HUB LEVELS
- SIGNAL REGENERATION AND RETIMING ON ALL PORTS
- COLLISION DETECTION AND SIGNALLING
- AUTOMATIC DETECTION OF UPPER-LEVEL HUB PRESENCE
- OPTION FOR NOT RETIMING
- SIX LED STATUS AND DIAGNOSTIC INDICATORS
- NO TERMINATION OR LOOPBACK PLUGS REQUIRED
- TRANSIENT VOLTAGE PROTECTION ON ALL PORTS
- SIGNAL FILTERING ON ALL PORTS
- 1 MBPS MANCHESTER SIGNAL REGENERATION
- BASED ON WD83C510A STARLAN HUB CONTROLLER CHIP
- MANUALLY-OPERATED SYSTEM TEST
- SEPARATE POWER ADAPTER SUPPORTS INPUT VOLTAGE OF 115 VAC/60 HZ OR 230 VAC/50-60 HZ
- POWER ADAPTER OUTPUT VOLTAGE OF 12 VAC, 50 OR 60 HZ
- POWER DISSIPATION OF 12 WATTS
- DIMENSIONS OF 13.8" W, 6.6" D, 2.0" H

## WD8003E High-Performance Ethernet PC Adapter Board

### FEATURES

- UNIQUE PC SHARED MEMORY INTERFACE: DUAL-PORTED 8K MEMORY SHARED WITH PC FOR HIGHEST THROUGHPUT
- NO PC DMA CHANNELS REQUIRED
- 10 MBPS OPERATION, CSMA/CD
- MEETS ETHERNET AND IEEE 802.3 STANDARDS
- ON-BOARD TRANSCEIVER FOR THIN ETHERNET INTERFACE
- HIGH-PERFORMANCE, LOW-POWER CMOS LAN CONTROLLER CHIP
- OPERATES IN IBM PC™, PC XT™, PC AT™, PS/2™  
– MODELS 25 AND 30, AND COMPATIBLES WITH SYSTEM CLOCKS UP TO 16 MHZ
- SAME PC SOFTWARE INTERFACE IS USED BY WD8003S STARLAN ADAPTER BOARD
- AVAILABLE WITH WESTERN DIGITAL'S VIANET® OPERATING SYSTEM, NOVELL'S ADVANCED NETWORK®, AND TCP/IP
- WESTERN DIGITAL'S NET BIOS/OSI INTERFACE PROGRAM SUPPORTS APPLICATIONS SUCH AS MICROSOFT'S MS-NET™ AND IBM PC LAN PROGRAM
- DIMENSIONS OF 5.25" W BY 3.9" H

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## WD8000SL – StarLAN PC Adapter Board

### FEATURES

- COMPLIES WITH IEEE 802.3 1BASE5 STARLAN STANDARD
- 1 MBPS OPERATION
- NETWORK LINKS UP TO 800 FEET
- SERVICES IBM PC™, PC XT™, PC AT™ AND COMPATIBLE COMPUTERS
- UNIQUE SMALL FORM FACTOR – ONLY 2.4" HIGH x 5.4" WIDE
- OPERATES IN SYSTEMS WITH BUS SPEEDS UP TO 16 MHZ
- JUMPER SELECTIONS FOR BASE I/O AND MEMORY ADDRESSES
- SOFTWARE ASSIGNMENT TO PC DMA CHANNELS 1, 2 OR 3
- CAN USE PC INTERRUPTS 2, 3, 4, 5, 6 OR 7
- UTILIZES WESTERN DIGITAL'S PC BUS LSI INTERFACE CONTROLLER
- STANDARD EIGHT-PIN MODULAR JACK FOR NETWORK CONNECTION
- OPTIONAL 16K BYTE BIOS ROM WITH IPL JUMPER SELECTION
- EIGHT BYTE LAN ADDRESS ROM
- MODULAR JACK FOR VOICE TELEPHONE CONNECTION
- SURFACE MOUNT TECHNOLOGY
- SOFTWARE COMPATIBLE WITH NOVELL'S ADVANCED NETWORK® AND BANYAN'S VINES™
- AVAILABLE WITH WESTERN DIGITAL'S VIANET® LAN OPERATING SYSTEM SOFTWARE AND NETBIOS/OSI INTERFACE PROGRAM

## WD8000SH/WD8000SH2 – StarLAN PC Adapter Boards with Integral One or Two-Port HUB

### FEATURES

- COMPLIES WITH IEEE 802.3 1BASE5 STARLAN STANDARD
- 1 MBPS OPERATION
- NETWORK LINKS UP TO 800 FEET
- SERVICES IBM PC™, PC XT™, PC AT™ AND COMPATIBLES
- OPERATES IN SYSTEMS WITH BUS SPEEDS UP TO 16MHZ
- JUMPER SELECTIONS FOR BASE I/O AND MEMORY ADDRESSES
- SOFTWARE ASSIGNMENT TO PC DMA CHANNELS 1, 2 OR 3
- CAN USE PC INTERRUPTS 2, 3, 4, 5, 6 OR 7
- INTEGRAL MINI-HUB PERMITS DAISY CHAIN OPERATION WITH ONE OR TWO INPUTS
- UTILIZES WESTERN DIGITAL'S PC BUS LSI INTERFACE CONTROLLER
- STANDARD EIGHT-PIN MODULAR JACK FOR NETWORK CONNECTION
- OPTIONAL 16K BYTE BIOS ROM WITH IPL JUMPER SELECTION
- STANDARD HALF-SIZE CARD FORM FACTOR
- EIGHT BYTE LAN ADDRESS ROM
- MODULAR JACK FOR VOICE TELEPHONE CONNECTION
- SURFACE MOUNT TECHNOLOGY
- SOFTWARE COMPATIBLE WITH NOVELL'S ADVANCED NETWORK AND BANYAN'S VINES
- AVAILABLE WITH WESTERN DIGITAL'S VIANET LAN OPERATING SYSTEM SOFTWARE AND NETBIOS/OSI INTERFACE PROGRAM

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## WD8003S High-Performance StarLAN PC Adapter Board

### FEATURES

- UNIQUE PC SHARED MEMORY INTERFACE; DUAL-PORTED 8K MEMORY SHARED WITH PC FOR HIGHEST THROUGHPUT
- NO PC DMA CHANNELS REQUIRED
- 1 MBPS OPERATION
- MEETS IEEE 802.3 1BASE5 STARLAN STANDARD
- HIGH-PERFORMANCE, LOW-POWER CMOS LAN CONTROLLER CHIP
- OPERATES IN IBM PC™, PC XT™, PC AT™, PS/2™ – MODELS 25 AND 30, AND COMPATIBLES WITH SYSTEM CLOCKS UP TO 16 MHZ
- NETWORK LINKS UP TO 800 FEET
- COMMON PC SOFTWARE INTERFACE FOR STARLAN AND ETHERNET/THIN ETHERNET (USING WESTERN DIGITAL'S WD8003E ETHERNET PC ADAPTER BOARD)
- AVAILABLE WITH WESTERN DIGITAL'S VIANET® OPERATING SYSTEM, NOVELL'S ADVANCED NETWORK®, AND TCP/IP
- WESTERN DIGITAL'S NETBIOS/OSI INTERFACE PROGRAM SUPPORTS APPLICATIONS SUCH AS MICROSOFT'S MS-NET™ AND IBM PC LAN PROGRAM
- DIMENSIONS OF 6.0" W by 3.9" H

## WD8003SH High-Performance StarLAN PC Adapter Board with Integral One-Port HUB

### FEATURES

- UNIQUE PC SHARED MEMORY INTERFACE; DUAL-PORTED 8K MEMORY SHARED WITH PC FOR HIGHEST THROUGHPUT
- NO PC DMA CHANNELS REQUIRED
- 1 MBPS OPERATION
- MEETS IEEE 802.3 1BASE5 STARLAN STANDARD
- HIGH-PERFORMANCE, LOW-POWER CMOS LAN CONTROLLER CHIP
- OPERATES IN IBM PC™, PC XT™, PC AT™, PS/2™ – MODELS 25 AND 30, AND COMPATIBLES WITH SYSTEM CLOCKS UP TO 16 MHZ
- COMMON PC SOFTWARE INTERFACE FOR WESTERN DIGITAL'S STARLAN AND WD8003E ETHERNET/THIN ETHERNET PC ADAPTER BOARDS
- INTEGRAL MINI-HUB PERMITS DAISY CHAIN OPERATION
- UTILIZES WESTERN DIGITAL'S MINI-HUB CONTROLLER
- OPTIONAL 16K BYTE BIOS ROM WITH IPL JUMPER SELECTION
- AVAILABLE WITH WESTERN DIGITAL'S VIANET OPERATING SYSTEM, NOVELL'S ADVANCED NETWORK, AND TCP/IP
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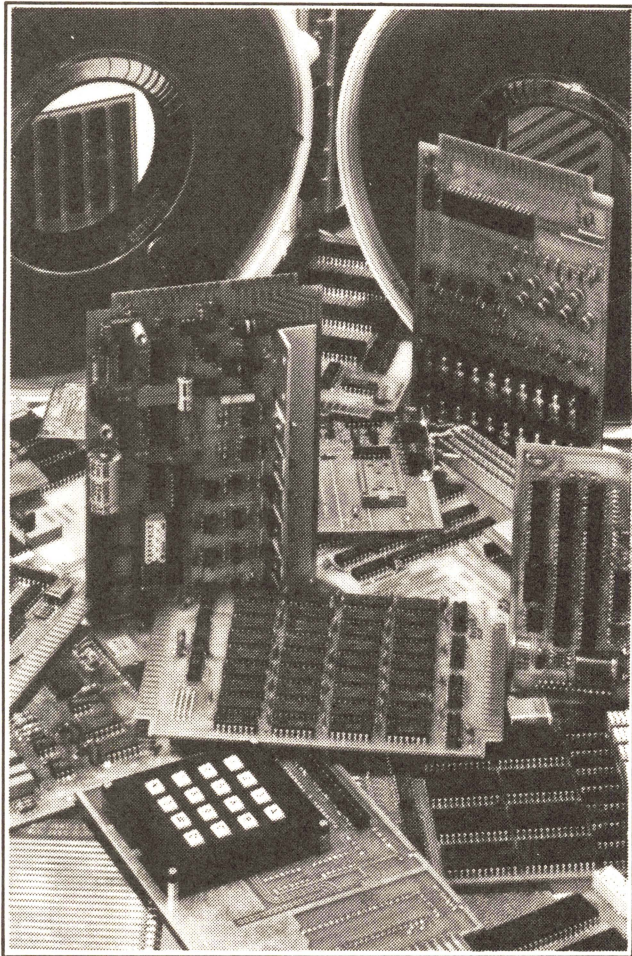
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- Software Development Tools
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Items listed on this page are just a sample of Wintek's wide product line. Call us toll free to request a complete catalog of Wintek products and services.

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All modules are 4.5 by 6.5 inches. Unit prices are listed. Quantity discounts for micro modules are: 10-24, 10%; 24-49, 20%; 50-99, 30%; 100-499, 40%; 500+, 50%. Manuals are available for \$5 per module.

MCH18	6809 MPU, 2K RAM, 3 ROM Sockets, 2 RS-232 serial ports, 4 parallel ports, watchdog timer, real-time clock	\$212
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MC111	16-button keypad with fifteen 7-segment LED displays	\$199
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PAS11	68HC11 Macro Assembler	\$495
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PCC01	6801 C Compiler and Macro Assembler	\$895
PCC09	6809 C Compiler and Macro Assembler	\$895
PCC11	68HC11 C Compiler and Macro Assembler	\$895

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### IC Options

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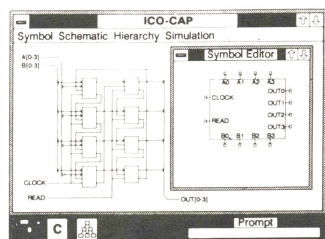
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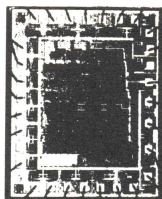
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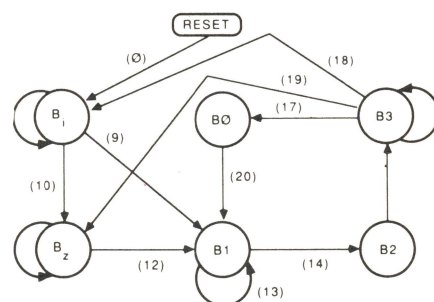
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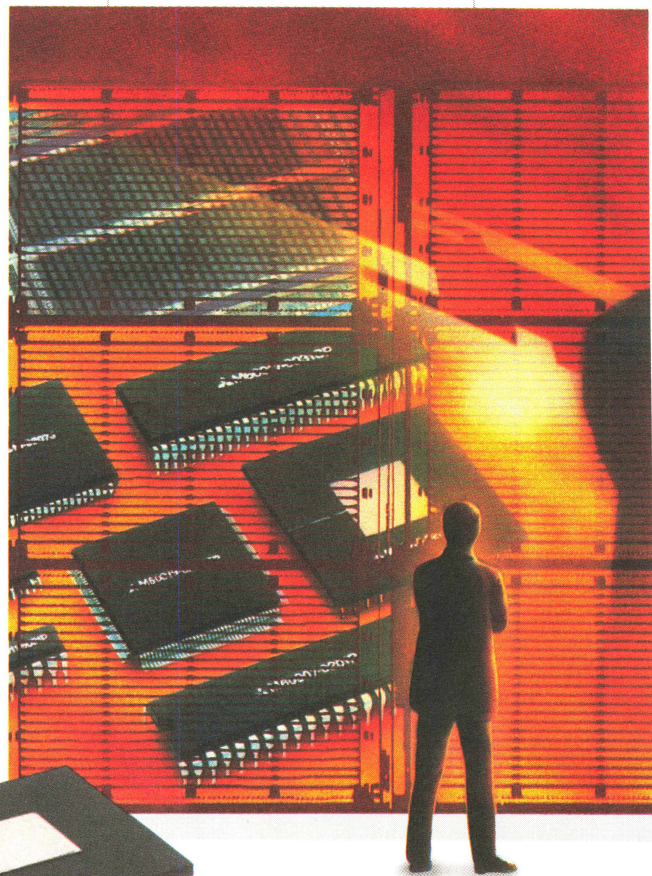
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Mitsubishi's design centers, located in Sunnyvale, CA and Durham, NC, are networked with Regional Technical Centers and a gate array engineering support staff ready to assist in all phases of design.

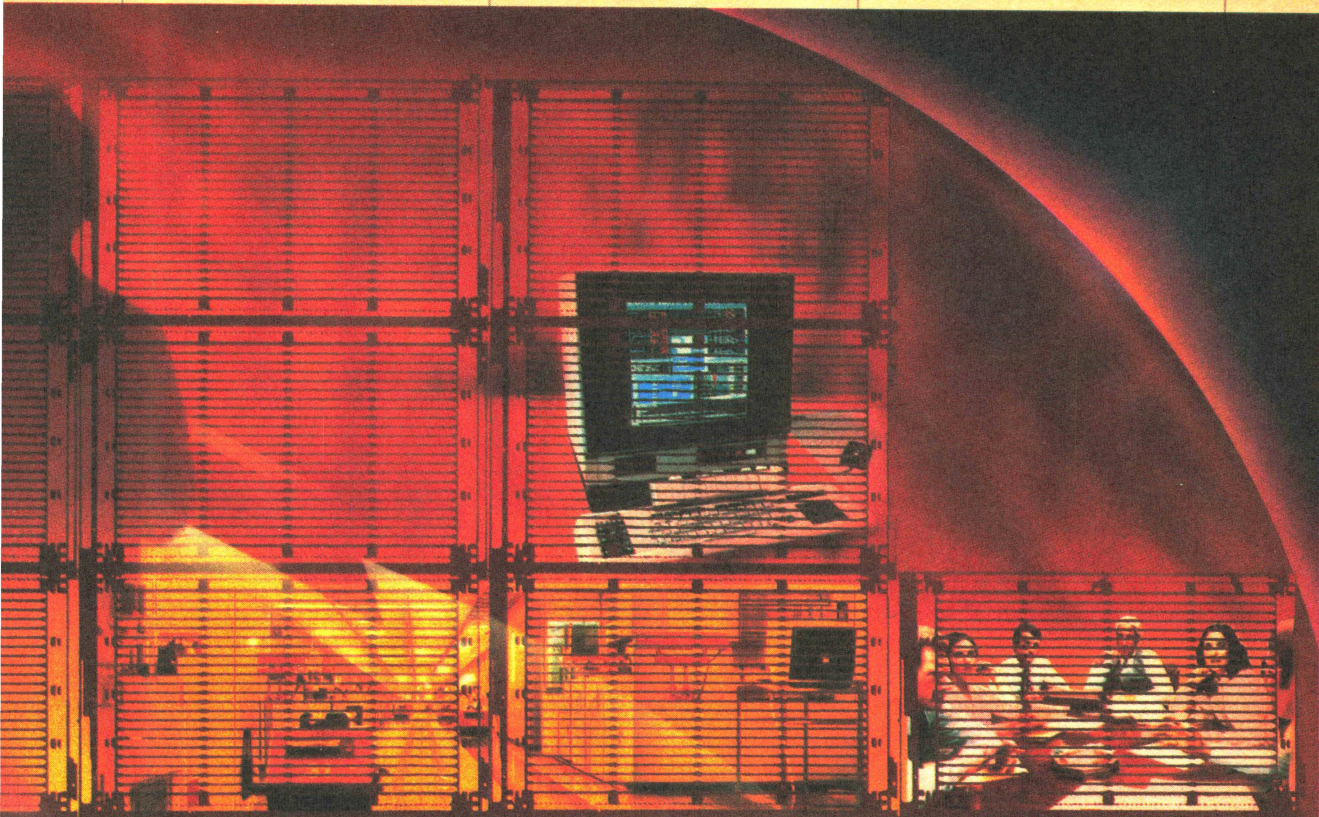
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## PACKAGING:

Mitsubishi offers a broad range of industry-standard and proprietary packaging options. A leadership foundation in high pin count surface-mount packages includes quad flat packages (QFP), now available with 160 leads and soon over 200. Mitsubishi provides a cost-effective alternative to PGAs by mounting QFPs on a PC board adaptor.





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Low power, 1.3 $\mu$ m, double metal CMOS technology is available today, with sub-micron levels on the way. Mitsubishi's patented\* gate isolation structure provides 10% to 20% faster performance, with a 15% to 25% higher gate density than conventional oxide isolation.

\*U.S. Patent No. 4,562,453

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#### DESIGN SUPPORT:

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